

# VFXO321

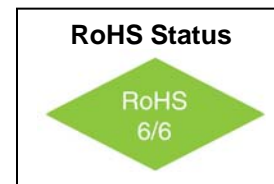
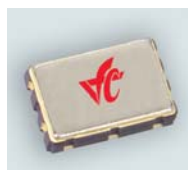
## XO Ultra Low Jitter 2.5V, 3.3V

### 5x7mm SMD, LVPECL / LVDS / LVCMOS



#### Features

- 16MHz to 800MHz Frequency Range
- Differential Output Levels (LVPECL/LVDS)
- Single Ended LVCMOS output available
- <0.2ps jitter RMS over 12KHz ~ 20MHz
- Selectable OE Logic



#### Applications

- Optical Networking, SONET / SDH
- 10 Gigabit Ethernet
- Broadband Access

#### Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Frequency Range	F		60 16		800 320	MHz	PECL / LVDS CMOS
Frequency Stability	$\Delta F/F$	Vs. Operating Temperature			$\pm 50$ $\pm 25$ $\pm 20$	ppm	Order Code B Order Code C Order Code D
		Vs. Supply Voltage Vs. Aging / Year		$\pm 3$ $\pm 3$ $\pm 1$		ppm/V ppm ppm	First Year After first year
Operating Temperature	T		0° -40°		+70° +85°	°C	Order Code B Order Code G
Output		LVPECL LVDS LVCMOS					Order Code L Order Code D Order Code C
Supply Voltage	V <sub>cc</sub>		3.15 2.25	3.3 2.5	3.45 2.75	V	Order Code E Order Code G
Period Jitter RMS		155.52 MHz 311.04 MHz 622.08 MHz		2.5 2.5 4	3 3 6	ps	
Integrated Jitter RMS 12KHz to 20MHz		155.52MHz 311.04MHz 622.08MHz		0.25 0.18 0.09		ps	
Period Jitter Peak-to-Peak		155.52MHz 311.04MHz 622.08MHz		18 18 25	20 20 30	ps	

\* NOTE: Certain frequency above 500MHz (3.3V<sub>DD</sub>) and above 300MHz (2.5V<sub>DD</sub>) isn't available.  
Consult factory for availability.



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#### Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Current	I <sub>CC</sub>	38 – 100MHz			65	mA	PECL
		100 – 300MHz			80		
		300 – 640MHz			90		
		38 – 100MHz			45	mA	LVDS
		100 – 320MHz			60		
		320 – 640MHz			70		
		At 100MHz, load = 15pF		16	20	mA	CMOS
Load	50 Ohm to V <sub>DD</sub> -2V (PECL) 100 Ohm (LVDS)						
Output High Voltage	V <sub>OH</sub>	R <sub>L</sub> = 50 ohm to (V <sub>DD</sub> -2V) I <sub>OH</sub> = -8.5mA	2.4	V <sub>DD</sub> -1.025 1.4	1.6	V	PECL LVDS CMOS
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = -8.5mA	0.9	1.1	V <sub>DD</sub> -1.620 0.4	V	PECL LVDS CMOS
Output Differential Voltage	V <sub>OD</sub>		247	355	454	mV	LVDS
Output Drive Voltage	I <sub>OSD</sub>	V <sub>OL</sub> = 0.4V, V <sub>OH</sub> = 2.4V		8.5		mA	CMOS
Offset Voltage	V <sub>OS</sub>		1.125	1.2	1.375	V	LVDS
Rise / Fall Time	Tr/Tf	20% to 80%		0.25 0.3 1.2	0.45 0.7 1.6	ns	PECL LVDS CMOS
Duty Cycle		V <sub>DD</sub> – 1.3V @ 1.25V 50% V <sub>DD</sub>	45	50	55	%	PECL LVDS CMOS
Tristate	"1": Output Enable – Pin 1 may float 2.8V min (3.3V V <sub>DD</sub> ) or 2.25V min (2.5V V <sub>DD</sub> ) "0": Tristate – Pin 1 requires 0.4V max (3.3V or 2.5V V <sub>DD</sub> )						

#### Phase Noise Performance

Parameter	Output Type	Frequency Range (MHz)	Carrier Freq. (MHz)	10Hz	100Hz	1KHz	10 KHz	100 KHz	1 MHz	10 MHz
Phase Noise (dBc/Hz)	PECL LVDS	300 - 800	622.08	-55	-85	-110	-130	-137	-148	-150
	CMOS	120 – 320	155.52	-50	-82	-110	-128	-142	-148	-150
	PECL LVDS	120 – 320	155.52	-50	-82	-110	-128	-142	-148	-150
	CMOS	16 – 160	155.52	-65	-95	-122	-138	-142	-148	-149
	PECL LVDS	60 – 160	155.52	-65	-95	-122	-138	-142	-148	-149



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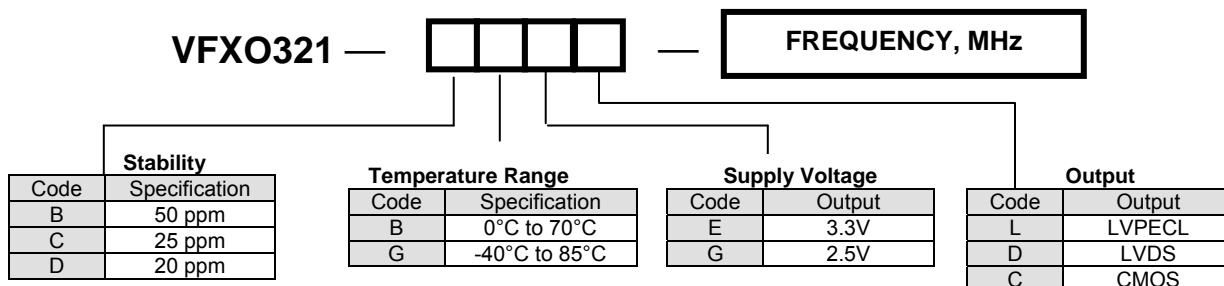
### 5x7mm SMD, LVPECL / LVDS / LVCMOS



### Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Lead Temperature		Soldering, 10s max			260	°C	
Storage Temperature	T <sub>s</sub>		-55		+125°	°C	
Junction Temperature	T <sub>j</sub>				+125°	°C	
ESD Protection		Input static discharge voltage protection			2	kV	
Supply Voltage	V <sub>DD</sub>				4.6	V	
Output Voltage	V <sub>O</sub>		V <sub>DD</sub> -0.5		V <sub>DD</sub> +0.5	V	

### How to Order



Note: DG combination not available at all frequencies. Consult factory.



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**Environmental and Mechanical Conditions**

Parameter	Specification
<b>Shock</b>	1000 Gs, 0.35ms, ½ sine wave, 3 shocks in each plane
<b>Humidity</b>	Resistant to 85 °R.H. at 85 °C
<b>Vibration</b>	10-2000 Hz of 0.06" d.a. or 20 Gs, whichever is less
<b>Leak</b>	MIL STD 883, Method 1014, Condition A1
<b>Case</b>	Ceramic with hermetic resistance-welded metal lid
<b>Pads</b>	Solderable gold over nickel
<b>Marking</b>	Epoxy ink or laser engraved
<b>Resistance to Solvents</b>	MIL STD 202, Method 215

**LVPECL, LVDS**

Pin #	Connection
1	Tristate
2	N/C
3	Case, GND
4	Output
5	Output
6	Supply Voltage

**LVCMOS**

Pin #	Connection
1	Tristate
2	N/C
3	Case, GND
4	Output
5*	N/C
6	Supply Voltage

\*For LVCMOS, Dual single ended outputs available – consult factory

