

P-channel enhancement mode MOS transistor

PHP125

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver, power management, synchronized rectifying, etc.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

DESCRIPTION

P-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

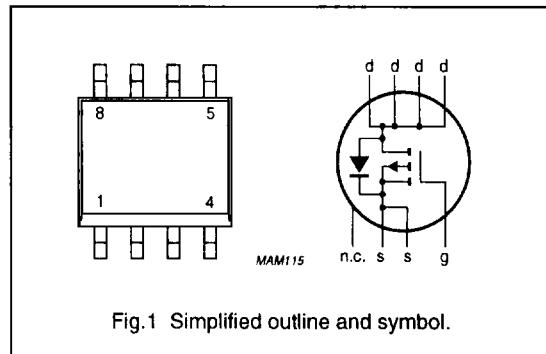


Fig. 1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		-	-30	V
V_{SD}	source-drain diode forward voltage	$I_S = -1.25 \text{ A}$	-	-1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	-	± 20	V
$V_{GS\text{th}}$	gate-source threshold voltage	$I_D = -1 \text{ mA}; V_{DS} = V_{GS}$	-1	-2.8	V
I_D	drain current (DC)		--	-2.3	A
$R_{DS\text{on}}$	drain-source on-state resistance	$I_D = -1 \text{ A}; V_{GS} = -10 \text{ V}$	-	0.25	Ω
P_{tot}	total power dissipation	up to $T_s = 80^\circ\text{C}$	-	2	W

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	-30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	± 20	V
I_D	drain current (DC)	$T_s \leq 80^\circ\text{C}$	–	-2.3	A
I_{DM}	peak drain current	note 1	–	-10	A
P_{tot}	total power dissipation	up to $T_s = 80^\circ\text{C}$	–	2	W
		up to $T_{amb} = 25^\circ\text{C}$; note 2	–	2	W
		up to $T_{amb} = 25^\circ\text{C}$; note 3	–	1.3	W
T_{stg}	storage temperature		-65	+150	$^\circ\text{C}$
T_j	operating junction temperature		–	150	$^\circ\text{C}$
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80^\circ\text{C}$	–	-1.25	A
I_{SM}	peak pulsed source current	note 1	–	-5	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Value based on PCB with a $R_{th\ a\rightarrow\ tp}$ (ambient to tie-point) of 27.5 K/W.
3. Value based on PCB with a $R_{th\ a\rightarrow\ tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	35	K/W

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CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = -10 \mu\text{A}$	-30	-	-	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}; I_D = -1 \text{ mA}$	-1	-	-2.8	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = -24 \text{ V}$	-	-	-100	nA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0$	-	-	± 100	nA
$I_{D(on)}$	on-state drain current	$V_{GS} = -10 \text{ V}; V_{DS} = -1 \text{ V}$	-2.3	-	-	A
		$V_{GS} = -4.5 \text{ V}; V_{DS} = -5 \text{ V}$	-1	-	-	A
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -0.5 \text{ A}$	-	0.33	0.4	Ω
		$V_{GS} = -10 \text{ V}; I_D = -1 \text{ A}$	-	0.22	0.25	Ω
$ y_{fs} $	forward transfer admittance	$V_{DS} = -20 \text{ V}; I_D = -1 \text{ A}$	1	2	-	S
C_{iss}	input capacitance	$V_{GS} = 0; V_{DS} = -20 \text{ V}; f = 1 \text{ MHz}$	-	250	-	pF
C_{oss}	output capacitance	$V_{GS} = 0; V_{DS} = -20 \text{ V}; f = 1 \text{ MHz}$	-	140	-	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0; V_{DS} = -20 \text{ V}; f = 1 \text{ MHz}$	-	50	-	pF
Q_g	total gate charge	$V_{GS} = -10 \text{ V}; V_{DS} = -15 \text{ V}; I_D = -2.3 \text{ A}$	-	10	25	nC
Q_{gs}	gate-source charge	$V_{GS} = -10 \text{ V}; V_{DS} = -15 \text{ V}; I_D = -2.3 \text{ A}$	-	1	-	nC
Q_{gd}	gate-drain charge	$V_{GS} = -10 \text{ V}; V_{DS} = -15 \text{ V}; I_D = -2.3 \text{ A}$	-	3	-	nC
t_{on}	turn-on time	$V_{GS} = 0 \text{ to } -10 \text{ V}; V_{DD} = -20 \text{ V}; I_D = -1 \text{ A}; R_L = 20 \Omega$	-	20	80	ns
t_{off}	turn-off time	$V_{GS} = -10 \text{ to } 0 \text{ V}; V_{DD} = -20 \text{ V}; I_D = -1 \text{ A}; R_L = 20 \Omega$	-	50	140	ns
Source-drain diode						
V_{SD}	source drain diode forward voltage	$V_{GS} = 0; I_S = -1.25 \text{ A}$	-	-	-1.6	V
t_{rr}	reverse recovery time	$I_S = -1.25 \text{ A}; di/dt = 100 \text{ A}/\mu\text{s}$	-	150	200	ns