

P3C230 ULTRA HIGH-SPEED 64K x 9 CMOS STATIC RAM



FEATURES

- Full CMOS Design
- Fast Access Times: 13/15/17/20ns (max.)
- Dual Chip Enables for Depth Expansion
- Output Enable for Bank Switching
- Supports Processor Speeds to 75MHz
- Standby Power Mode when disabled
- Single 3.3V ± 0.3V Power Supply
- Common Data I/O
- TTL-Compatible Inputs & Outputs
- Three-State Outputs
- 44-pin PLCC Package



DESCRIPTION

The P3C230 is a 589,824-bit ultra high-speed CMOS static RAM organized as 64Kx9 for general-purpose high-density low-power applications. Dual complementary chip enable controls (\overline{CE}_1 , CE_2) facilitate easy depth expansion to 128K with no decoding penalty. An output enable (\overline{OE}) control permits fast bus turnaround and switching between several memory banks.

Access times as fast as 13ns are available permitting processor speeds up to 75MHz. A single 3.3V ± 0.3V tolerance power supply is needed. Power dissipation is 600mW (max.) when active and only 120mW when deselected using either chip enable.

The P3C230 is ideally suited for use at 13ns as secondary cache with the 3.3V MIPS PR4000S at 75MHz. Twenty

units comprise a 1MByte cache (including tag and check bits), which can be used with the PR4000S in the joint- or split-cache modes. Total power dissipation in the cache is under 5W (max.) assuming a 25% activity cycle.

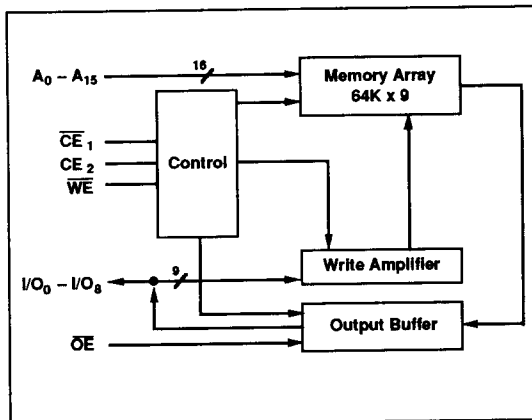
The P3C230 can be used as primary cache (i386) and secondary cache (i486) with the ix86 processor family at 3.3V, in lap-top applications. Only four units are required for a 256KByte cache in a 32-bit bus system.

The P3C230 is manufactured using PACE III technology and is available in a 44-pin PLCC package, providing high board-level density.

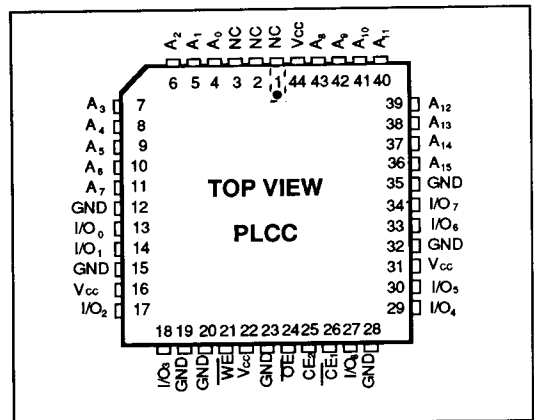
6



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Means Quality, Service and Speed

©1992 Performance Semiconductor Corporation

TRUTH TABLE

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	MODE	OUTPUT
H	X	X	X	Deselected Cycle	High Z
X	L	X	X		
L	H	H	H	Output Disabled	High Z
L	H	H	L	Read Cycle	Data Out
L	H	L	X	Write Cycle	Data In

APPLICATION EXAMPLE: PR4000 Secondary Cache

(1MByte configured as split instruction-data caches of 512KBytes each).

