

TISP4015H1BJ, TISP4020H1BJ, TISP4040H1BJ VERY LOW VOLTAGE BIDIRECTIONAL OVERVOLTAGE PROTECTORS

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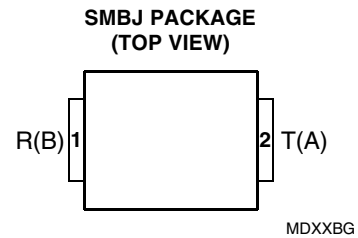
SELV TELECOMMUNICATION LINE OVERVOLTAGE PROTECTION

- **Digital Line Signal Level Protection**
 - ISDN
 - xDSL
- **Safety Extra Low Voltage, SELV, values**

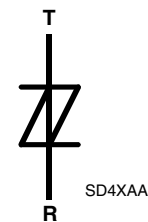
DEVICE	V _{DRM} V	V _(BO) V
'4015	± 5	± 15
'4020	± 8	± 20
'4040	± 25	± 40

- **Low Capacitance**
 - 50 pF for '4040 through to 85 pF for '4015
- **High Current "H" Series for ITU-T K20, FCC Part 68 and GR-1089-CORE**

WAVE SHAPE	STANDARD	I _{TSP} A
2/10 μs	GR-1089-CORE	500
8/20 μs	IEC 61000-4-5	400
10/160 μs	FCC Part 68	200
10/700 μs	ITU-T K20/21 FCC Part 68	150
10/560 μs	FCC Part 68	120
10/1000 μs	GR-1089-CORE	100



device symbol



Terminals T and R correspond to the alternative line designators of A and B

- **100 A Functional Replacements for:**

DEVICE TYPE	FUNCTIONAL REPLACEMENT
P0080Sx (February 1998 issue)	TISP4015H1BJ
P0080Sx	TISP4020H1BJ
P0300Sx	TISP4040H1BJ
SMP100-8, SMP75-8 (See Note 1)	TISP4020H1BJ

NOTE 1. The TISP4020H1BJ has a higher a.c. V_(BO) than SMP75-8, but has the same impulse V_(BO).

description

These devices are designed to limit overvoltages on digital telecommunication lines. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line. A single device provides 2-point protection and is typically used for the protection of transformer windings and low voltage electronics.

HOW TO ORDER

DEVICE	PACKAGE	CARRIER	ORDER AS
TISP40xxH1	BJ (J-Bend DO-214AA/SMB)	Embossed Tape Reeled	TISP40xxH1BJR
TISP40xxH1	BJ (J-Bend DO-214AA/SMB)	Bulk Pack	TISP40xxH1BJ

Insert xx value corresponding to protection voltages of 15 V, 20 V and 40 V

The protector consists of a symmetrical voltage-triggered bidirectional thyristor. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on-state condition. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The device switches off when the diverted current falls below the holding current value.

ADVANCE INFORMATION

Information relates to new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.



A Bourns Company

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absolute maximum ratings, $T_A = 25\text{ }^\circ\text{C}$ (unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage	V_{DRM}	± 5	V
		± 8	
		± 25	
Non-repetitive peak on-state pulse current (see Notes 2 and 3) 2/10 μs (Telcordia GR-1089-CORE, 2/10 μs voltage wave shape) 8/20 μs (IEC 61000-4-5, combination wave generator, 1.2/50 voltage, 8/20 current) 10/160 μs (FCC Part 68, 10/160 μs voltage wave shape) 5/310 μs (ITU-T K20/21, 10/700 μs voltage wave shape) 5/320 μs (FCC Part 68, 9/720 μs voltage wave shape) 10/560 μs (FCC Part 68, 10/560 μs voltage wave shape) 10/1000 μs (Telcordia GR-1089-CORE, 10/1000 μs voltage wave shape)	I_{TSP}	± 500	A
		± 400	
		± 200	
		± 150	
		± 150	
		± 120	
		± 100	
Non-repetitive peak on-state current (see Notes 2 and 3) 20 ms (50 Hz) full sine wave 16.7 ms (60 Hz) full sine wave 0.2 s 50/60 Hz a.c. 2 s 50/60 Hz a.c. 1000 s 50 Hz/60 Hz a.c.	I_{TSM}	55	A
		60	
		25	
		12	
		2	
Initial rate of rise of current (2/10 waveshape)	di/dt	300	A/ μs
Maximum junction temperature	T_{JM}	150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-65 to +150	$^\circ\text{C}$

NOTES: 2. Initially the device must be in thermal equilibrium with $T_J = 25\text{ }^\circ\text{C}$.
 3. The surge may be repeated after the device returns to its initial conditions.

electrical characteristics for the R and T terminals, $T_A = 25\text{ }^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRM} Repetitive peak off-state current	$V_D = V_{\text{DRM}}$			± 5	μA
$V_{(\text{BO})}$ Breakover voltage	$di/dt = \pm 0.8\text{ A/ms}$			± 15 ± 20 ± 40	V
$V_{(\text{BO})}$ Impulse breakover voltage	$dv/dt \leq \pm 1000\text{ V}/\mu\text{s}$, Linear voltage ramp, Maximum ramp value = $\pm 500\text{ V}$ $di/dt = \pm 20\text{ A}/\mu\text{s}$, Linear current ramp, Maximum ramp value = $\pm 10\text{ A}$			± 20 ± 25 ± 45	V
$I_{(\text{BO})}$ Breakover current	$di/dt = \pm 0.8\text{ A/ms}$			± 0.8	A
I_D Off-state current	$V_D = \pm 4\text{ V}$ $V_D = \pm 6\text{ V}$ $V_D = \pm 22\text{ V}$			± 2	μA
I_H Holding current	$I_T = \pm 5\text{ A}$, $di/dt = \pm 30\text{ mA/ms}$	± 50			mA

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electrical characteristics for the R and T terminals, $T_A = 25\text{ }^\circ\text{C}$ (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{off} Off-state capacitance	f = 1 MHz, $V_d = 1\text{ V rms}$, $V_D = 0$	'4015	95		pF
		'4020	85		
		'4040	60		
	f = 1 MHz, $V_d = 1\text{ V rms}$, $V_D = 1\text{ V}$	'4015	90		
		'4020	80		
		'4040	55		
	f = 1 MHz, $V_d = 1\text{ V rms}$, $V_D = 2\text{ V}$	'4015	85		
		'4020	75		
		'4040	50		

thermal characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, $T_A = 25\text{ }^\circ\text{C}$, (see Note 4)			115	$^\circ\text{C/W}$
	265 mm x 210 mm populated line card, 4-layer PCB, $I_T = I_{TSM(1000)}$, $T_A = 25\text{ }^\circ\text{C}$		52		

NOTE 4: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

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PARAMETER MEASUREMENT INFORMATION

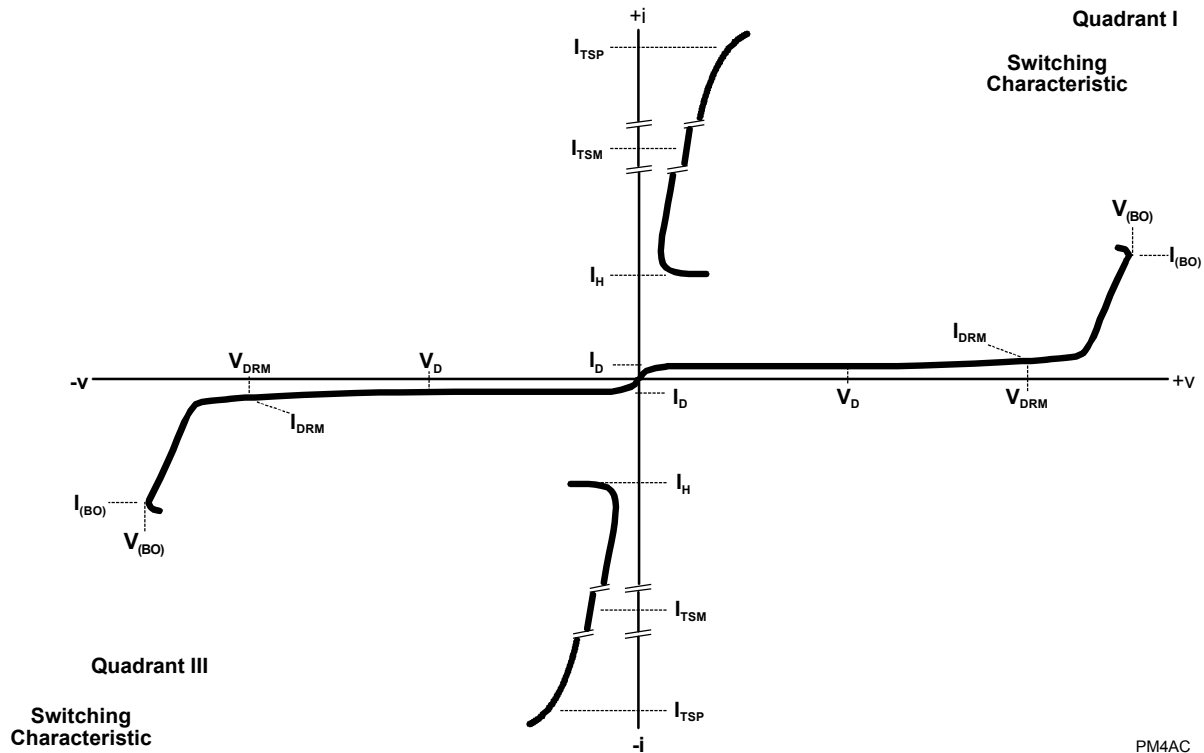


Figure 1. VOLTAGE-CURRENT CHARACTERISTIC FOR T AND R TERMINALS
ALL MEASUREMENTS ARE REFERENCED TO THE R TERMINAL

APPLICATIONS INFORMATION

transformer protection

The inductance of a transformer winding reduces considerably when the magnetic core material saturates. Saturation occurs when the magnetising current through the winding inductance exceeds a certain value. It should be noted that this is a different current to the transformed current component from primary to secondary. The standard inductance-current relationship is:

$$E = -\left(L \frac{di}{dt}\right)$$

where:

L = unsaturated inductance value in H

di = current change in A

dt = time period in s for current change di

E = winding voltage in V

Re-arranging this equation and working large Δ changes to saturation gives the useful circuit relationship of:

$$E \times \Delta t = L \times \Delta i$$

A transformer winding volt-second value for saturation gives the designer an idea of circuit operation under overvoltage conditions. The volt-second value is not normally quoted, but most manufacturers should provide

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it on request. A 50 V μ s winding will support rectangular voltage pulses of 50 V for 1 μ s, 25 V for 2 μ s, 1 V for 50 μ s and so on. Once the transformer saturates, primary to secondary coupling will be lost and the winding resistance, RW, shunts the overvoltage protector, Th1, see Figure 2. This saturated condition is a concern for long duration impulses and a.c. fault conditions because the current capability of the winding wire may be exceeded. For example, if the on-state voltage of the protector is 1 V and the winding resistance is 0.2 Ω , the winding would bypass a current of $1/0.2 = 5$ A, even through the protector was in the low voltage condition.



Figure 2. TRANSFORMER SATURATION

Figure 3 shows a generic protection arrangement. Resistors R1 and R2, together with the overcurrent protection, prevent excessive winding current flow under a.c. conditions. Alternatively, a split winding could be used with a single resistor connecting the windings. This resistor could be by-passed by a small capacitor to reduce signal attenuation.

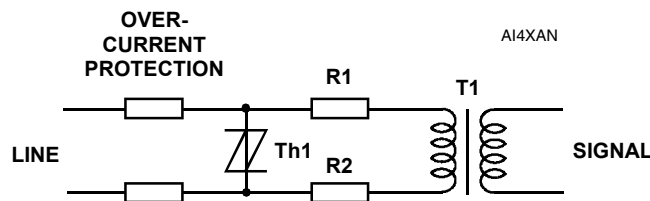


Figure 3. TRANSFORMER WINDING PROTECTION

Overcurrent protection upstream from the overvoltage protector can be fuse, PTC or thick film resistor based. For very high frequency circuits, fuse inductance due to spiral wound elements may need to be evaluated.

TISP[®] voltage selection

Normally the working voltage value of the protector, V_{DRM} , would be chosen to be just greater than the peak signal amplitude over the equipment temperature range. This would give the lowest possible protection voltage, $V_{(BO)}$. This would minimise the peak voltage applied to the transformer winding and increase the time to core saturation.

In high frequency circuits there are two further considerations. Low voltage protectors have a higher capacitance than high voltage protectors. So a higher voltage protector might be chosen specifically to reduce the protector capacitive effects on the signal.

Low energy short duration spikes will be clipped by the protector. This will extend the spike duration and the data loss time. A higher protector voltage will reduce the data loss time. Generally this will not be a significant factor for inter-conductor protection.

However, clipping is significant for protection to ground, where there is continuous low-level a.c. common mode induction. In some cases the induced a.c. voltage can be over 10 V. Repetitive clipping at the induced a.c. peaks by the protector would cause severe data corruption. The expected a.c. voltage induced should be added to the maximum signal level for setting the protector V_{DRM} value.

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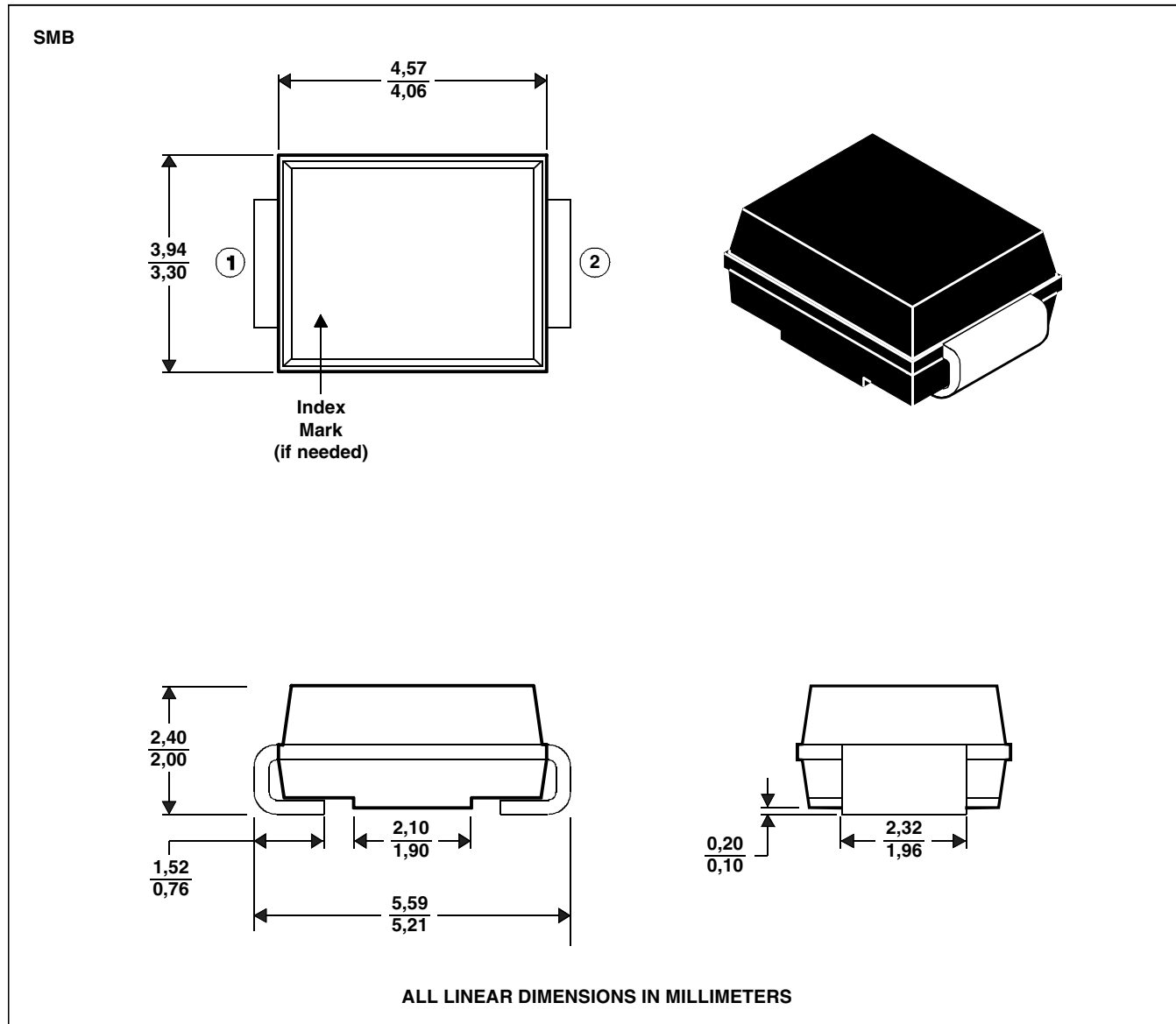
MECHANICAL DATA

SMBJ (DO-214AA)

plastic surface mount diode package

This surface mount package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

ADVANCE INFORMATION



MDXXBHA

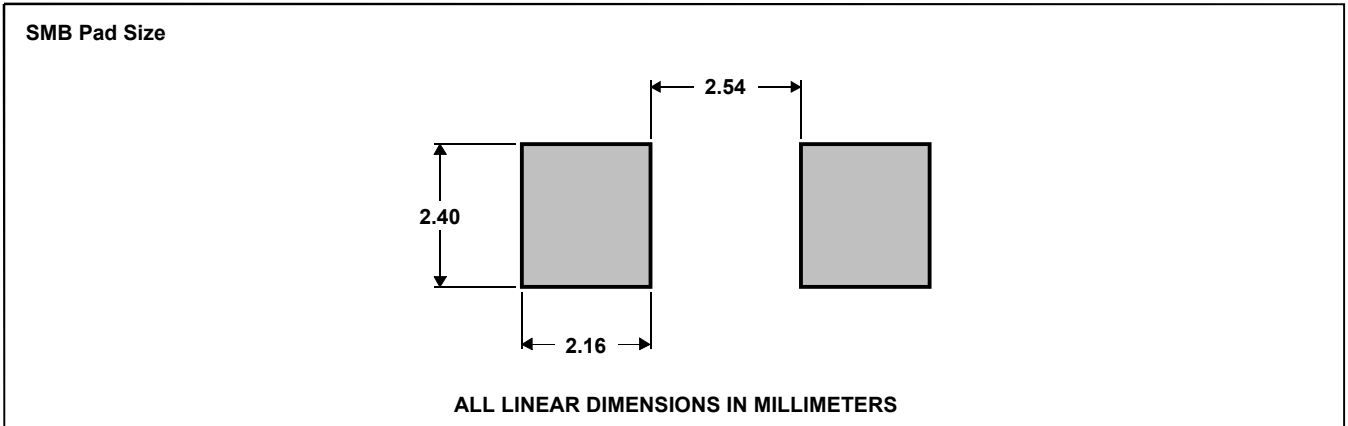
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MECHANICAL DATA

recommended printed wiring footprint.



MDXXBI

device symbolization

Devices are coded as below. As the device parameters are symmetrical, terminal 1 is not identified.

DEVICE	SYMOBLIZATION
TISP4015H1BJ	4015H1
TISP4020H1BJ	4020H1
TISP4040H1BJ	4040H1

carrier information

Devices are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer, devices will be shipped in the most practical carrier. For production quantities the carrier will be embossed tape reel pack. Evaluation quantities may be shipped in bulk pack or embossed tape.

CARRIER	STANDARD QUANTITY
Embossed Tape Reeled	3 000
Bulk Pack	2 000

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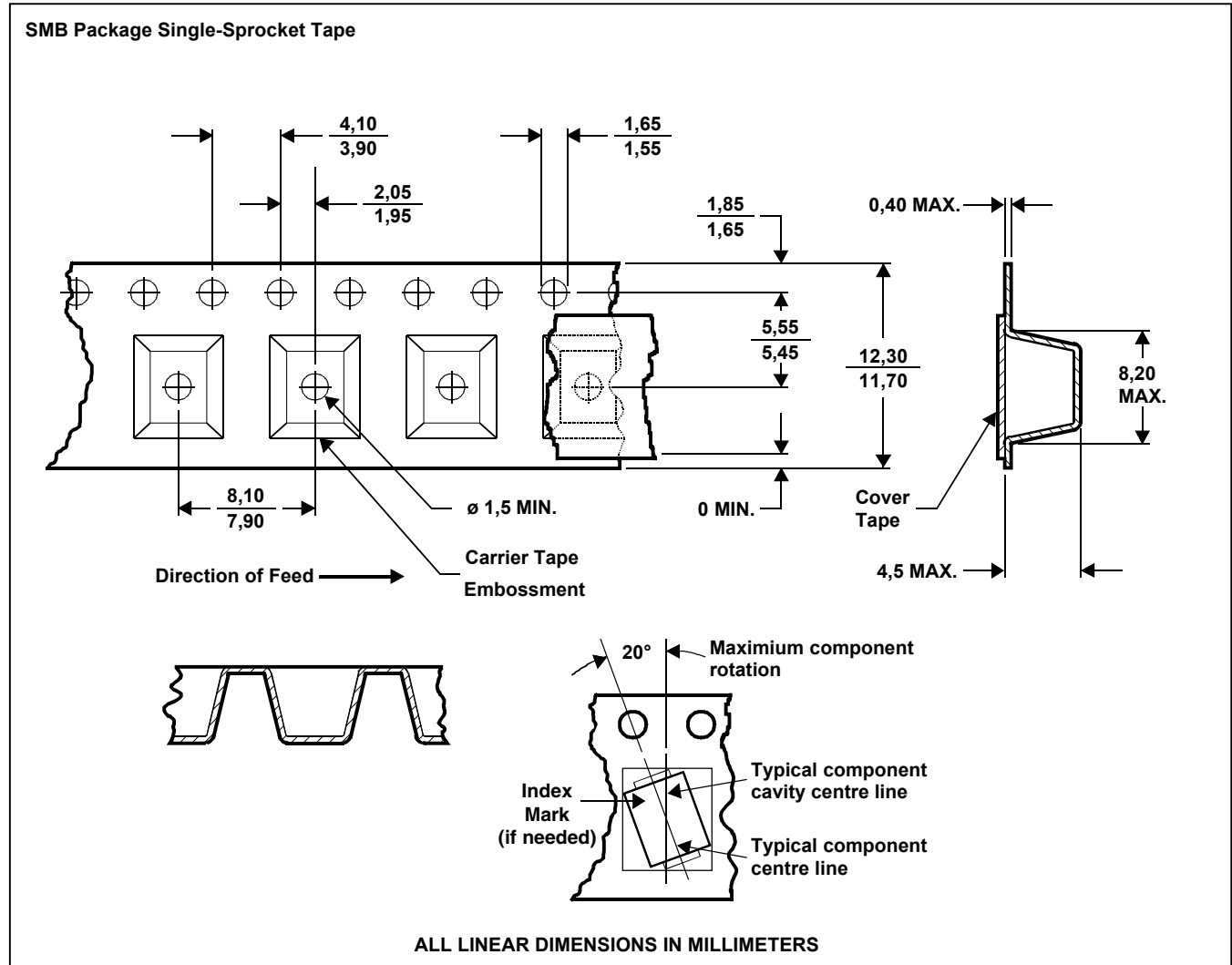


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MECHANICAL DATA

tape dimensions



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NOTES: A. The clearance between the component and the cavity must be within 0,05 mm MIN. to 0,65 mm MAX. so that the component cannot rotate more than 20° within the determined cavity.

MDXXBJ

B. Taped devices are supplied on a reel of the following dimensions:-

Reel diameter: 330 ±3,0 mm
 Reel hub diameter: 75 mm MIN.
 Reel axial hole: 13,0 ±0,5 mm

C. 3000 devices are on a reel.

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