

SPANSION™ MCP

Data Sheet



September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

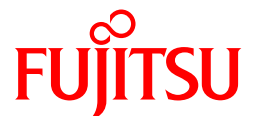
There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.



Stacked MCP (Multi-Chip Package) FLASH MEMORY & SRAM
CMOS

16M (×8/×16) FLASH MEMORY & 2M (×8/×16) STATIC RAM

MB84VD2108XEM-70/MB84VD2109XEM-70

■ FEATURES

- Power Supply Voltage of 2.7 V to 3.3 V
- High Performance
70 ns maximum access time (Flash)
70 ns maximum access time (SRAM)
- Operating Temperature
-40 °C to +85 °C
- Package 56-ball BGA

(Continued)

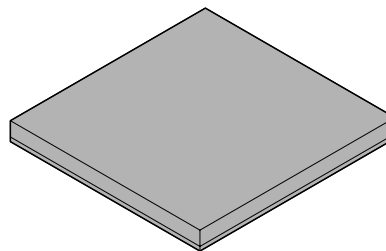
■ PRODUCT LINE UP

| Part No. | MB84VD2108XEM/MB84VD2109XEM | |
|---|--|--|
| Supply Voltage(V) | $V_{ccf} = 3.0 \text{ V} \begin{smallmatrix} +0.3 \text{ V} \\ -0.3 \text{ V} \end{smallmatrix}$ | $V_{ccs} = 3.0 \text{ V} \begin{smallmatrix} +0.3 \text{ V} \\ -0.3 \text{ V} \end{smallmatrix}$ |
| Max Address Access Time (ns) | 70 | 70 |
| Max $\overline{\text{CE}}$ Access Time (ns) | 70 | 70 |
| Max $\overline{\text{OE}}$ Access Time (ns) | 30 | 35 |

Note: Both V_{ccf} and V_{ccs} must be in recommended operation range when either part is being accessed.

■ PACKAGE

56-ball plastic BGA



(BGA-56P-M02)

MB84VD2108XEM/2109XEM-70

(Continued)

• FLASH MEMORY

• Simultaneous Read/Write Operations (Dual Bank)

Multiple devices available with different bank sizes (Please refer to ORDERING INFORMATION)

Host system can program or erase in one bank, then immediately and simultaneously read from the other bank

Zero latency between read and write operations

Read-while-erase

Read-while-program

• Minimum 100,000 Write/Erase Cycles

• Sector Erase Architecture

Eight 4 K words and thirty one 32 K words.

Any combination of sectors can be concurrently erased. Also supports full chip erase.

• Boot Code Sector Architecture

MB84VD2108XEM: Top sector

MB84VD2109XEM: Bottom sector

• Embedded Erase™* Algorithms

Automatically pre-programs and erases the chip or any sector

• Embedded Program™* Algorithms

Automatically writes and verifies data at specified address

• Data Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion

• Ready-Busy Output (RY/BY)

Hardware method for detection of program or erase cycle completion

• Automatic Sleep Mode

When addresses remain stable, automatically switch themselves to low power mode.

• Low V_{CC} Write Inhibit ≤ 2.5 V

• HiddenROM Region

64K byte of HiddenROM, accessible through a new “HiddenROM Enable” command sequence

Factory serialized and protected to provide a secure electronic serial number (ESN)

• WP/ACC Input Pin

At V_{IL}, allows protection of boot sectors, regardless of sector protection/unprotection status

(MB84VD2108XEM:SA37,SA38 MB84VD2109XEM:SA0,SA1)

At V_{IH}, allows removal of boot sector protection

At V_{ACC}, program time will reduce by 40%.

• Erase Suspend/Resume

Suspends the erase operation to allow a read in another sector within the same device

• Please refer to “MBM29DL16XTE/BE” Datasheet in Detailed Function

* : Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

• SRAM

• Power Dissipation

Operating : 40 mA Max

Standby : 7 μA Max

• Power Down Features using $\overline{CE1}$ s and CE2s

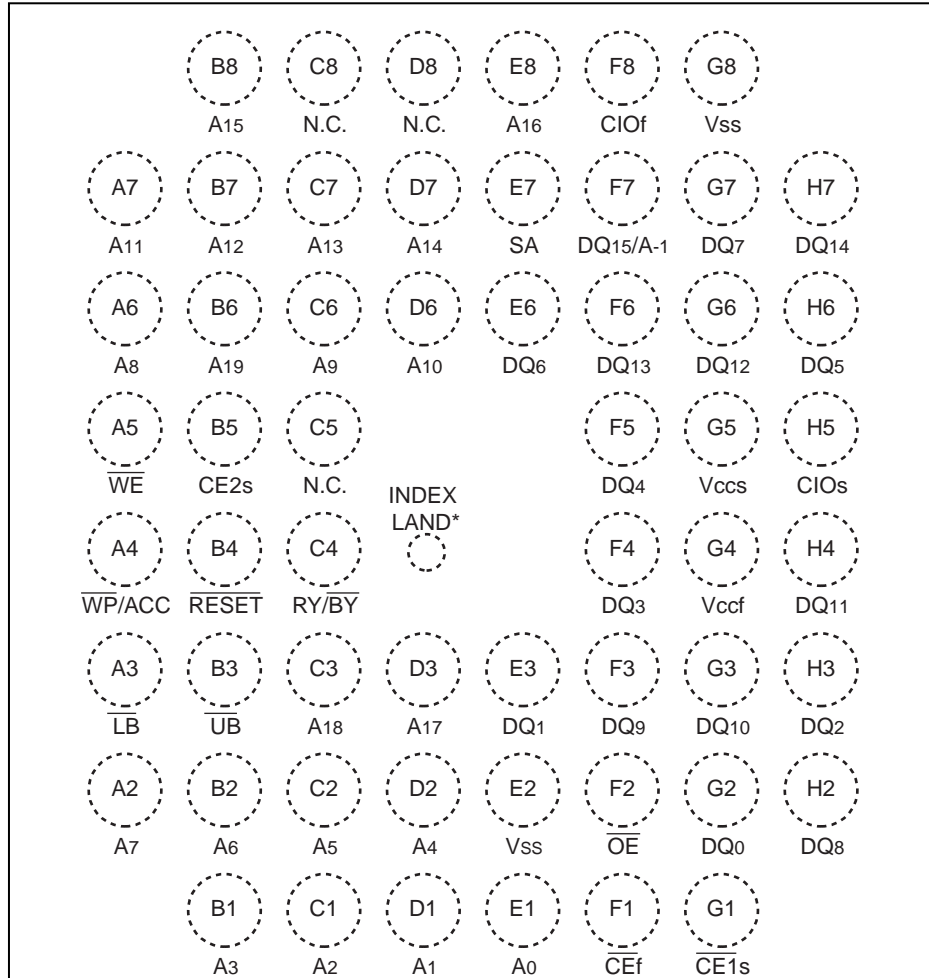
• Data Retention Supply Voltage: 1.5 V to 3.3 V

• $\overline{CE1}$ s and CE2s Chip Select

• Byte Data Control: \overline{LB} (DQ₇ to DQ₀), \overline{UB} (DQ₁₅ to DQ₈)

■ PIN ASSIGNMENT

(Top View)
Marking side



* : There is no solder ball. This land should be open electrically.

(BGA-56P-M02)

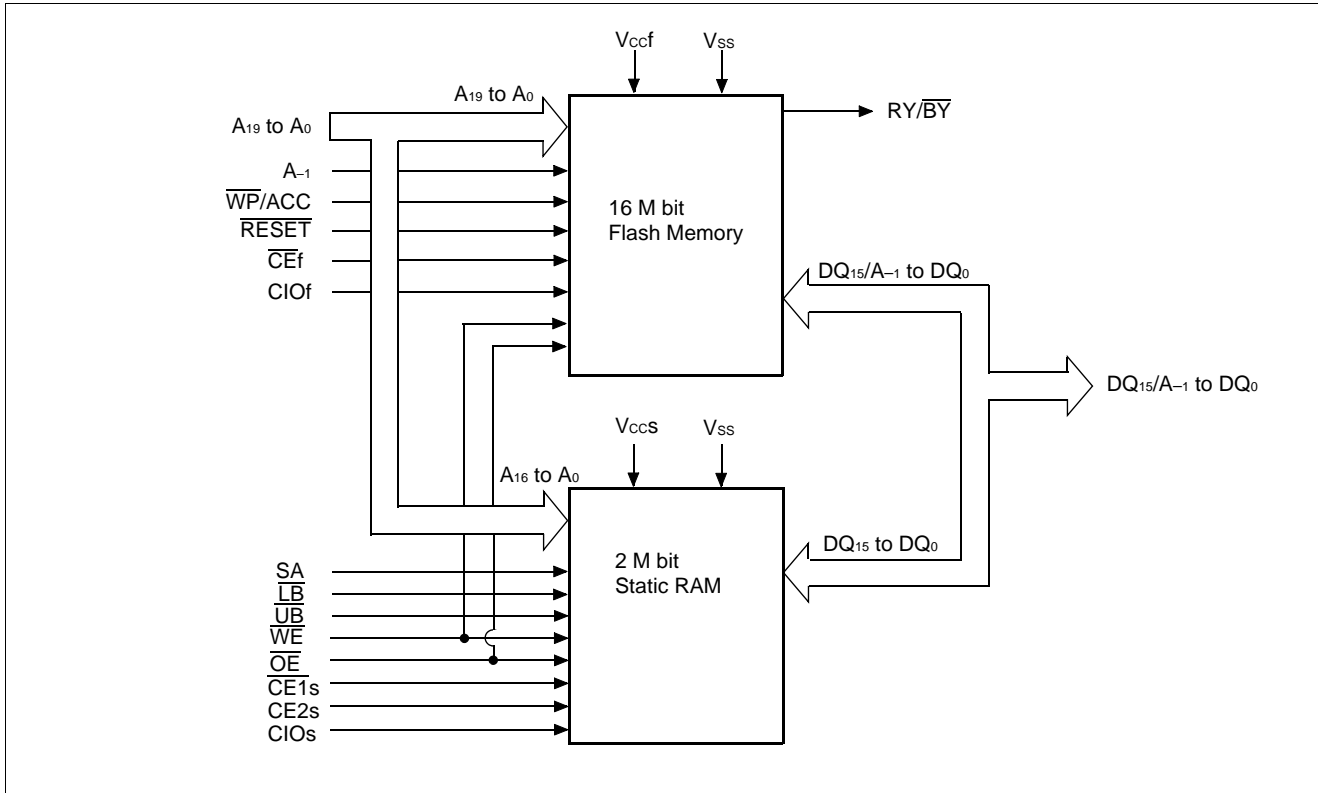
MB84VD2108XEM/2109XEM-70

■ PIN DESCRIPTION

| Pin Name | Function | Input/Output |
|--|---|--------------|
| A ₁₆ to A ₀ | Address Inputs (Common) | I |
| A ₁₉ to A ₁₇ , A ₋₁ | Address Input (Flash) | I |
| SA | Address Input (SRAM) | I |
| DQ ₁₅ to DQ ₀ | Data Inputs / Outputs (Common) | I/O |
| $\overline{\text{CE}}_f$ | Chip Enable (Flash) | I |
| $\overline{\text{CE}}_{1s}$ | Chip Enable (SRAM) | I |
| CE _{2s} | Chip Enable (SRAM) | I |
| $\overline{\text{OE}}$ | Output Enable (Common) | I |
| $\overline{\text{WE}}$ | Write Enable (Common) | I |
| RY/ $\overline{\text{BY}}$ | Ready/Busy Outputs (Flash) Open Drain Output | O |
| $\overline{\text{UB}}$ | Upper Byte Control (SRAM) | I |
| $\overline{\text{LB}}$ | Lower Byte Control (SRAM) | I |
| CIO _f | I/O Configuration (Flash) CIO _f =V _{ccf} is Word mode (×16), CIO _f =V _{ss} is Byte mode (× 8) | I |
| CIO _s | I/O Configuration (SRAM) CIO _s =V _{ccs} is Word mode (×16), CIO _s =V _{ss} is Byte mode (× 8) | I |
| $\overline{\text{RESET}}$ | Hardware Reset Pin / Sector Protection Un- lock (Flash) | I |
| $\overline{\text{WP/ACC}}$ | Write Protect / Acceleration (Flash) | I |
| N.C. | No Internal Connection | — |
| V _{ss} | Device Ground (Common) | Power |
| V _{ccf} | Device Power Supply (Flash) | Power |
| V _{ccs} | Device Power Supply (SRAM) | Power |

MB84VD2108XEM/2109XEM-70

■ BLOCK DIAGRAM



MB84VD2108XEM/2109XEM-70

■ DEVICE BUS OPERATIONS

User Bus Operations Table (Flash = Word mode; CIO_f = V_{ccf}, SRAM = Word mode; CIO_s = V_{ccs})

| Operation *1, *3 | \overline{CEf} | $\overline{CE1s}$ | CE2s | \overline{OE} | \overline{WE} | SA | \overline{LB} | \overline{UB} | DQ ₇ to DQ ₀ | DQ ₁₅ to DQ ₈ | \overline{RESET} | $\overline{WP/ACC}$ *5 |
|--|------------------|-------------------|------|-----------------|-----------------|----|-----------------|-----------------|------------------------------------|-------------------------------------|--------------------|------------------------|
| Full Standby | H | H | X | X | X | X | X | X | High-Z | High-Z | H | X |
| | | X | L | | | | | | | | | |
| Output Disable | H | L | H | H | H | X | X | X | High-Z | High-Z | H | X |
| | | | | X | X | X | H | H | High-Z | High-Z | | |
| | L | H | X | H | H | X | X | X | High-Z | High-Z | | |
| | | X | L | | | | | | | | | |
| Read from Flash *2 | L | H | X | L | H | X | X | X | D _{OUT} | D _{OUT} | H | X |
| | | | X | | | | | | L | | | |
| Write to Flash | L | H | X | H | L | X | X | X | D _{IN} | D _{IN} | H | X |
| | | | X | | | | | | L | | | |
| Read from SRAM | H | L | H | L | H | X | L | L | D _{OUT} | D _{OUT} | H | X |
| | | | | | | | H | L | High-Z | D _{OUT} | | |
| | | | | | | | L | H | D _{OUT} | High-Z | | |
| Write to SRAM | H | L | H | X | L | X | L | L | D _{IN} | D _{IN} | H | X |
| | | | | | | | H | L | High-Z | D _{IN} | | |
| | | | | | | | L | H | D _{IN} | High-Z | | |
| Temporary Sector Group Unprotection *4 | X | X | X | X | X | X | X | X | X | X | V _{ID} | X |
| Flash Hardware Reset | X | H | X | X | X | X | X | X | High-Z | High-Z | L | X |
| | | X | L | | | | | | | | | |
| Boot Block Sector Write Protection | X | X | X | X | X | X | X | X | X | X | X | L |

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : \overline{WE} can be V_{IL} if \overline{OE} is V_{IL}, \overline{OE} at V_{IH} initiates the write operations.

*3 : Do not apply $\overline{CEf} = V_{IL}$, $\overline{CE1s} = V_{IL}$ and CE2s = V_{IH} at a time.

*4 : It is also used for the extended sector group protections.

*5 : $\overline{WP/ACC} = V_{IL}$; protection of boot sectors.

$\overline{WP/ACC} = V_{IH}$; removal of boot sectors protection.

$\overline{WP/ACC} = V_{ACC}$ (9 V); Program time will reduce by 40%.

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User Bus Operations Table (Flash = Word mode; CIO_f = V_{ccf}, SRAM = Byte mode; CIO_s = V_{ss})

| Operation *1, *3 | \overline{CEf} | $\overline{CE1s}$ | CE2s | \overline{OE} | \overline{WE} | SA | \overline{LB} | \overline{UB} | DQ ₇ to DQ ₀ | DQ ₁₅ to DQ ₈ | \overline{RESET} | $\overline{WP/ACC}$ *5 |
|--|------------------|-------------------|------|-----------------|-----------------|----|-----------------|-----------------|------------------------------------|-------------------------------------|--------------------|------------------------|
| Full Standby | H | H | X | X | X | X | X | X | High-Z | High-Z | H | X |
| | | X | L | | | | | | | | | |
| Output Disable | H | L | H | H | H | X | X | X | High-Z | High-Z | H | X |
| | | | | X | X | X | H | H | High-Z | High-Z | | |
| | L | H | X | H | H | X | X | X | High-Z | High-Z | | |
| X | | | | | | | | | | | L | |
| Read from Flash *2 | L | H | X | L | H | X | X | X | D _{OUT} | D _{OUT} | H | X |
| | | X | L | | | | | | | | | |
| Write to Flash | L | H | X | H | L | X | X | X | D _{IN} | D _{IN} | H | X |
| | | X | L | | | | | | | | | |
| Read from SRAM | H | L | H | L | H | SA | X | X | D _{OUT} | High-Z | H | X |
| Write to SRAM | H | L | H | X | L | SA | X | X | D _{IN} | High-Z | H | X |
| Temporary Sector Group Unprotection *4 | X | X | X | X | X | X | X | X | X | X | V _{ID} | X |
| Flash Hardware Reset | X | H | X | X | X | X | X | X | High-Z | High-Z | L | X |
| | | X | L | | | | | | | | | |
| Boot Block Sector Write Protection | X | X | X | X | X | X | X | X | X | X | X | L |

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : \overline{WE} can be V_{IL} if \overline{OE} is V_{IL}, \overline{OE} at V_{IH} initiates the write operations.

*3 : Do not apply \overline{CEf} = V_{IL}, $\overline{CE1s}$ = V_{IL} and CE2s = V_{IH} at a time.

*4 : It is also used for the extended sector group protections.

*5 : $\overline{WP/ACC}$ = V_{IL}; protection of boot sectors.

$\overline{WP/ACC}$ = V_{IH}; removal of boot sectors protection.

$\overline{WP/ACC}$ = V_{ACC} (9 V); Program time will reduce by 40%.

MB84VD2108XEM/2109XEM-70

User Bus Operations Table (Flash = Byte mode; CIO_f = V_{SS}, SRAM = Byte mode; CIO_s = V_{SS})

| Operation *1,*3 | \overline{CE}_f | \overline{CE}_{1s} | CE_{2s} | DQ _{15/A-1} | \overline{OE} | \overline{WE} | SA | \overline{LB} | \overline{UB} | DQ ₇ to DQ ₀ | DQ ₁₄ to DQ ₈ | \overline{RESET} | $\overline{WP/ACC}$ *5 |
|--|-------------------|----------------------|-----------|----------------------|-----------------|-----------------|----|-----------------|-----------------|------------------------------------|-------------------------------------|--------------------|------------------------|
| Full Standby | H | H | X | X | X | X | X | X | X | High-Z | High-Z | H | X |
| | | X | L | | | | | | | | | | |
| Output Disable | H | L | H | X | H | H | X | X | X | High-Z | High-Z | H | X |
| | | | | X | X | X | H | H | High-Z | High-Z | | | |
| | L | H | X | A-1 | H | H | X | X | X | High-Z | High-Z | | |
| | | | | | | | | | | | | | |
| Read from Flash *2 | L | H | X | A-1 | L | H | X | X | X | D _{OUT} | High-Z | H | X |
| | | X | L | | | | | | | | | | |
| Write to Flash | L | H | X | A-1 | H | L | X | X | X | D _{IN} | High-Z | H | X |
| | | X | L | | | | | | | | | | |
| Read from SRAM | H | L | H | X | L | H | SA | X | X | D _{OUT} | High-Z | H | X |
| Write to SRAM | H | L | H | X | X | L | SA | X | X | D _{IN} | High-Z | H | X |
| Temporary Sector Group Unprotection *4 | X | X | X | X | X | X | X | X | X | X | X | V _{ID} | X |
| Flash Hardware Reset | X | H | X | X | X | X | X | X | X | High-Z | High-Z | L | X |
| | | X | L | | | | | | | | | | |
| Boot Block Sector Write Protection | X | X | X | X | X | X | X | X | X | X | X | X | L |

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : \overline{WE} can be V_{IL} if \overline{OE} is V_{IL}, \overline{OE} at V_{IH} initiates the write operations.

*3 : Do not apply $\overline{CE}_f = V_{IL}$, $\overline{CE}_{1s} = V_{IL}$ and $CE_{2s} = V_{IH}$ at a time.

*4 : It is also used for the extended sector group protections.

*5 : $\overline{WP/ACC} = V_{IL}$; protection of boot sectors.

$\overline{WP/ACC} = V_{IH}$; removal of boot sectors protection.

$\overline{WP/ACC} = V_{ACC}$ (9 V); Program time will reduce by 40%.

■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|--|-------------------------------------|--------|-----------------------|------|
| | | Min | Max | |
| Storage Temperature | T _{stg} | -55 | +125 | °C |
| Ambient Temperature with Power Applied | T _A | -40 | +85 | °C |
| Voltage with Respect to Ground All pins except $\overline{\text{RESET}}$, $\overline{\text{WP/ACC}}$ *1 | V _{IN} , V _{OUT} | -0.3 | V _{ccf} +0.4 | V |
| | | | V _{ccs} +0.4 | V |
| V _{ccf} /V _{ccs} Supply *1 | V _{ccf} , V _{ccs} | -0.3 | +4.0 | V |
| $\overline{\text{RESET}}$ *2 | V _{IN} | -0.5 | + 13.0 | V |
| $\overline{\text{WP/ACC}}$ *3 | V _{IN} | -0.5 | +10.5 | V |

*1 : Minimum DC voltage on input or I/O pins is -0.3 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{ccf}+0.4 V or V_{ccs}+0.4 V. During voltage transitions, input or I/O pins may overshoot to V_{ccf}+2.0 V or V_{ccs}+2.0 V for periods of up to 20 ns.

*2 : Minimum DC input voltage on $\overline{\text{RESET}}$ pin is -0.5 V. During voltage transitions, $\overline{\text{RESET}}$ pins may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN}-V_{ccf} or V_{ccs}) does not exceed +9.0 V. Maximum DC input voltage on $\overline{\text{RESET}}$ pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

*3 : Minimum DC input voltage on $\overline{\text{WP/ACC}}$ pin is -0.5 V. During voltage transitions, $\overline{\text{WP/ACC}}$ pin may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{\text{WP/ACC}}$ pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns, when V_{ccf} is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | Unit |
|--|-------------------------------------|-------|------|------|
| | | Min | Max | |
| Ambient Temperature | T _A | -40 | +85 | °C |
| V _{ccf} /V _{ccs} Supply Voltages | V _{ccf} , V _{ccs} | +2.7 | +3.3 | V |

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

MB84VD2108XEM/2109XEM-70

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

| Parameter | Symbol | Test Conditions | Value | | | Unit | | |
|---|------------|--|-------------------------------------|------|------|---------------|----|----|
| | | | Min | Typ | Max | | | |
| Input Leakage Current | I_{LI} | $V_{IN} = V_{SS} \text{ to } V_{CCf}, V_{CCS}$ | -1.0 | — | +1.0 | μA | | |
| Output Leakage Current | I_{LO} | $V_{OUT} = V_{SS} \text{ to } V_{CCf}, V_{CCS}$ | -1.0 | — | +1.0 | μA | | |
| $\overline{\text{RESET}}$ Inputs Leakage Current | I_{LIT} | $V_{CCf} = V_{CCf} \text{ Max}, V_{CCS} = V_{CCS} \text{ Max},$ $\overline{\text{RESET}} = 12.5 \text{ V}$ | — | — | 35 | μA | | |
| Flash V_{CC} Active Current (Read) *1 | I_{CC1f} | $\overline{\text{CE}}f = V_{IL},$ $\overline{\text{OE}} = V_{IH}$ | $t_{\text{CYCLE}} = 5 \text{ MHz}$ | Byte | — | — | 13 | mA |
| | | | $t_{\text{CYCLE}} = 5 \text{ MHz}$ | Word | — | — | 15 | |
| | | | $t_{\text{CYCLE}} = 1 \text{ MHz}$ | Byte | — | — | 7 | mA |
| | | | $t_{\text{CYCLE}} = 1 \text{ MHz}$ | Word | — | — | 7 | |
| Flash V_{CC} Active Current (Program/Erase) *2 | I_{CC2f} | $\overline{\text{CE}}f = V_{IL}, \overline{\text{OE}} = V_{IH}$ | — | — | 35 | mA | | |
| Flash V_{CC} Active Current (Read-While-Program) *5 | I_{CC3f} | $\overline{\text{CE}}f = V_{IL}, \overline{\text{OE}} = V_{IH}$ | Byte | — | — | 48 | mA | |
| | | | Word | — | — | 50 | | |
| Flash V_{CC} Active Current (Read-While-Erase) *5 | I_{CC4f} | $\overline{\text{CE}}f = V_{IL}, \overline{\text{OE}} = V_{IH}$ | Byte | — | — | 48 | mA | |
| | | | Word | — | — | 50 | | |
| Flash V_{CC} Active Current (Erase-Suspend-Program) | I_{CC5f} | $\overline{\text{CE}}f = V_{IL}, \overline{\text{OE}} = V_{IH}$ | — | — | 35 | mA | | |
| ACC Input Leakage Current | I_{LIA} | $V_{CCf} = V_{CCf} \text{ Max}, V_{CCS} = V_{CCS} \text{ Max},$ $\overline{\text{WP/ACC}} = V_{ACC} \text{ Max}$ | — | — | 20 | mA | | |
| SRAM V_{CC} Active Current | I_{CC1S} | $V_{CCS} = V_{CCS} \text{ Max},$ $\overline{\text{CE}}1s = V_{IL},$ $\overline{\text{CE}}2s = V_{IH}$ | $t_{\text{CYCLE}} = 10 \text{ MHz}$ | — | — | 40 | mA | |
| SRAM V_{CC} Active Current | I_{CC2S} | $\overline{\text{CE}}1s = 0.2 \text{ V},$ $\overline{\text{CE}}2s = V_{CCS} - 0.2 \text{ V}$ | $t_{\text{CYCLE}} = 10 \text{ MHz}$ | — | — | 40 | mA | |
| | | | $t_{\text{CYCLE}} = 1 \text{ MHz}$ | — | — | 8 | mA | |
| Flash V_{CC} Standby Current | I_{SB1f} | $V_{CCf} = V_{CCf} \text{ Max}, \overline{\text{CE}}f = V_{CCf} \pm 0.3 \text{ V}$ $\overline{\text{RESET}} = V_{CCf} \pm 0.3 \text{ V},$ $\overline{\text{WP/ACC}} = V_{CCf} \pm 0.3 \text{ V}$ | — | 1 | 5 | μA | | |
| Flash V_{CC} Standby Current (RESET) | I_{SB2f} | $V_{CCf} = V_{CCf} \text{ Max}, \overline{\text{RESET}} = V_{SS} \pm 0.3 \text{ V},$ $\overline{\text{WP/ACC}} = V_{CCf} \pm 0.3 \text{ V}$ | — | 1 | 5 | μA | | |
| Flash V_{CC} Current (Automatic Sleep Mode) *3 | I_{SB3f} | $V_{CCf} = V_{CCf} \text{ Max}, \overline{\text{CE}}f = V_{SS} \pm 0.3 \text{ V}$ $\overline{\text{RESET}} = V_{CCf} \pm 0.3 \text{ V},$ $\overline{\text{WP/ACC}} = V_{CCf} \pm 0.3 \text{ V}$ $V_{IN} = V_{CCf} \pm 0.3 \text{ V} \text{ or } V_{SS} \pm 0.3 \text{ V}$ | — | 1 | 5 | μA | | |

(Continued)

MB84VD2108XEM/2109XEM-70

(Continued)

| Parameter | Symbol | Test Conditions | Value | | | Unit |
|---|-------------------|--|-------|-----|----------------------------|------|
| | | | Min | Typ | Max | |
| SRAM V _{CC} Standby Current | I _{SB1S} | $\overline{CE1s} \geq V_{CCS} - 0.2 \text{ V}, CE2s \geq V_{CCS} - 0.2 \text{ V}$ $\overline{LB} = \overline{UB} \geq V_{CCS} - 0.2 \text{ V or } \leq 0.2 \text{ V}$ | — | — | 7 | μA |
| SRAM V _{CC} Standby Current | I _{SB2S} | $\overline{CE1s} \geq V_{CCS} - 0.2 \text{ V or } \leq 0.2 \text{ V},$ $CE2s \leq 0.2 \text{ V}$ $\overline{LB} = \overline{UB} \geq V_{CCS} - 0.2 \text{ V or } \leq 0.2 \text{ V}$ | — | — | 7 | μA |
| Input Low Level | V _{IL} | — | -0.3 | — | 0.5 | V |
| Input High Level | V _{IH} | — | 2.4 | — | V _{CC} +0.3 *6 | V |
| Voltage for Sector Protection, and Temporary Sector Unprotection (RESET) *4 | V _{ID} | — | 11.5 | — | 12.5 | V |
| Voltage for Program Acceleration ($\overline{WP/ACC}$) *4 | V _{ACC} | — | 8.5 | 9.0 | 9.5 | V |
| SRAM Output Low Level | V _{OL} | V _{CCS} = V _{CCS} Min, I _{OL} = 4.0 mA | — | — | 0.45 | V |
| SRAM Output High Level | V _{OH} | V _{CCS} = V _{CCS} Min, I _{OH} = -0.5 mA | 2.4 | — | — | V |
| Flash Output Low Level | V _{OL} | V _{CCF} = V _{CCF} Min, I _{OL} = 4.0 mA | — | — | 0.4 | V |
| Flash Output High Level | V _{OH} | V _{CCF} = V _{CCF} Min, I _{OH} = -0.5 mA | 2.4 | — | — | V |
| Flash Low V _{CCF} Lock-Out Voltage | V _{LKO} | — | 2.3 | — | 2.5 | V |

* 1 : The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2 : I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3 : Automatic sleep mode enables the low power mode when address remain stable for 150 ns.

*4 : Applicable for only V_{CCF} applying.

*5 : Embedded Algorithm (program or erase) is in progress. (@5 MHz)

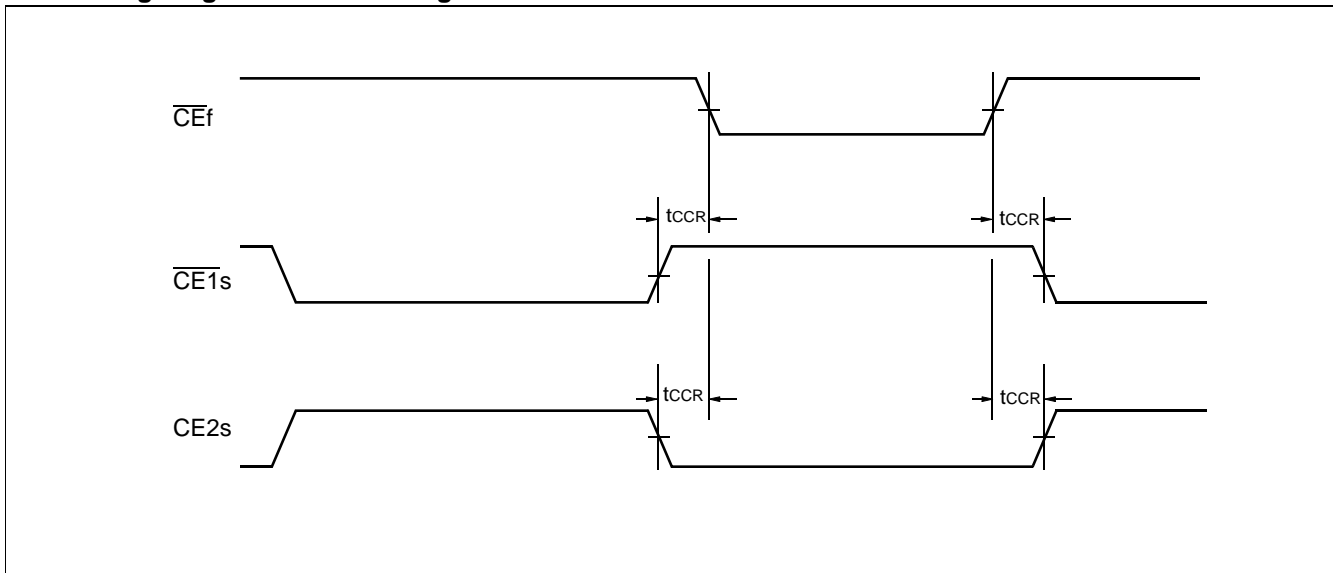
*6 : V_{CC} indicates lower of V_{CCF} or V_{CCS}.

2. AC Characteristics

- \overline{CE} Timing

| Parameter | Symbol | | Test Setup | Value | Unit |
|------------------------------|--------|-----------|------------|-------|------|
| | JEDEC | Standard | | Min | |
| \overline{CE} Recover Time | — | t_{CCR} | — | 0 | ns |

- Timing Diagram for alternating SRAM to Flash



- **Flash Characteristics**

Please refer to “■16M FLASH MEMORY CHARACTERISTICS for MCP” part.

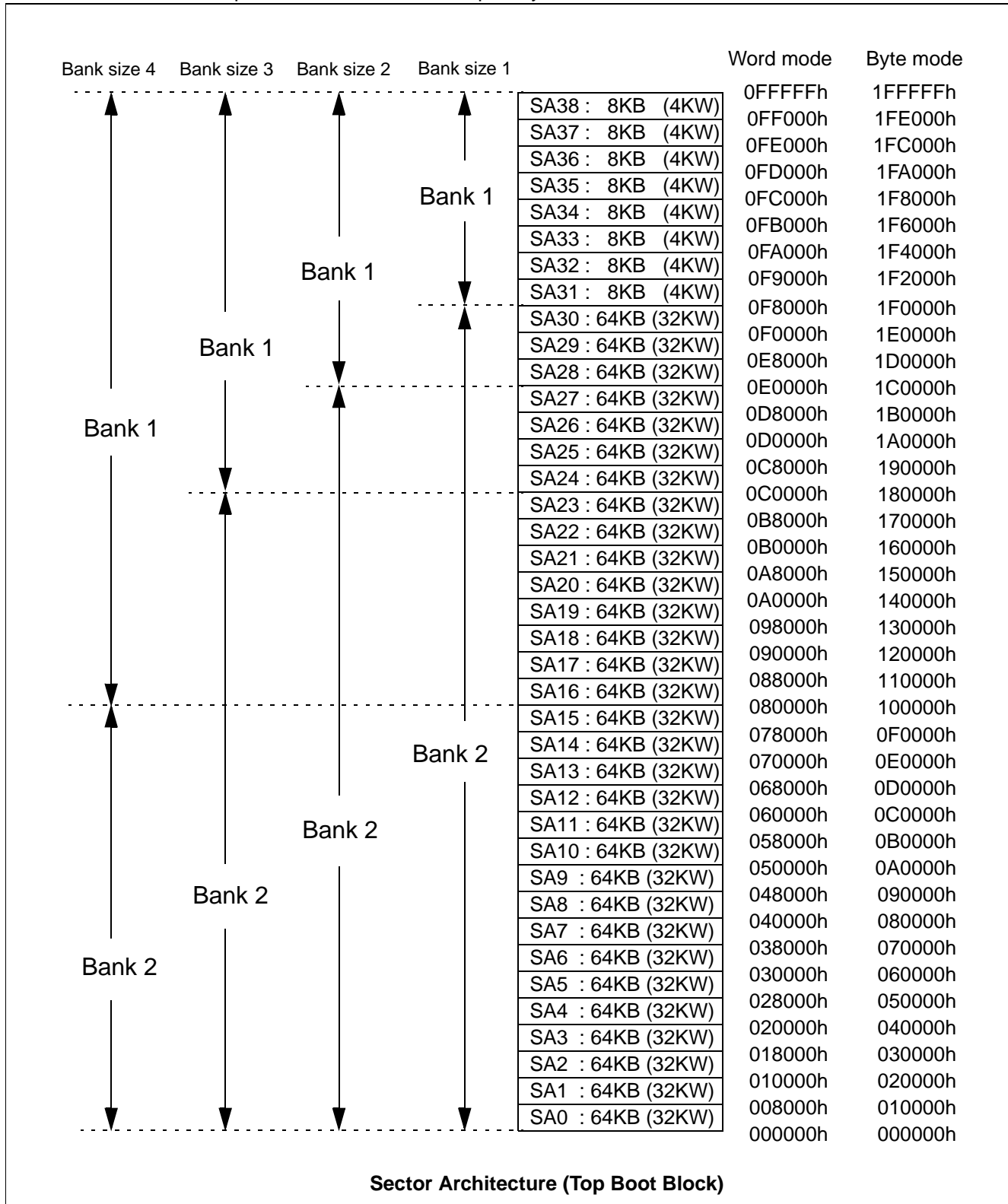
- **SRAM Characteristics,**

Please refer to “■2M SRAM CHARACTERISTICS for MCP” part.

■ 16M FLASH MEMORY CHARACTERISTICS for MCP

1. Flexible Sector-erase Architecture on Flash Memory

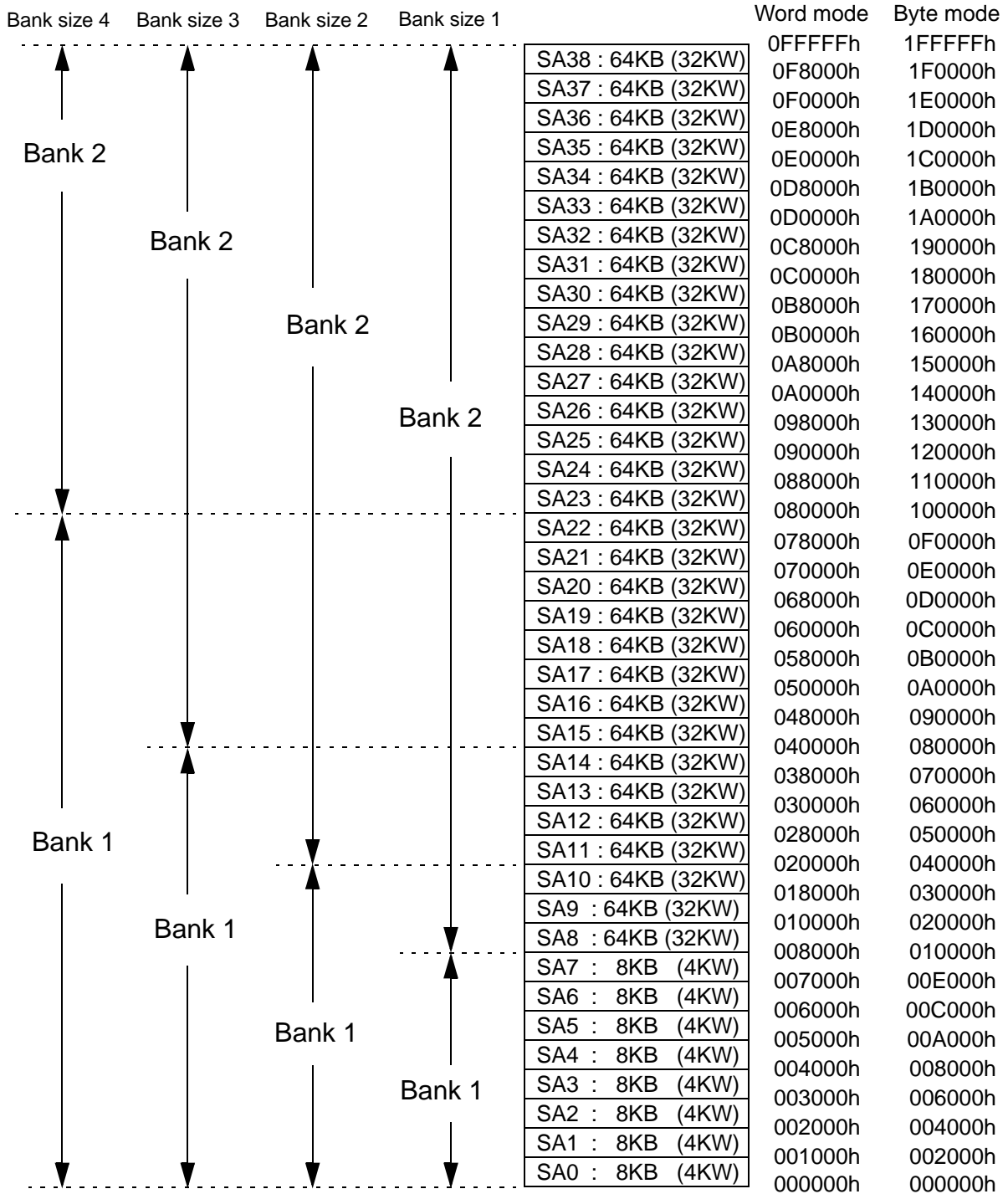
- Eight 4 K words, and thirty one 32 K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



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(Continued)

(Continued)



Sector Architecture (Bottom Boot Block)

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Sector Address Table (Top Boot Block, Bank Size=1)

| Bank | Sector | Sector Address | | | | | | | | Address Range (Byte mode) | Address Range (Word mode) |
|---------------|--------|----------------|-----|-----|-----|-----|-----|-----|--------------------|------------------------------|------------------------------|
| | | Bank Address | | | | | | | | | |
| | | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | | |
| Bank 2 | SA0 | 0 | 0 | 0 | 0 | 0 | X | X | X | 000000h to 00FFFFh | 000000h to 007FFFh |
| | SA1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 010000h to 01FFFFh | 008000h to 00FFFFh |
| | SA2 | 0 | 0 | 0 | 1 | 0 | X | X | X | 020000h to 02FFFFh | 010000h to 017FFFh |
| | SA3 | 0 | 0 | 0 | 1 | 1 | X | X | X | 030000h to 03FFFFh | 018000h to 01FFFFh |
| | SA4 | 0 | 0 | 1 | 0 | 0 | X | X | X | 040000h to 04FFFFh | 020000h to 027FFFh |
| | SA5 | 0 | 0 | 1 | 0 | 1 | X | X | X | 050000h to 05FFFFh | 028000h to 02FFFFh |
| | SA6 | 0 | 0 | 1 | 1 | 0 | X | X | X | 060000h to 06FFFFh | 030000h to 037FFFh |
| | SA7 | 0 | 0 | 1 | 1 | 1 | X | X | X | 070000h to 07FFFFh | 038000h to 03FFFFh |
| | SA8 | 0 | 1 | 0 | 0 | 0 | X | X | X | 080000h to 08FFFFh | 040000h to 047FFFh |
| | SA9 | 0 | 1 | 0 | 0 | 1 | X | X | X | 090000h to 09FFFFh | 048000h to 04FFFFh |
| | SA10 | 0 | 1 | 0 | 1 | 0 | X | X | X | 0A0000h to 0AFFFFh | 050000h to 057FFFh |
| | SA11 | 0 | 1 | 0 | 1 | 1 | X | X | X | 0B0000h to 0BFFFFh | 058000h to 05FFFFh |
| | SA12 | 0 | 1 | 1 | 0 | 0 | X | X | X | 0C0000h to 0CFFFFh | 060000h to 067FFFh |
| | SA13 | 0 | 1 | 1 | 0 | 1 | X | X | X | 0D0000h to 0DFFFFh | 068000h to 06FFFFh |
| | SA14 | 0 | 1 | 1 | 1 | 0 | X | X | X | 0E0000h to 0EFFFFh | 070000h to 077FFFh |
| | SA15 | 0 | 1 | 1 | 1 | 1 | X | X | X | 0F0000h to 0FFFFFh | 078000h to 07FFFFh |
| | SA16 | 1 | 0 | 0 | 0 | 0 | X | X | X | 100000h to 10FFFFh | 080000h to 087FFFh |
| | SA17 | 1 | 0 | 0 | 0 | 1 | X | X | X | 110000h to 11FFFFh | 088000h to 08FFFFh |
| | SA18 | 1 | 0 | 0 | 1 | 0 | X | X | X | 120000h to 12FFFFh | 090000h to 097FFFh |
| | SA19 | 1 | 0 | 0 | 1 | 1 | X | X | X | 130000h to 13FFFFh | 098000h to 09FFFFh |
| | SA20 | 1 | 0 | 1 | 0 | 0 | X | X | X | 140000h to 14FFFFh | 0A0000h to 0A7FFFh |
| | SA21 | 1 | 0 | 1 | 0 | 1 | X | X | X | 150000h to 15FFFFh | 0A8000h to 0AFFFFh |
| | SA22 | 1 | 0 | 1 | 1 | 0 | X | X | X | 160000h to 16FFFFh | 0B0000h to 0B7FFFh |
| | SA23 | 1 | 0 | 1 | 1 | 1 | X | X | X | 170000h to 17FFFFh | 0B8000h to 0BFFFFh |
| | SA24 | 1 | 1 | 0 | 0 | 0 | X | X | X | 180000h to 18FFFFh | 0C0000h to 0C7FFFh |
| | SA25 | 1 | 1 | 0 | 0 | 1 | X | X | X | 190000h to 19FFFFh | 0C8000h to 0CFFFFh |
| | SA26 | 1 | 1 | 0 | 1 | 0 | X | X | X | 1A0000h to 1AFFFFh | 0D0000h to 0D7FFFh |
| | SA27 | 1 | 1 | 0 | 1 | 1 | X | X | X | 1B0000h to 1BFFFFh | 0D8000h to 0DFFFFh |
| | SA28 | 1 | 1 | 1 | 0 | 0 | X | X | X | 1C0000h to 1CFFFFh | 0E0000h to 0E7FFFh |
| | SA29 | 1 | 1 | 1 | 0 | 1 | X | X | X | 1D0000h to 1DFFFFh | 0E8000h to 0EFFFFh |
| SA30 | 1 | 1 | 1 | 1 | 0 | X | X | X | 1E0000h to 1EFFFFh | 0F0000h to 0F7FFFh | |
| Bank 1 | SA31 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1F0000h to 1F1FFFh | 0F8000h to 0F8FFFh |
| | SA32 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1F2000h to 1F3FFFh | 0F9000h to 0F9FFFh |
| | SA33 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1F4000h to 1F5FFFh | 0FA000h to 0FAFFFh |
| | SA34 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1F6000h to 1F7FFFh | 0FB000h to 0FBFFFh |
| | SA35 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1F8000h to 1F9FFFh | 0FC000h to 0FCFFFh |
| | SA36 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1FA000h to 1FBFFFh | 0FD000h to 0FDFFFh |
| | SA37 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1FC000h to 1FDFFFh | 0FE000h to 0FEFFFh |
| | SA38 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1FE000h to 1FFFFFh | 0FF000h to 0FFFFFh |

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Sector Address Table (Bottom Boot Block, Bank Size=1)

| Bank | Sector | Sector Address | | | | | | | | Address Range (BYTE mode) | Address Range (WORD mode) | |
|--------|--------|----------------|-----|-----|-----|-----|-----|-----|---------------------|------------------------------|------------------------------|--------------------|
| | | Bank Address | | | | | | | | | | |
| | | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | | | |
| Bank 1 | SA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000000h to 001FFFh | 000000h to 000FFFh | |
| | SA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 002000h to 003FFFh | 001000h to 001FFFh | |
| | SA2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 004000h to 005FFFh | 002000h to 002FFFh |
| | SA3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 006000h to 007FFFh | 003000h to 003FFFh |
| | SA4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 008000h to 009FFFh | 004000h to 004FFFh |
| | SA5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 00A000h to 00BFFFh | 005000h to 005FFFh |
| | SA6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 00C000h to 00DFFFh | 006000h to 006FFFh |
| | SA7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 00E000h to 00FFFFh | 007000h to 007FFFh |
| Bank 2 | SA8 | 0 | 0 | 0 | 0 | 1 | X | X | X | 010000h to 01FFFFh | 008000h to 00FFFFh | |
| | SA9 | 0 | 0 | 0 | 1 | 0 | X | X | X | 020000h to 02FFFFh | 010000h to 017FFFh | |
| | SA10 | 0 | 0 | 0 | 1 | 1 | X | X | X | 030000h to 03FFFFh | 018000h to 01FFFFh | |
| | SA11 | 0 | 0 | 1 | 0 | 0 | X | X | X | 040000h to 04FFFFh | 020000h to 027FFFh | |
| | SA12 | 0 | 0 | 1 | 0 | 1 | X | X | X | 050000h to 05FFFFh | 028000h to 02FFFFh | |
| | SA13 | 0 | 0 | 1 | 1 | 0 | X | X | X | 060000h to 06FFFFh | 030000h to 037FFFh | |
| | SA14 | 0 | 0 | 1 | 1 | 1 | X | X | X | 070000h to 07FFFFh | 038000h to 03FFFFh | |
| | SA15 | 0 | 1 | 0 | 0 | 0 | X | X | X | 080000h to 08FFFFh | 040000h to 047FFFh | |
| | SA16 | 0 | 1 | 0 | 0 | 1 | X | X | X | 090000h to 09FFFFh | 048000h to 04FFFFh | |
| | SA17 | 0 | 1 | 0 | 1 | 0 | X | X | X | 0A0000h to 0AFFFFh | 050000h to 057FFFh | |
| | SA18 | 0 | 1 | 0 | 1 | 1 | X | X | X | 0B0000h to 0BFFFFh | 058000h to 05FFFFh | |
| | SA19 | 0 | 1 | 1 | 0 | 0 | X | X | X | 0C0000h to 0CFFFFh | 060000h to 067FFFh | |
| | SA20 | 0 | 1 | 1 | 0 | 1 | X | X | X | 0D0000h to 0DFFFFh | 068000h to 06FFFFh | |
| | SA21 | 0 | 1 | 1 | 1 | 0 | X | X | X | 0E0000h to 0EFFFFh | 070000h to 077FFFh | |
| | SA22 | 0 | 1 | 1 | 1 | 1 | X | X | X | 0F0000h to 0FFFFFFh | 078000h to 07FFFFh | |
| | SA23 | 1 | 0 | 0 | 0 | 0 | X | X | X | 100000h to 10FFFFh | 080000h to 087FFFh | |
| | SA24 | 1 | 0 | 0 | 0 | 1 | X | X | X | 110000h to 11FFFFh | 088000h to 08FFFFh | |
| | SA25 | 1 | 0 | 0 | 1 | 0 | X | X | X | 120000h to 12FFFFh | 090000h to 097FFFh | |
| | SA26 | 1 | 0 | 0 | 1 | 1 | X | X | X | 130000h to 13FFFFh | 098000h to 09FFFFh | |
| | SA27 | 1 | 0 | 1 | 0 | 0 | X | X | X | 140000h to 14FFFFh | 0A0000h to 0A7FFFh | |
| | SA28 | 1 | 0 | 1 | 0 | 1 | X | X | X | 150000h to 15FFFFh | 0A8000h to 0AFFFFh | |
| | SA29 | 1 | 0 | 1 | 1 | 0 | X | X | X | 160000h to 16FFFFh | 0B0000h to 0B7FFFh | |
| | SA30 | 1 | 0 | 1 | 1 | 1 | X | X | X | 170000h to 17FFFFh | 0B8000h to 0BFFFFh | |
| | SA31 | 1 | 1 | 0 | 0 | 0 | X | X | X | 180000h to 18FFFFh | 0C0000h to 0C7FFFh | |
| | SA32 | 1 | 1 | 0 | 0 | 1 | X | X | X | 190000h to 19FFFFh | 0C8000h to 0CFFFFh | |
| | SA33 | 1 | 1 | 0 | 1 | 0 | X | X | X | 1A0000h to 1AFFFFh | 0D0000h to 0D7FFFh | |
| | SA34 | 1 | 1 | 0 | 1 | 1 | X | X | X | 1B0000h to 1BFFFFh | 0D8000h to 0DFFFFh | |
| | SA35 | 1 | 1 | 1 | 0 | 0 | X | X | X | 1C0000h to 1CFFFFh | 0E0000h to 0E7FFFh | |
| | SA36 | 1 | 1 | 1 | 0 | 1 | X | X | X | 1D0000h to 1DFFFFh | 0E8000h to 0EFFFFh | |
| | SA37 | 1 | 1 | 1 | 1 | 0 | X | X | X | 1E0000h to 1EFFFFh | 0F0000h to 0F7FFFh | |
| SA38 | 1 | 1 | 1 | 1 | 1 | X | X | X | 1F0000h to 1FFFFFFh | 0F8000h to 0FFFFFFh | | |

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Sector Address Table (Top Boot Block, Bank Size=2)

| Bank | Sector | Sector Address | | | | | | | | Address Range (BYTE mode) | Address Range (WORD mode) |
|---------------|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------|------------------------------|------------------------------|
| | | Bank Address | | | | | | | | | |
| | | A ₁₉ | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | | |
| Bank 2 | SA0 | 0 | 0 | 0 | 0 | 0 | X | X | X | 000000h to 00FFFFh | 000000h to 007FFFh |
| | SA1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 010000h to 01FFFFh | 008000h to 00FFFFh |
| | SA2 | 0 | 0 | 0 | 1 | 0 | X | X | X | 020000h to 02FFFFh | 010000h to 017FFFh |
| | SA3 | 0 | 0 | 0 | 1 | 1 | X | X | X | 030000h to 03FFFFh | 018000h to 01FFFFh |
| | SA4 | 0 | 0 | 1 | 0 | 0 | X | X | X | 040000h to 04FFFFh | 020000h to 027FFFh |
| | SA5 | 0 | 0 | 1 | 0 | 1 | X | X | X | 050000h to 05FFFFh | 028000h to 02FFFFh |
| | SA6 | 0 | 0 | 1 | 1 | 0 | X | X | X | 060000h to 06FFFFh | 030000h to 037FFFh |
| | SA7 | 0 | 0 | 1 | 1 | 1 | X | X | X | 070000h to 07FFFFh | 038000h to 03FFFFh |
| | SA8 | 0 | 1 | 0 | 0 | 0 | X | X | X | 080000h to 08FFFFh | 040000h to 047FFFh |
| | SA9 | 0 | 1 | 0 | 0 | 1 | X | X | X | 090000h to 09FFFFh | 048000h to 04FFFFh |
| | SA10 | 0 | 1 | 0 | 1 | 0 | X | X | X | 0A0000h to 0AFFFFh | 050000h to 057FFFh |
| | SA11 | 0 | 1 | 0 | 1 | 1 | X | X | X | 0B0000h to 0BFFFFh | 058000h to 05FFFFh |
| | SA12 | 0 | 1 | 1 | 0 | 0 | X | X | X | 0C0000h to 0CFFFFh | 060000h to 067FFFh |
| | SA13 | 0 | 1 | 1 | 0 | 1 | X | X | X | 0D0000h to 0DFFFFh | 068000h to 06FFFFh |
| | SA14 | 0 | 1 | 1 | 1 | 0 | X | X | X | 0E0000h to 0EFFFFh | 070000h to 077FFFh |
| | SA15 | 0 | 1 | 1 | 1 | 1 | X | X | X | 0F0000h to 0FFFFh | 078000h to 077FFFh |
| | SA16 | 1 | 0 | 0 | 0 | 0 | X | X | X | 100000h to 10FFFFh | 080000h to 087FFFh |
| | SA17 | 1 | 0 | 0 | 0 | 1 | X | X | X | 110000h to 11FFFFh | 088000h to 08FFFFh |
| | SA18 | 1 | 0 | 0 | 1 | 0 | X | X | X | 120000h to 12FFFFh | 090000h to 097FFFh |
| | SA19 | 1 | 0 | 0 | 1 | 1 | X | X | X | 130000h to 13FFFFh | 098000h to 09FFFFh |
| | SA20 | 1 | 0 | 1 | 0 | 0 | X | X | X | 140000h to 14FFFFh | 0A0000h to 0A7FFFh |
| | SA21 | 1 | 0 | 1 | 0 | 1 | X | X | X | 150000h to 15FFFFh | 0A8000h to 0AFFFFh |
| | SA22 | 1 | 0 | 1 | 1 | 0 | X | X | X | 160000h to 16FFFFh | 0B0000h to 0B7FFFh |
| | SA23 | 1 | 0 | 1 | 1 | 1 | X | X | X | 170000h to 17FFFFh | 0B8000h to 0BFFFFh |
| | SA24 | 1 | 1 | 0 | 0 | 0 | X | X | X | 180000h to 18FFFFh | 0C0000h to 0C7FFFh |
| | SA25 | 1 | 1 | 0 | 0 | 1 | X | X | X | 190000h to 19FFFFh | 0C8000h to 0CFFFFh |
| | SA26 | 1 | 1 | 0 | 1 | 0 | X | X | X | 1A0000h to 1AFFFFh | 0D0000h to 0D7FFFh |
| SA27 | 1 | 1 | 0 | 1 | 1 | X | X | X | 1B0000h to 1BFFFFh | 0D8000h to 0DFFFFh | |
| Bank 1 | SA28 | 1 | 1 | 1 | 0 | 0 | X | X | X | 1C0000h to 1CFFFFh | 0E0000h to 0E7FFFh |
| | SA29 | 1 | 1 | 1 | 0 | 1 | X | X | X | 1D0000h to 1DFFFFh | 0E8000h to 0EFFFFh |
| | SA30 | 1 | 1 | 1 | 1 | 0 | X | X | X | 1E0000h to 1EFFFFh | 0F0000h to 0F7FFFh |
| | SA31 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1F0000h to 1F1FFFh | 0F8000h to 0F8FFFh |
| | SA32 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1F2000h to 1F3FFFh | 0F9000h to 0F9FFFh |
| | SA33 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1F4000h to 1F5FFFh | 0FA000h to 0FAFFFh |
| | SA34 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1F6000h to 1F7FFFh | 0FB000h to 0FBFFFh |
| | SA35 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1F8000h to 1F9FFFh | 0FC000h to 0FCFFFh |
| | SA36 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1FA000h to 1FBFFFh | 0FD000h to 0FDFFFh |
| | SA37 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1FC000h to 1FDFFFh | 0FE000h to 0FEFFFh |
| | SA38 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1FE000h to 1FFFFh | 0FF000h to 0FFFFh |

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Sector Address Table (Bottom Boot Block, Bank Size=2)

| Bank | Sector | Sector Address | | | | | | | | Address Range (BYTE mode) | Address Range (WORD mode) | |
|--------|--------|----------------|-----|-----|-----|-----|-----|-----|-----|------------------------------|------------------------------|--------------------|
| | | Bank Address | | | | | | | | | | |
| | | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | | | |
| Bank 1 | SA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000000h to 001FFFh | 000000h to 000FFFh | |
| | SA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 002000h to 003FFFh | 001000h to 001FFFh | |
| | SA2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 004000h to 005FFFh | 002000h to 002FFFh |
| | SA3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 006000h to 007FFFh | 003000h to 003FFFh |
| | SA4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 008000h to 009FFFh | 004000h to 004FFFh |
| | SA5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 00A000h to 00BFFFh | 005000h to 005FFFh |
| | SA6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 00C000h to 00DFFFh | 006000h to 006FFFh |
| | SA7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 00E000h to 00FFFFh | 007000h to 007FFFh |
| | SA8 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | 010000h to 01FFFFh | 008000h to 00FFFFh |
| | SA9 | 0 | 0 | 0 | 1 | 0 | X | X | X | | 020000h to 02FFFFh | 010000h to 017FFFh |
| | SA10 | 0 | 0 | 0 | 1 | 1 | X | X | X | | 030000h to 03FFFFh | 018000h to 01FFFFh |
| Bank 2 | SA11 | 0 | 0 | 1 | 0 | 0 | X | X | X | 040000h to 04FFFFh | 020000h to 027FFFh | |
| | SA12 | 0 | 0 | 1 | 0 | 1 | X | X | X | 050000h to 05FFFFh | 028000h to 02FFFFh | |
| | SA13 | 0 | 0 | 1 | 1 | 0 | X | X | X | 060000h to 06FFFFh | 030000h to 037FFFh | |
| | SA14 | 0 | 0 | 1 | 1 | 1 | X | X | X | 070000h to 07FFFFh | 038000h to 03FFFFh | |
| | SA15 | 0 | 1 | 0 | 0 | 0 | X | X | X | 080000h to 08FFFFh | 040000h to 047FFFh | |
| | SA16 | 0 | 1 | 0 | 0 | 1 | X | X | X | 090000h to 09FFFFh | 048000h to 04FFFFh | |
| | SA17 | 0 | 1 | 0 | 1 | 0 | X | X | X | 0A0000h to 0AFFFFh | 050000h to 057FFFh | |
| | SA18 | 0 | 1 | 0 | 1 | 1 | X | X | X | 0B0000h to 0BFFFFh | 058000h to 05FFFFh | |
| | SA19 | 0 | 1 | 1 | 0 | 0 | X | X | X | 0C0000h to 0CFFFFh | 060000h to 067FFFh | |
| | SA20 | 0 | 1 | 1 | 0 | 1 | X | X | X | 0D0000h to 0DFFFFh | 068000h to 06FFFFh | |
| | SA21 | 0 | 1 | 1 | 1 | 0 | X | X | X | 0E0000h to 0EFFFFh | 070000h to 077FFFh | |
| | SA22 | 0 | 1 | 1 | 1 | 1 | X | X | X | 0F0000h to 0FFFFFFh | 078000h to 07FFFFh | |
| | SA23 | 1 | 0 | 0 | 0 | 0 | X | X | X | 100000h to 10FFFFh | 080000h to 087FFFh | |
| | SA24 | 1 | 0 | 0 | 0 | 1 | X | X | X | 110000h to 11FFFFh | 088000h to 08FFFFh | |
| | SA25 | 1 | 0 | 0 | 1 | 0 | X | X | X | 120000h to 12FFFFh | 090000h to 097FFFh | |
| | SA26 | 1 | 0 | 0 | 1 | 1 | X | X | X | 130000h to 13FFFFh | 098000h to 09FFFFh | |
| | SA27 | 1 | 0 | 1 | 0 | 0 | X | X | X | 140000h to 14FFFFh | 0A0000h to 0A7FFFh | |
| | SA28 | 1 | 0 | 1 | 0 | 1 | X | X | X | 150000h to 15FFFFh | 0A8000h to 0AFFFFh | |
| | SA29 | 1 | 0 | 1 | 1 | 0 | X | X | X | 160000h to 16FFFFh | 0B0000h to 0B7FFFh | |
| | SA30 | 1 | 0 | 1 | 1 | 1 | X | X | X | 170000h to 17FFFFh | 0B8000h to 0BFFFFh | |
| | SA31 | 1 | 1 | 0 | 0 | 0 | X | X | X | 180000h to 18FFFFh | 0C0000h to 0C7FFFh | |
| | SA32 | 1 | 1 | 0 | 0 | 1 | X | X | X | 190000h to 19FFFFh | 0C8000h to 0CFFFFh | |
| | SA33 | 1 | 1 | 0 | 1 | 0 | X | X | X | 1A0000h to 1AFFFFh | 0D0000h to 0D7FFFh | |
| | SA34 | 1 | 1 | 0 | 1 | 1 | X | X | X | 1B0000h to 1BFFFFh | 0D8000h to 0DFFFFh | |
| | SA35 | 1 | 1 | 1 | 0 | 0 | X | X | X | 1C0000h to 1CFFFFh | 0E0000h to 0E7FFFh | |
| | SA36 | 1 | 1 | 1 | 0 | 1 | X | X | X | 1D0000h to 1DFFFFh | 0E8000h to 0EFFFFh | |
| | SA37 | 1 | 1 | 1 | 1 | 0 | X | X | X | 1E0000h to 1EFFFFh | 0F0000h to 0F7FFFh | |
| | SA38 | 1 | 1 | 1 | 1 | 1 | X | X | X | 1F0000h to 1FFFFFFh | 0F8000h to 0FFFFFFh | |

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Sector Address Table (Top Boot Block, Bank Size=3)

| Bank | Sector | Sector Address | | | | | | | | Address Range (BYTE mode) | Address Range (WORD mode) |
|--------|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------|------------------------------|------------------------------|
| | | Bank Address | | | | | | | | | |
| | | A ₁₉ | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | | |
| Bank 2 | SA0 | 0 | 0 | 0 | 0 | 0 | X | X | X | 000000h to 00FFFFh | 000000h to 007FFFh |
| | SA1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 010000h to 01FFFFh | 008000h to 00FFFFh |
| | SA2 | 0 | 0 | 0 | 1 | 0 | X | X | X | 020000h to 02FFFFh | 010000h to 017FFFh |
| | SA3 | 0 | 0 | 0 | 1 | 1 | X | X | X | 030000h to 03FFFFh | 018000h to 01FFFFh |
| | SA4 | 0 | 0 | 1 | 0 | 0 | X | X | X | 040000h to 04FFFFh | 020000h to 027FFFh |
| | SA5 | 0 | 0 | 1 | 0 | 1 | X | X | X | 050000h to 05FFFFh | 028000h to 02FFFFh |
| | SA6 | 0 | 0 | 1 | 1 | 0 | X | X | X | 060000h to 06FFFFh | 030000h to 037FFFh |
| | SA7 | 0 | 0 | 1 | 1 | 1 | X | X | X | 070000h to 07FFFFh | 038000h to 03FFFFh |
| | SA8 | 0 | 1 | 0 | 0 | 0 | X | X | X | 080000h to 08FFFFh | 040000h to 047FFFh |
| | SA9 | 0 | 1 | 0 | 0 | 1 | X | X | X | 090000h to 09FFFFh | 048000h to 04FFFFh |
| | SA10 | 0 | 1 | 0 | 1 | 0 | X | X | X | 0A0000h to 0AFFFFh | 050000h to 057FFFh |
| | SA11 | 0 | 1 | 0 | 1 | 1 | X | X | X | 0B0000h to 0BFFFFh | 058000h to 05FFFFh |
| | SA12 | 0 | 1 | 1 | 0 | 0 | X | X | X | 0C0000h to 0CFFFFh | 060000h to 067FFFh |
| | SA13 | 0 | 1 | 1 | 0 | 1 | X | X | X | 0D0000h to 0DFFFFh | 068000h to 06FFFFh |
| | SA14 | 0 | 1 | 1 | 1 | 0 | X | X | X | 0E0000h to 0EFFFFh | 070000h to 077FFFh |
| | SA15 | 0 | 1 | 1 | 1 | 1 | X | X | X | 0F0000h to 0FFFFFh | 078000h to 07FFFFh |
| | SA16 | 1 | 0 | 0 | 0 | 0 | X | X | X | 100000h to 10FFFFh | 080000h to 087FFFh |
| | SA17 | 1 | 0 | 0 | 0 | 1 | X | X | X | 110000h to 11FFFFh | 088000h to 08FFFFh |
| | SA18 | 1 | 0 | 0 | 1 | 0 | X | X | X | 120000h to 12FFFFh | 090000h to 097FFFh |
| | SA19 | 1 | 0 | 0 | 1 | 1 | X | X | X | 130000h to 13FFFFh | 098000h to 09FFFFh |
| | SA20 | 1 | 0 | 1 | 0 | 0 | X | X | X | 140000h to 14FFFFh | 0A0000h to 0A7FFFh |
| | SA21 | 1 | 0 | 1 | 0 | 1 | X | X | X | 150000h to 15FFFFh | 0A8000h to 0AFFFFh |
| | SA22 | 1 | 0 | 1 | 1 | 0 | X | X | X | 160000h to 16FFFFh | 0B0000h to 0B7FFFh |
| SA23 | 1 | 0 | 1 | 1 | 1 | X | X | X | 170000h to 17FFFFh | 0B8000h to 0BFFFFh | |
| Bank 1 | SA24 | 1 | 1 | 0 | 0 | 0 | X | X | X | 180000h to 18FFFFh | 0C0000h to 0C7FFFh |
| | SA25 | 1 | 1 | 0 | 0 | 1 | X | X | X | 190000h to 19FFFFh | 0C8000h to 0CFFFFh |
| | SA26 | 1 | 1 | 0 | 1 | 0 | X | X | X | 1A0000h to 1AFFFFh | 0D0000h to 0D7FFFh |
| | SA27 | 1 | 1 | 0 | 1 | 1 | X | X | X | 1B0000h to 1BFFFFh | 0D8000h to 0DFFFFh |
| | SA28 | 1 | 1 | 1 | 0 | 0 | X | X | X | 1C0000h to 1CFFFFh | 0E0000h to 0E7FFFh |
| | SA29 | 1 | 1 | 1 | 0 | 1 | X | X | X | 1D0000h to 1DFFFFh | 0E8000h to 0EFFFFh |
| | SA30 | 1 | 1 | 1 | 1 | 0 | X | X | X | 1E0000h to 1EFFFFh | 0F0000h to 0F7FFFh |
| | SA31 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1F0000h to 1F1FFFh | 0F8000h to 0F8FFFh |
| | SA32 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1F2000h to 1F3FFFh | 0F9000h to 0F9FFFh |
| | SA33 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1F4000h to 1F5FFFh | 0FA000h to 0FAFFFh |
| | SA34 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1F6000h to 1F7FFFh | 0FB000h to 0FBFFFh |
| | SA35 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1F8000h to 1F9FFFh | 0FC000h to 0FCFFFh |
| | SA36 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1FA000h to 1FBFFFh | 0FD000h to 0FDFFFh |
| | SA37 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1FC000h to 1FDFFFh | 0FE000h to 0FEFFFh |
| | SA38 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1FE000h to 1FFFFFh | 0FF000h to 0FFFFFh |

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Sector Address Table (Bottom Boot Block, Bank Size=3)

| Bank | Sector | Sector Address | | | | | | | | Address Range (BYTE mode) | Address Range (WORD mode) | |
|--------|--------|----------------|-----|-----|-----|-----|-----|-----|-----|------------------------------|------------------------------|--------------------|
| | | Bank Address | | | | | | | | | | |
| | | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | | | |
| Bank 1 | SA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000000h to 001FFFh | 000000h to 000FFFh | |
| | SA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 002000h to 003FFFh | 001000h to 001FFFh | |
| | SA2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 004000h to 005FFFh | 002000h to 002FFFh | |
| | SA3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 006000h to 007FFFh | 003000h to 003FFFh | |
| | SA4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 008000h to 009FFFh | 004000h to 004FFFh | |
| | SA5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 00A000h to 00BFFFh | 005000h to 005FFFh | |
| | SA6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 00C000h to 00DFFFh | 006000h to 006FFFh | |
| | SA7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 00E000h to 00FFFFh | 007000h to 007FFFh | |
| | SA8 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | 010000h to 01FFFFh | 008000h to 00FFFFh |
| | SA9 | 0 | 0 | 0 | 1 | 0 | 0 | X | X | X | 020000h to 02FFFFh | 010000h to 017FFFh |
| | SA10 | 0 | 0 | 0 | 1 | 1 | 0 | X | X | X | 030000h to 03FFFFh | 018000h to 01FFFFh |
| | SA11 | 0 | 0 | 1 | 0 | 0 | 0 | X | X | X | 040000h to 04FFFFh | 020000h to 027FFFh |
| | SA12 | 0 | 0 | 1 | 0 | 1 | 0 | X | X | X | 050000h to 05FFFFh | 028000h to 02FFFFh |
| | SA13 | 0 | 0 | 1 | 1 | 0 | 0 | X | X | X | 060000h to 06FFFFh | 030000h to 037FFFh |
| SA14 | 0 | 0 | 1 | 1 | 1 | 0 | X | X | X | 070000h to 07FFFFh | 038000h to 03FFFFh | |
| Bank 2 | SA15 | 0 | 1 | 0 | 0 | 0 | X | X | X | 080000h to 08FFFFh | 040000h to 047FFFh | |
| | SA16 | 0 | 1 | 0 | 0 | 1 | X | X | X | 090000h to 09FFFFh | 048000h to 04FFFFh | |
| | SA17 | 0 | 1 | 0 | 1 | 0 | X | X | X | 0A0000h to 0AFFFFh | 050000h to 057FFFh | |
| | SA18 | 0 | 1 | 0 | 1 | 1 | X | X | X | 0B0000h to 0BFFFFh | 058000h to 05FFFFh | |
| | SA19 | 0 | 1 | 1 | 0 | 0 | X | X | X | 0C0000h to 0CFFFFh | 060000h to 067FFFh | |
| | SA20 | 0 | 1 | 1 | 0 | 1 | X | X | X | 0D0000h to 0DFFFFh | 068000h to 06FFFFh | |
| | SA21 | 0 | 1 | 1 | 1 | 0 | X | X | X | 0E0000h to 0EFFFFh | 070000h to 077FFFh | |
| | SA22 | 0 | 1 | 1 | 1 | 1 | X | X | X | 0F0000h to 0FFFFFh | 078000h to 07FFFFh | |
| | SA23 | 1 | 0 | 0 | 0 | 0 | X | X | X | 100000h to 10FFFFh | 080000h to 087FFFh | |
| | SA24 | 1 | 0 | 0 | 0 | 1 | X | X | X | 110000h to 11FFFFh | 088000h to 08FFFFh | |
| | SA25 | 1 | 0 | 0 | 1 | 0 | X | X | X | 120000h to 12FFFFh | 090000h to 097FFFh | |
| | SA26 | 1 | 0 | 0 | 1 | 1 | X | X | X | 130000h to 13FFFFh | 098000h to 09FFFFh | |
| | SA27 | 1 | 0 | 1 | 0 | 0 | X | X | X | 140000h to 14FFFFh | 0A0000h to 0A7FFFh | |
| | SA28 | 1 | 0 | 1 | 0 | 1 | X | X | X | 150000h to 15FFFFh | 0A8000h to 0AFFFFh | |
| | SA29 | 1 | 0 | 1 | 1 | 0 | X | X | X | 160000h to 16FFFFh | 0B0000h to 0B7FFFh | |
| | SA30 | 1 | 0 | 1 | 1 | 1 | X | X | X | 170000h to 17FFFFh | 0B8000h to 0BFFFFh | |
| | SA31 | 1 | 1 | 0 | 0 | 0 | X | X | X | 180000h to 18FFFFh | 0C0000h to 0C7FFFh | |
| | SA32 | 1 | 1 | 0 | 0 | 1 | X | X | X | 190000h to 19FFFFh | 0C8000h to 0CFFFFh | |
| | SA33 | 1 | 1 | 0 | 1 | 0 | X | X | X | 1A0000h to 1AFFFFh | 0D0000h to 0D7FFFh | |
| | SA34 | 1 | 1 | 0 | 1 | 1 | X | X | X | 1B0000h to 1BFFFFh | 0D8000h to 0DFFFFh | |
| | SA35 | 1 | 1 | 1 | 0 | 0 | X | X | X | 1C0000h to 1CFFFFh | 0E0000h to 0E7FFFh | |
| | SA36 | 1 | 1 | 1 | 0 | 1 | X | X | X | 1D0000h to 1DFFFFh | 0E8000h to 0EFFFFh | |
| | SA37 | 1 | 1 | 1 | 1 | 0 | X | X | X | 1E0000h to 1EFFFFh | 0F0000h to 0F7FFFh | |
| | SA38 | 1 | 1 | 1 | 1 | 1 | X | X | X | 1F0000h to 1FFFFFh | 0F8000h to 0FFFFFh | |

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Sector Address Table (Top Boot Block, Bank Size=4)

| Bank | Sector | Sector Address | | | | | | | | Address Range (BYTE mode) | Address Range (WORD mode) |
|---------------|--------|----------------|-----|-----|-----|-----|-----|-----|--------------------|------------------------------|------------------------------|
| | | Bank Address | | | | | | | | | |
| | | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | | |
| Bank 2 | SA0 | 0 | 0 | 0 | 0 | 0 | X | X | X | 000000h to 00FFFFh | 000000h to 007FFFh |
| | SA1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 010000h to 01FFFFh | 008000h to 00FFFFh |
| | SA2 | 0 | 0 | 0 | 1 | 0 | X | X | X | 020000h to 02FFFFh | 010000h to 017FFFh |
| | SA3 | 0 | 0 | 0 | 1 | 1 | X | X | X | 030000h to 03FFFFh | 018000h to 01FFFFh |
| | SA4 | 0 | 0 | 1 | 0 | 0 | X | X | X | 040000h to 04FFFFh | 020000h to 027FFFh |
| | SA5 | 0 | 0 | 1 | 0 | 1 | X | X | X | 050000h to 05FFFFh | 028000h to 02FFFFh |
| | SA6 | 0 | 0 | 1 | 1 | 0 | X | X | X | 060000h to 06FFFFh | 030000h to 037FFFh |
| | SA7 | 0 | 0 | 1 | 1 | 1 | X | X | X | 070000h to 07FFFFh | 038000h to 03FFFFh |
| | SA8 | 0 | 1 | 0 | 0 | 0 | X | X | X | 080000h to 08FFFFh | 040000h to 047FFFh |
| | SA9 | 0 | 1 | 0 | 0 | 1 | X | X | X | 090000h to 09FFFFh | 048000h to 04FFFFh |
| | SA10 | 0 | 1 | 0 | 1 | 0 | X | X | X | 0A0000h to 0AFFFFh | 050000h to 057FFFh |
| | SA11 | 0 | 1 | 0 | 1 | 1 | X | X | X | 0B0000h to 0BFFFFh | 058000h to 05FFFFh |
| | SA12 | 0 | 1 | 1 | 0 | 0 | X | X | X | 0C0000h to 0CFFFFh | 060000h to 067FFFh |
| | SA13 | 0 | 1 | 1 | 0 | 1 | X | X | X | 0D0000h to 0DFFFFh | 068000h to 06FFFFh |
| | SA14 | 0 | 1 | 1 | 1 | 0 | X | X | X | 0E0000h to 0EFFFFh | 070000h to 077FFFh |
| SA15 | 0 | 1 | 1 | 1 | 1 | X | X | X | 0F0000h to 0FFFFFh | 078000h to 07FFFFh | |
| Bank 1 | SA16 | 1 | 0 | 0 | 0 | 0 | X | X | X | 100000h to 10FFFFh | 080000h to 087FFFh |
| | SA17 | 1 | 0 | 0 | 0 | 1 | X | X | X | 110000h to 11FFFFh | 088000h to 08FFFFh |
| | SA18 | 1 | 0 | 0 | 1 | 0 | X | X | X | 120000h to 12FFFFh | 090000h to 097FFFh |
| | SA19 | 1 | 0 | 0 | 1 | 1 | X | X | X | 130000h to 13FFFFh | 098000h to 09FFFFh |
| | SA20 | 1 | 0 | 1 | 0 | 0 | X | X | X | 140000h to 14FFFFh | 0A0000h to 0A7FFFh |
| | SA21 | 1 | 0 | 1 | 0 | 1 | X | X | X | 150000h to 15FFFFh | 0A8000h to 0AFFFFh |
| | SA22 | 1 | 0 | 1 | 1 | 0 | X | X | X | 160000h to 16FFFFh | 0B0000h to 0B7FFFh |
| | SA23 | 1 | 0 | 1 | 1 | 1 | X | X | X | 170000h to 17FFFFh | 0B8000h to 0BFFFFh |
| | SA24 | 1 | 1 | 0 | 0 | 0 | X | X | X | 180000h to 18FFFFh | 0C0000h to 0C7FFFh |
| | SA25 | 1 | 1 | 0 | 0 | 1 | X | X | X | 190000h to 19FFFFh | 0C8000h to 0CFFFFh |
| | SA26 | 1 | 1 | 0 | 1 | 0 | X | X | X | 1A0000h to 1AFFFFh | 0D0000h to 0D7FFFh |
| | SA27 | 1 | 1 | 0 | 1 | 1 | X | X | X | 1B0000h to 1BFFFFh | 0D8000h to 0DFFFFh |
| | SA28 | 1 | 1 | 1 | 0 | 0 | X | X | X | 1C0000h to 1CFFFFh | 0E0000h to 0E7FFFh |
| | SA29 | 1 | 1 | 1 | 0 | 1 | X | X | X | 1D0000h to 1DFFFFh | 0E8000h to 0EFFFFh |
| | SA30 | 1 | 1 | 1 | 1 | 0 | X | X | X | 1E0000h to 1EFFFFh | 0F0000h to 0F7FFFh |
| | SA31 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1F0000h to 1F1FFFh | 0F8000h to 0F8FFFh |
| | SA32 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1F2000h to 1F3FFFh | 0F9000h to 0F9FFFh |
| | SA33 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1F4000h to 1F5FFFh | 0FA000h to 0FAFFFh |
| | SA34 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1F6000h to 1F7FFFh | 0FB000h to 0FBFFFh |
| | SA35 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1F8000h to 1F9FFFh | 0FC000h to 0FCFFFh |
| | SA36 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1FA000h to 1FBFFFh | 0FD000h to 0FDFFFh |
| | SA37 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1FC000h to 1FDFFFh | 0FE000h to 0FEFFFh |
| | SA38 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1FE000h to 1FFFFFh | 0FF000h to 0FFFFFh |

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Sector Address Table (Bottom Boot Block, Bank Size=4)

| Bank | Sector | Sector Address | | | | | | | | Address Range (BYTE mode) | Address Range (WORD mode) | |
|--------|--------|----------------|-----|-----|-----|-----|-----|-----|-----|------------------------------|------------------------------|--------------------|
| | | Bank Address | | | | | | | | | | |
| | | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | | | |
| Bank 1 | SA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000000h to 001FFFh | 000000h to 000FFFh | |
| | SA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 002000h to 003FFFh | 001000h to 001FFFh | |
| | SA2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 004000h to 005FFFh | 002000h to 002FFFh |
| | SA3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 006000h to 007FFFh | 003000h to 003FFFh |
| | SA4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 008000h to 009FFFh | 004000h to 004FFFh |
| | SA5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 00A000h to 00BFFFh | 005000h to 005FFFh |
| | SA6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 00C000h to 00DFFFh | 006000h to 006FFFh |
| | SA7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 00E000h to 00FFFFh | 007000h to 007FFFh |
| | SA8 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | 010000h to 01FFFFh | 008000h to 00FFFFh |
| | SA9 | 0 | 0 | 0 | 1 | 0 | X | X | X | | 020000h to 02FFFFh | 010000h to 017FFFh |
| | SA10 | 0 | 0 | 0 | 1 | 1 | X | X | X | | 030000h to 03FFFFh | 018000h to 01FFFFh |
| | SA11 | 0 | 0 | 1 | 0 | 0 | X | X | X | | 040000h to 04FFFFh | 020000h to 027FFFh |
| | SA12 | 0 | 0 | 1 | 0 | 1 | X | X | X | | 050000h to 05FFFFh | 028000h to 02FFFFh |
| | SA13 | 0 | 0 | 1 | 1 | 0 | X | X | X | | 060000h to 06FFFFh | 030000h to 037FFFh |
| | SA14 | 0 | 0 | 1 | 1 | 1 | X | X | X | | 070000h to 07FFFFh | 038000h to 03FFFFh |
| | SA15 | 0 | 1 | 0 | 0 | 0 | X | X | X | | 080000h to 08FFFFh | 040000h to 047FFFh |
| | SA16 | 0 | 1 | 0 | 0 | 1 | X | X | X | | 090000h to 09FFFFh | 048000h to 04FFFFh |
| | SA17 | 0 | 1 | 0 | 1 | 0 | X | X | X | | 0A0000h to 0AFFFFh | 050000h to 057FFFh |
| | SA18 | 0 | 1 | 0 | 1 | 1 | X | X | X | | 0B0000h to 0BFFFFh | 058000h to 05FFFFh |
| | SA19 | 0 | 1 | 1 | 0 | 0 | X | X | X | | 0C0000h to 0CFFFFh | 060000h to 067FFFh |
| | SA20 | 0 | 1 | 1 | 0 | 1 | X | X | X | | 0D0000h to 0DFFFFh | 068000h to 06FFFFh |
| | SA21 | 0 | 1 | 1 | 1 | 0 | X | X | X | | 0E0000h to 0EFFFFh | 070000h to 077FFFh |
| SA22 | 0 | 1 | 1 | 1 | 1 | X | X | X | | 0F0000h to 0FFFFFh | 078000h to 07FFFFh | |
| Bank 2 | SA23 | 1 | 0 | 0 | 0 | 0 | X | X | X | 100000h to 10FFFFh | 080000h to 087FFFh | |
| | SA24 | 1 | 0 | 0 | 0 | 1 | X | X | X | 110000h to 11FFFFh | 088000h to 08FFFFh | |
| | SA25 | 1 | 0 | 0 | 1 | 0 | X | X | X | 120000h to 12FFFFh | 090000h to 097FFFh | |
| | SA26 | 1 | 0 | 0 | 1 | 1 | X | X | X | 130000h to 13FFFFh | 098000h to 09FFFFh | |
| | SA27 | 1 | 0 | 1 | 0 | 0 | X | X | X | 140000h to 14FFFFh | 0A0000h to 0A7FFFh | |
| | SA28 | 1 | 0 | 1 | 0 | 1 | X | X | X | 150000h to 15FFFFh | 0A8000h to 0AFFFFh | |
| | SA29 | 1 | 0 | 1 | 1 | 0 | X | X | X | 160000h to 16FFFFh | 0B0000h to 0B7FFFh | |
| | SA30 | 1 | 0 | 1 | 1 | 1 | X | X | X | 170000h to 17FFFFh | 0B8000h to 0BFFFFh | |
| | SA31 | 1 | 1 | 0 | 0 | 0 | X | X | X | 180000h to 18FFFFh | 0C0000h to 0C7FFFh | |
| | SA32 | 1 | 1 | 0 | 0 | 1 | X | X | X | 190000h to 19FFFFh | 0C8000h to 0CFFFFh | |
| | SA33 | 1 | 1 | 0 | 1 | 0 | X | X | X | 1A0000h to 1AFFFFh | 0D0000h to 0D7FFFh | |
| | SA34 | 1 | 1 | 0 | 1 | 1 | X | X | X | 1B0000h to 1BFFFFh | 0D8000h to 0DFFFFh | |
| | SA35 | 1 | 1 | 1 | 0 | 0 | X | X | X | 1C0000h to 1CFFFFh | 0E0000h to 0E7FFFh | |
| | SA36 | 1 | 1 | 1 | 0 | 1 | X | X | X | 1D0000h to 1DFFFFh | 0E8000h to 0EFFFFh | |
| | SA37 | 1 | 1 | 1 | 1 | 0 | X | X | X | 1E0000h to 1EFFFFh | 0F0000h to 0F7FFFh | |
| | SA38 | 1 | 1 | 1 | 1 | 1 | X | X | X | 1F0000h to 1FFFFFh | 0F8000h to 0FFFFFh | |

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Sector Group Addresses Table (Top Boot Block)

| Sector Group | A ₁₉ | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | Sectors |
|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------|
| SGA0 | 0 | 0 | 0 | 0 | 0 | X | X | X | SA0 |
| SGA1 | 0 | 0 | 0 | 0 | 1 | X | X | X | SA1 to SA3 |
| | 0 | 0 | 0 | 1 | 0 | X | X | X | |
| | 0 | 0 | 0 | 1 | 1 | X | X | X | |
| SGA2 | 0 | 0 | 1 | X | X | X | X | X | SA4 to SA7 |
| SGA3 | 0 | 1 | 0 | X | X | X | X | X | SA8 to SA11 |
| SGA4 | 0 | 1 | 1 | X | X | X | X | X | SA12 to SA15 |
| SGA5 | 1 | 0 | 0 | X | X | X | X | X | SA16 to SA19 |
| SGA6 | 1 | 0 | 1 | X | X | X | X | X | SA20 to SA23 |
| SGA7 | 1 | 1 | 0 | X | X | X | X | X | SA24 to SA27 |
| SGA8 | 1 | 1 | 1 | 0 | 0 | X | X | X | SA28 to SA30 |
| | 1 | 1 | 1 | 0 | 1 | X | X | X | |
| | 1 | 1 | 1 | 1 | 0 | X | X | X | |
| SGA9 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | SA31 |
| SGA10 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | SA32 |
| SGA11 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | SA33 |
| SGA12 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | SA34 |
| SGA13 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | SA35 |
| SGA14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | SA36 |
| SGA15 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | SA37 |
| SGA16 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | SA38 |

Sector Group Addresses Table (Bottom Boot Block)

| Sector Group | A ₁₉ | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | Sectors |
|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------|
| SGA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SA0 |
| SGA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SA1 |
| SGA2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | SA2 |
| SGA3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | SA3 |
| SGA4 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | SA4 |
| SGA5 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SA5 |
| SGA6 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | SA6 |
| SGA7 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | SA7 |
| SGA8 | 0 | 0 | 0 | 0 | 1 | X | X | X | SA8 to SA10 |
| | 0 | 0 | 0 | 1 | 0 | X | X | X | |
| | 0 | 0 | 0 | 1 | 1 | X | X | X | |
| SGA9 | 0 | 0 | 1 | X | X | X | X | X | SA11 to SA14 |
| SGA10 | 0 | 1 | 0 | X | X | X | X | X | SA15 to SA18 |
| SGA11 | 0 | 1 | 1 | X | X | X | X | X | SA19 to SA22 |
| SGA12 | 1 | 0 | 0 | X | X | X | X | X | SA23 to SA26 |
| SGA13 | 1 | 0 | 1 | X | X | X | X | X | SA27 to SA30 |
| SGA14 | 1 | 1 | 0 | X | X | X | X | X | SA31 to SA34 |
| SGA15 | 1 | 1 | 1 | 0 | 0 | X | X | X | SA35 to SA37 |
| | 1 | 1 | 1 | 0 | 1 | X | X | X | |
| | 1 | 1 | 1 | 1 | 0 | X | X | X | |
| SGA16 | 1 | 1 | 1 | 1 | 1 | X | X | X | SA38 |

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Flash Memory Autoselect Codes Table

| Type | | A ₁₉ to A ₁₂ | A ₆ | A ₁ | A ₀ | A ₋₁ *1 | Code (HEX) | |
|----------------------|----------------------------------|------------------------------------|-----------------|-----------------|-----------------|--------------------|-----------------|-------|
| Manufacturer's Code | | X | V _{IL} | V _{IL} | V _{IL} | V _{IL} | 04h | |
| Device Code | Top Boot Block Bank Size=1 | Byte | X | V _{IL} | V _{IL} | V _{IH} | V _{IL} | 36h |
| | | Word | | | | | X | 2236h |
| | Bottom Boot Block Bank Size=1 | Byte | X | V _{IL} | V _{IL} | V _{IH} | V _{IL} | 39 |
| | | Word | | | | | X | 2239h |
| | Top Boot Block Bank Size=2 | Byte | X | V _{IL} | V _{IL} | V _{IH} | V _{IL} | 2D |
| | | Word | | | | | X | 222Dh |
| | Bottom Boot Block Bank Size=2 | Byte | X | V _{IL} | V _{IL} | V _{IH} | V _{IL} | 2E |
| | | Word | | | | | X | 222Eh |
| | Top Boot Block Bank Size=3 | Byte | X | V _{IL} | V _{IL} | V _{IH} | V _{IL} | 28h |
| | | Word | | | | | X | 2228h |
| | Bottom Boot Block Bank Size=3 | Byte | X | V _{IL} | V _{IL} | V _{IH} | V _{IL} | 2Bh |
| | | Word | | | | | X | 222Bh |
| | Top Boot Block Bank Size=4 | Byte | X | V _{IL} | V _{IL} | V _{IH} | V _{IL} | 33h |
| | | Word | | | | | X | 2233h |
| | Bottom Boot Block Bank Size=4 | Byte | X | V _{IL} | V _{IL} | V _{IH} | V _{IL} | 35 |
| | | Word | | | | | X | 2235h |
| Sector Group protect | | Sector Group Address | V _{IL} | V _{IH} | V _{IL} | V _{IL} | 01h*2 | |

*1: A₋₁ is for Byte mode.

*2: Output 01h at protected sector address and output 00h at unprotected sector address.

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Flash Memory Command Definitions Table

| Command Sequence | | Bus Write Cycles Req'd | First Bus Write Cycle | | Second Bus Write Cycle | | Third Bus Write Cycle | | Fourth Bus Read/Write Cycle | | Fifth Bus Write Cycle | | Sixth Bus Write Cycle | |
|-------------------------------------|------|------------------------|-----------------------|------|------------------------|-----------|-----------------------|------|-----------------------------|------|-----------------------|------|-----------------------|------|
| | | | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data |
| Read/Reset *1 | | 1 | XXXh | F0h | — | — | — | — | — | — | — | — | — | — |
| Read/Reset *1 | Word | 3 | 555h | AAh | 2AAh | 55h | 555h | F0h | RA | RD | — | — | — | — |
| | Byte | | AAAh | | 555h | | AAAh | | | | | | | |
| Autoselect | Word | 3 | 555h | AAh | 2AAh | 55h | (BA) 555h | 90h | — | — | — | — | — | — |
| | Byte | | AAAh | | 555h | | (BA) AAAh | | | | | | | |
| Program | Word | 4 | 555h | AAh | 2AAh | 55h | 555h | A0h | PA | PD | — | — | — | — |
| | Byte | | AAAh | | 555h | | AAAh | | | | | | | |
| Chip Erase | Word | 6 | 555h | AAh | 2AAh | 55h | 555h | 80h | 555h | AAh | 2AAh | 55h | 555h | 10h |
| | Byte | | AAAh | | 555h | | AAAh | | 555h | | AAAh | | | |
| Sector Erase | Word | 6 | 555h | AAh | 2AAh | 55h | 555h | 80h | 555h | AAh | 2AAh | 55h | SA | 30h |
| | Byte | | AAAh | | 555h | | AAAh | | 555h | | AAAh | | | |
| Sector Erase Suspend | | 1 | BA | B0h | — | — | — | — | — | — | — | — | — | — |
| Sector Erase Resume | | 1 | BA | 30h | — | — | — | — | — | — | — | — | — | — |
| Set to Fast Mode | Word | 3 | 555h | AAh | 2AAh | 55h | 555h | 20h | — | — | — | — | — | — |
| | Byte | | AAAh | | 555h | | AAAh | | | | | | | |
| Fast Program*2 | Word | 2 | XXXh | A0h | PA | PD | — | — | — | — | — | — | — | — |
| | Byte | | — | — | — | — | — | — | — | — | — | — | — | — |
| Reset from Fast Mode *2 | Word | 2 | BA | 90h | XXXh | F0h *6 | — | — | — | — | — | — | — | — |
| | Byte | | — | — | — | — | — | — | — | — | — | — | — | — |
| Extended Sector Group Protection *3 | Word | 4 | XXXh | 60h | SPA | 60h | SPA | 40h | SPA | SD | — | — | — | — |
| | Byte | | — | — | — | — | — | — | — | — | — | — | — | — |
| Query *4 | Word | 1 | 55h | 98h | — | — | — | — | — | — | — | — | — | — |
| | Byte | | AAh | — | — | — | — | — | — | — | — | — | — | — |
| HiddenROM Entry | Word | 3 | 555h | AAh | 2AAh | 55h | 555h | 88h | — | — | — | — | — | — |
| | Byte | | AAAh | | 555h | | AAAh | | | | | | | |
| HiddenROM Program *5 | Word | 4 | 555h | AAh | 2AAh | 55h | 555h | A0h | PA | PD | — | — | — | — |
| | Byte | | AAAh | | 555h | | AAAh | | | | | | | |
| HiddenROM Erase *5 | Word | 6 | 555h | AAh | 2AAh | 55h | 555h | 80h | 555h | AAh | 2AAh | 55h | HRA | 30h |
| | Byte | | AAAh | | 555h | | AAAh | | 555h | | AAAh | | | |
| HiddenROM Exit *5 | Word | 4 | 555h | AAh | 2AAh | 55h | (HRBA) 555h | 90h | XXXh | 00h | — | — | — | — |
| | Byte | | AAAh | | 555h | | (HRBA) AAAh | | | | | | | |

MB84VD2108XEM/2109XEM-70

• Read Only Operations Characteristics (Flash)

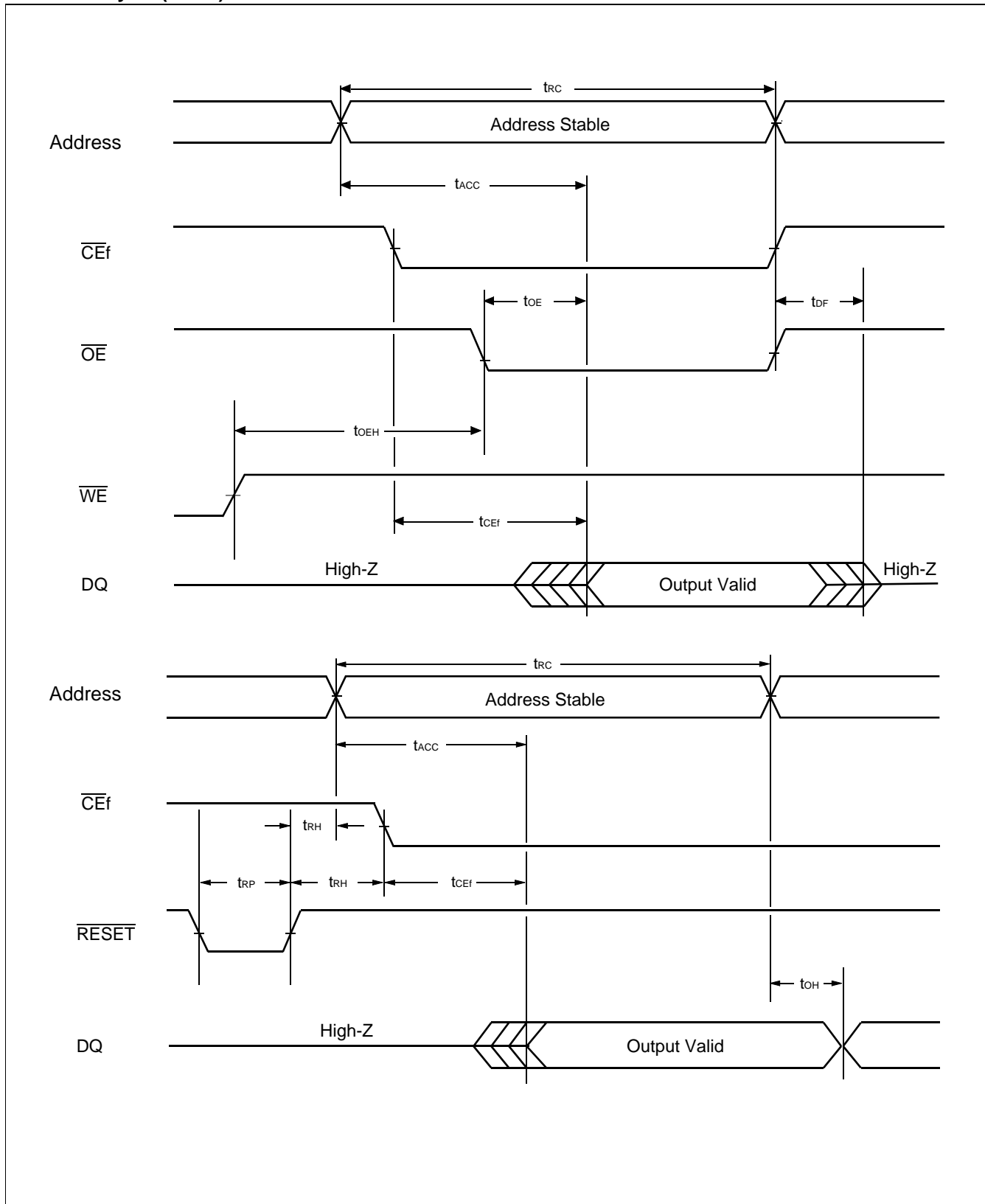
| Parameter | Symbol | | Test Setup | Value* | | Unit |
|---|-------------------|--------------------|---|--------|-----|------|
| | JEDEC | Standard | | Min | Max | |
| Read Cycle Time | t _{AVAV} | t _{RC} | — | 70 | — | ns |
| Address to Output Delay | t _{AVQV} | t _{ACC} | $\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$ | — | 70 | ns |
| Chip Enable to Output Delay | t _{ELQV} | t _{CEf} | $\overline{OE} = V_{IL}$ | — | 70 | ns |
| Output Enable to Output Delay | t _{GLQV} | t _{OE} | — | — | 30 | ns |
| Chip Enable to Output High-Z | t _{EHQZ} | t _{DF} | — | — | 25 | ns |
| Output Enable to Output High-Z | t _{GHQZ} | t _{DF} | — | — | 25 | ns |
| Output Hold Time From Addresses, $\overline{CE}f$ or \overline{OE} , Whichever Occurs First | t _{AXQX} | t _{OH} | — | 0 | — | ns |
| \overline{RESET} Pin Low to Read Mode | — | t _{READY} | — | — | 20 | μs |

* : Test Conditions

Output Load : 1 TTL gate and 30 pF
 Input rise and fall times: 5 ns
 Input pulse levels : 0.0 V to 3.0 V
 Timing measurement reference level
 Input : 1.5 V
 Output : 1.5 V

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• Read Cycle (Flash)



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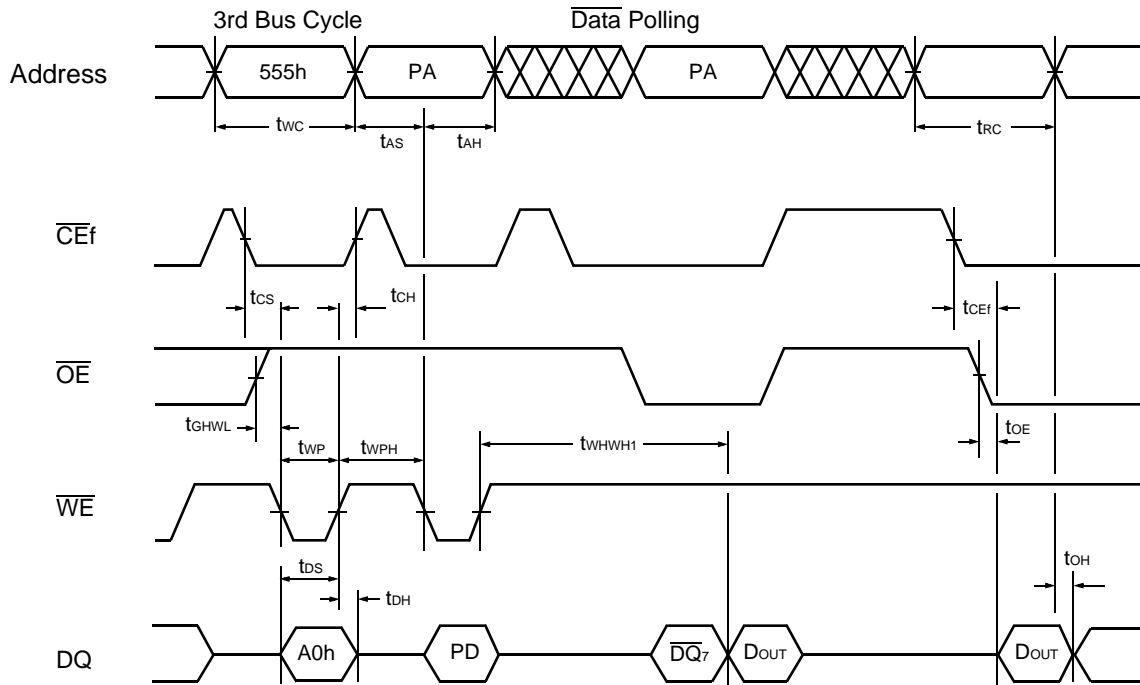
• Erase/Program Operations (Flash)

| Parameter | Symbol | | Value | | | Unit |
|---|-------------------------|--------------------|-------|-----|-----|------|
| | JEDEC | Standard | Min | Typ | Max | |
| Write Cycle Time | t _{AVAV} | t _{WC} | 70 | — | — | ns |
| Address Setup Time (\overline{WE} to Addr.) | t _{AVWL} | t _{AS} | 0 | — | — | ns |
| Address Setup Time to \overline{CEf} Low During Toggle Bit Polling | — | t _{ASO} | 12 | — | — | ns |
| Address Hold Time (\overline{WE} to Addr.) | t _{WLAX} | t _{AH} | 45 | — | — | ns |
| Address Hold Time from \overline{CEf} or \overline{OE} High During Toggle Bit Polling | — | t _{AHT} | 0 | — | — | ns |
| Data Setup Time | t _{DVWH} | t _{DS} | 30 | — | — | ns |
| Data Hold Time | t _{WDHX} | t _{DH} | 0 | — | — | ns |
| Output Enable Setup Time | — | t _{OES} | 0 | — | — | ns |
| Output Enable Hold Time | Read | — | 0 | — | — | ns |
| | Toggle and Data Polling | | | | | |
| \overline{CEf} High During Toggle Bit Polling | — | t _{CEPH} | 20 | — | — | ns |
| \overline{OE} High During Toggle Bit Polling | — | t _{OEPH} | 20 | — | — | ns |
| Read Recover Time Before Write (\overline{OE} to \overline{CEf}) | t _{GHEL} | t _{GHEL} | 0 | — | — | ns |
| Read Recover Time Before Write (\overline{OE} to \overline{WE}) | t _{GHWL} | t _{GHWL} | 0 | — | — | ns |
| \overline{WE} Setup Time (\overline{CEf} to \overline{WE}) | t _{WLWL} | t _{WS} | 0 | — | — | ns |
| \overline{CEf} Setup Time (\overline{WE} to \overline{CEf}) | t _{ELWL} | t _{CS} | 0 | — | — | ns |
| \overline{WE} Hold Time (\overline{CEf} to \overline{WE}) | t _{EHWH} | t _{WH} | 0 | — | — | ns |
| \overline{CEf} Hold Time (\overline{WE} to \overline{CEf}) | t _{WHEH} | t _{CH} | 0 | — | — | ns |
| Write Pulse Width | t _{WLWH} | t _{WP} | 35 | — | — | ns |
| \overline{CEf} Pulse Width | t _{LELH} | t _{CP} | 35 | — | — | ns |
| Write Pulse Width High | t _{WHWL} | t _{WPH} | 25 | — | — | ns |
| \overline{CEf} Pulse Width High | t _{EHEL} | t _{CPH} | 25 | — | — | ns |
| Byte Programming Operation | t _{WHWH1} | t _{WHWH1} | — | 8 | — | μs |
| Word Programming Operation | | | — | 16 | — | μs |
| Sector Erase Operation *1 | t _{WHWH2} | t _{WHWH2} | — | 1 | — | s |
| V _{ccf} Setup Time | — | t _{VCS} | 50 | — | — | μs |
| Voltage Transition Time *2 | — | t _{VLHT} | 4 | — | — | μs |
| Rise Time to V _{ID} *2 | — | t _{VIDR} | 500 | — | — | ns |
| Rise Time to V _{ACC} | — | t _{VACCR} | 500 | — | — | ns |
| Recover Time from RY/ \overline{BY} | — | t _{RB} | 0 | — | — | ns |
| RESET Pulse Width | — | t _{RP} | 500 | — | — | ns |
| Delay Time from Embedded Output Enable | — | t _{EOE} | — | — | 70 | ns |
| RESET Hold Time Before Read | — | t _{RH} | 200 | — | — | ns |
| Program/Erase Valid to RY/ \overline{BY} Delay | — | t _{BUSY} | — | — | 90 | ns |
| Erase Time-out Time *3 | — | t _{TOW} | 50 | — | — | μs |
| Erase Suspend Transition Time *4 | — | t _{SPD} | — | — | 20 | μs |

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- *1 : This does not include the preprogramming time.
- *2 : This timing is for Sector Protection Operation.
- *3 : The time between writes must be less than “ t_{row} ” otherwise that command will not be accepted and erasure will start. A time-out or “ t_{row} ” from the rising edge of last \overline{CE} or \overline{WE} whichever happens first will initiate the execution of the Sector Erase command(s).
- *4 : When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of “ t_{SPD} ” to suspend the erase operation.

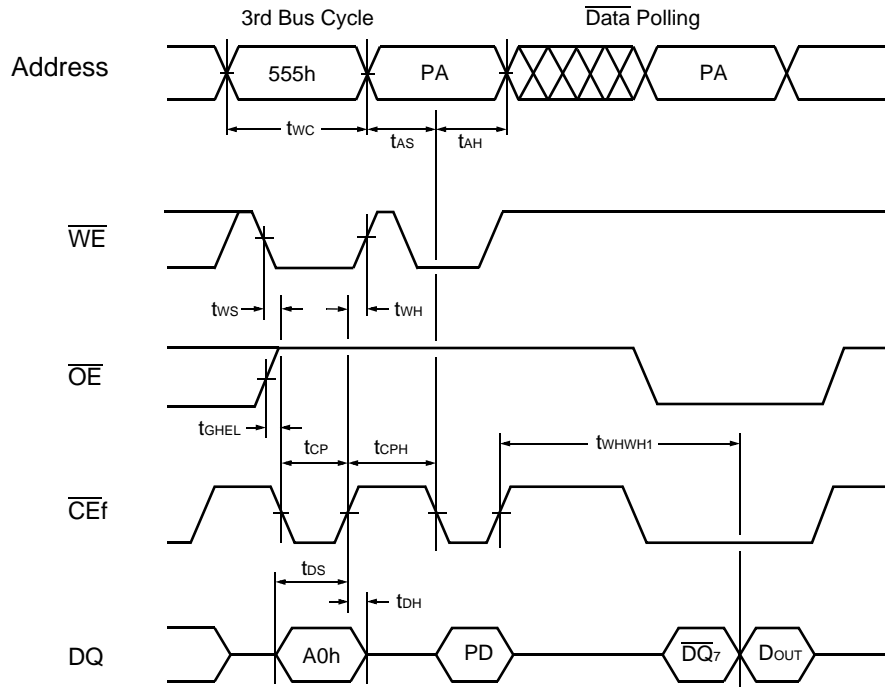
• Write Cycle (\overline{WE} control) (Flash)



- Notes :
- PA is address of the memory location to be programmed.
 - PD is data to be programmed at byte address.
 - \overline{DQ}_7 is the output of the complement of the data written to the device.
 - D_{OUT} is the output of the data written to the device.
 - Figure indicates last two bus cycles out of four bus cycle sequence.
 - These waveforms are for the x16 mode. (The addresses differ from x8 mode.)

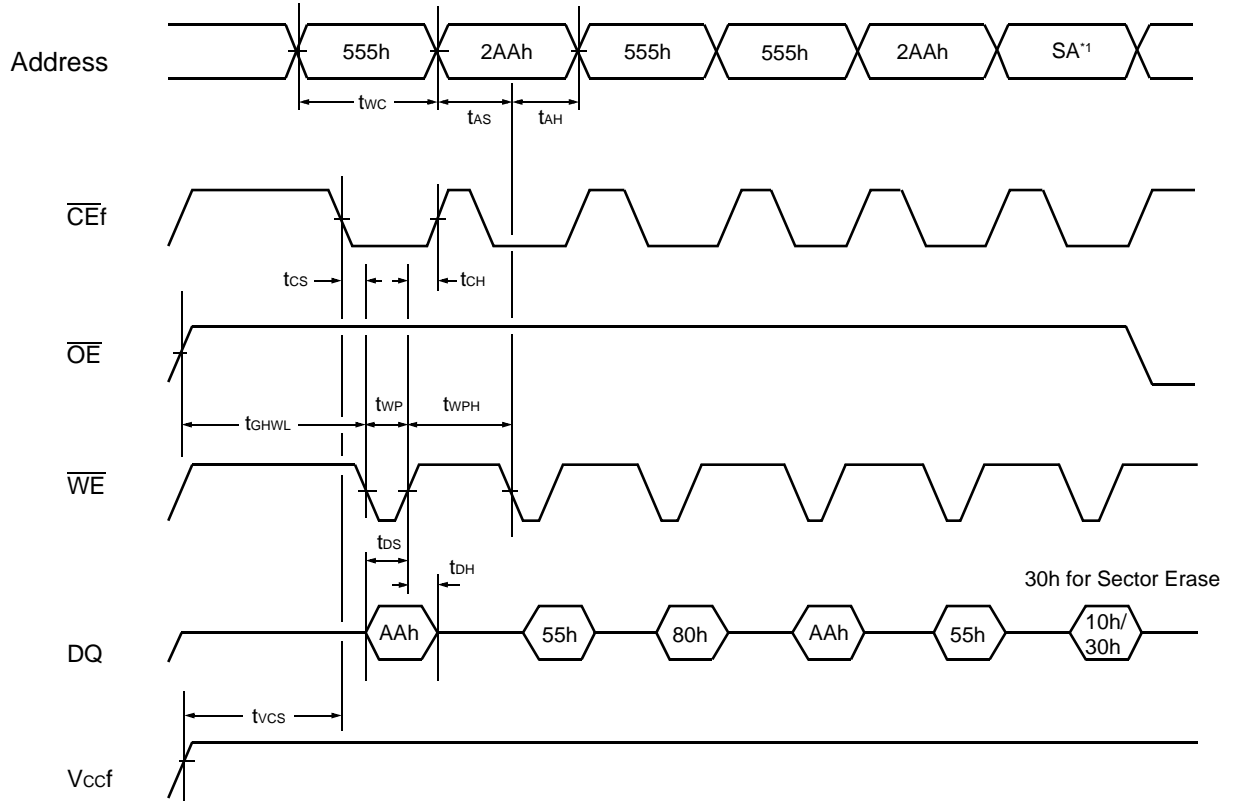
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• Write Cycle ($\overline{\text{CEf}}$ control) (Flash)



- Notes :
- PA is address of the memory location to be programmed.
 - PD is data to be programmed at byte address.
 - $\overline{\text{DQ}}_7$ is the output of the complement of the data written to the device.
 - D_{OUT} is the output of the data written to the device.
 - Figure indicates last two bus cycles out of four bus cycle sequence.
 - These waveforms are for the x16 mode. (The addresses differ from x8 mode.)

• AC Waveforms Chip/Sector Erase Operations (Flash)

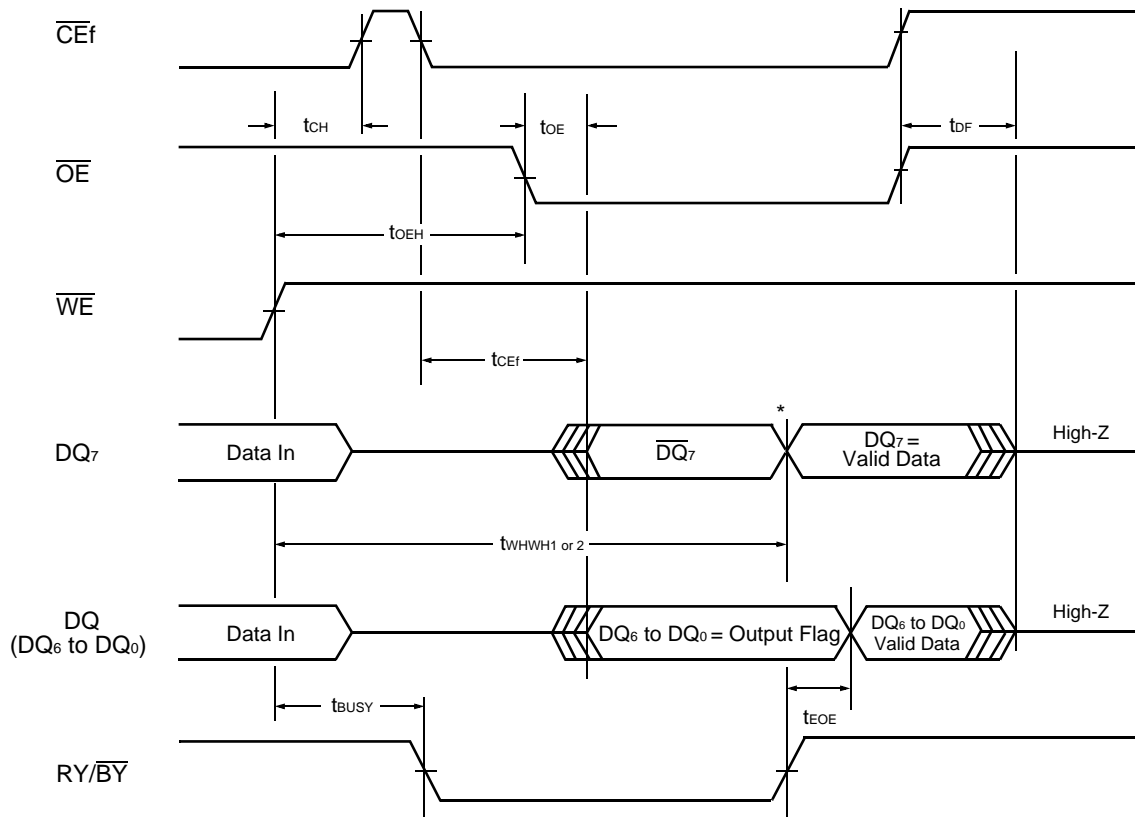


* : SA is the sector address for Sector Erase. Addresses = 555h for Chip Erase.

Note : These waveform are for the x16 mode. (The addresses differ from x8 mode.)

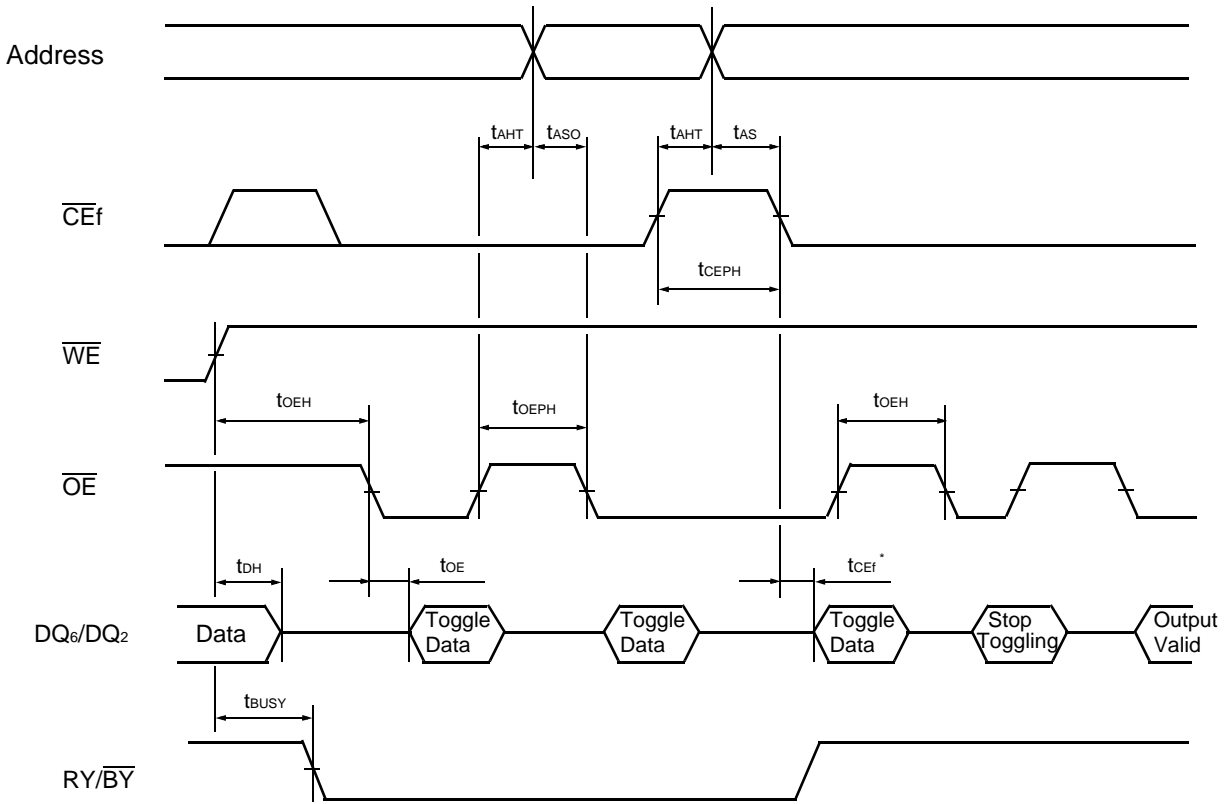
MB84VD2108XEM/2109XEM-70

• AC Waveforms for Data Polling during Embedded Algorithm Operations (Flash)



* : DQ_7 = Valid Data (The device has completed the Embedded operation.)

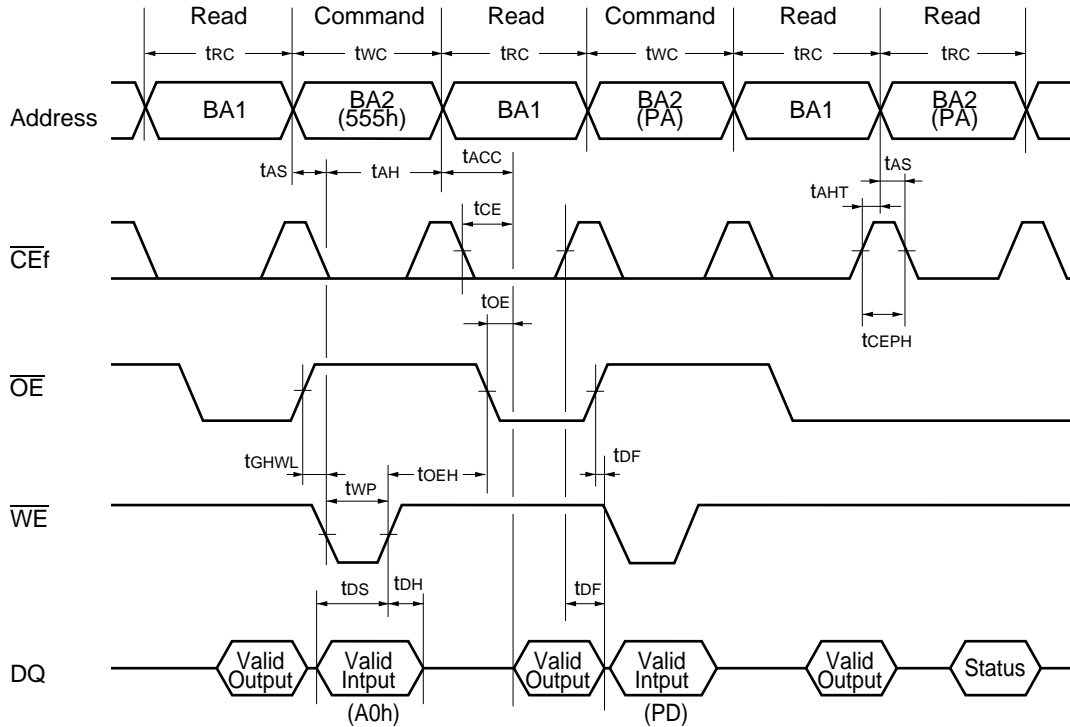
• AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)



* : DQ_6 stops toggling (The device has completed the Embedded operation).

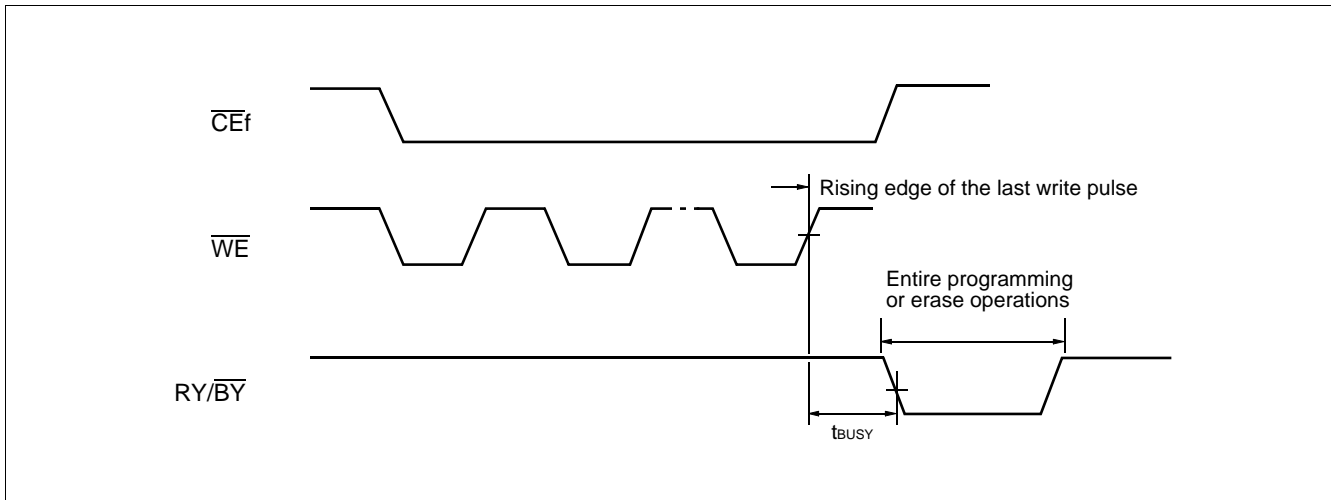
MB84VD2108XEM/2109XEM-70

• Bank-to-bank Read/Write Timing Diagram (Flash)

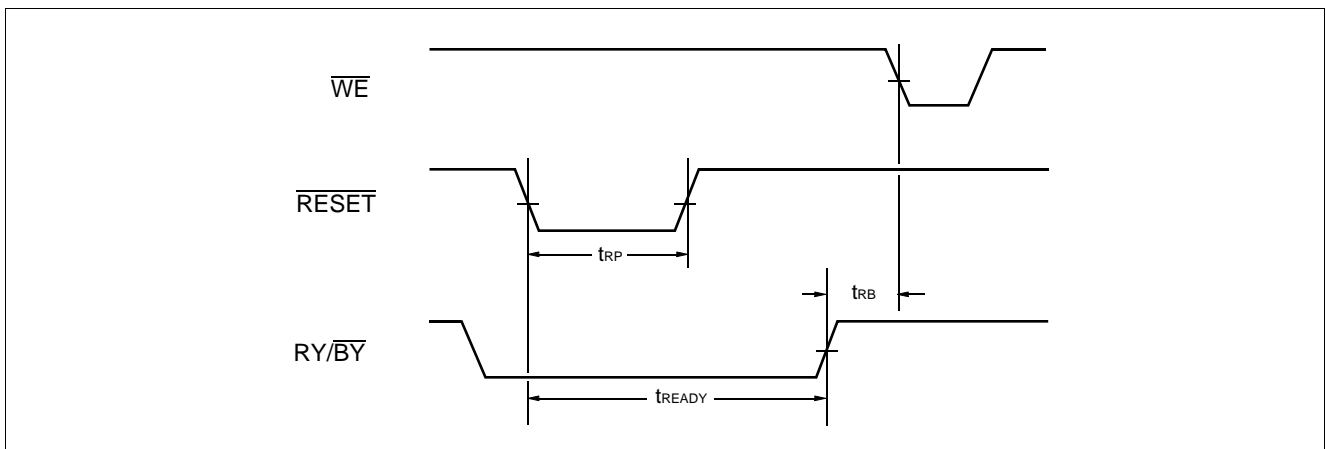


Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
 BA1: Address of Bank 1.
 BA2: Address of Bank 2.

- $\overline{RY}/\overline{BY}$ Timing Diagram during Write/Erase Operations (Flash)

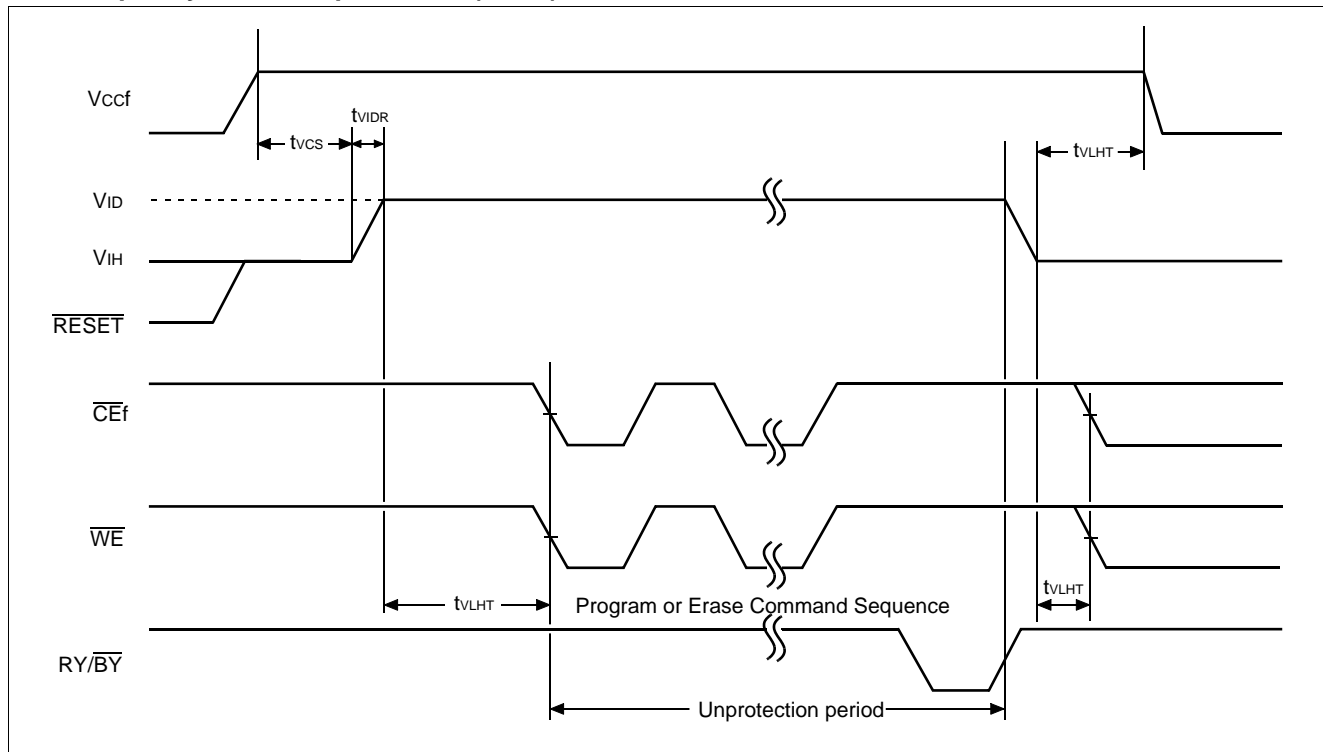


- \overline{RESET} , $\overline{RY}/\overline{BY}$ Timing Diagram (Flash)

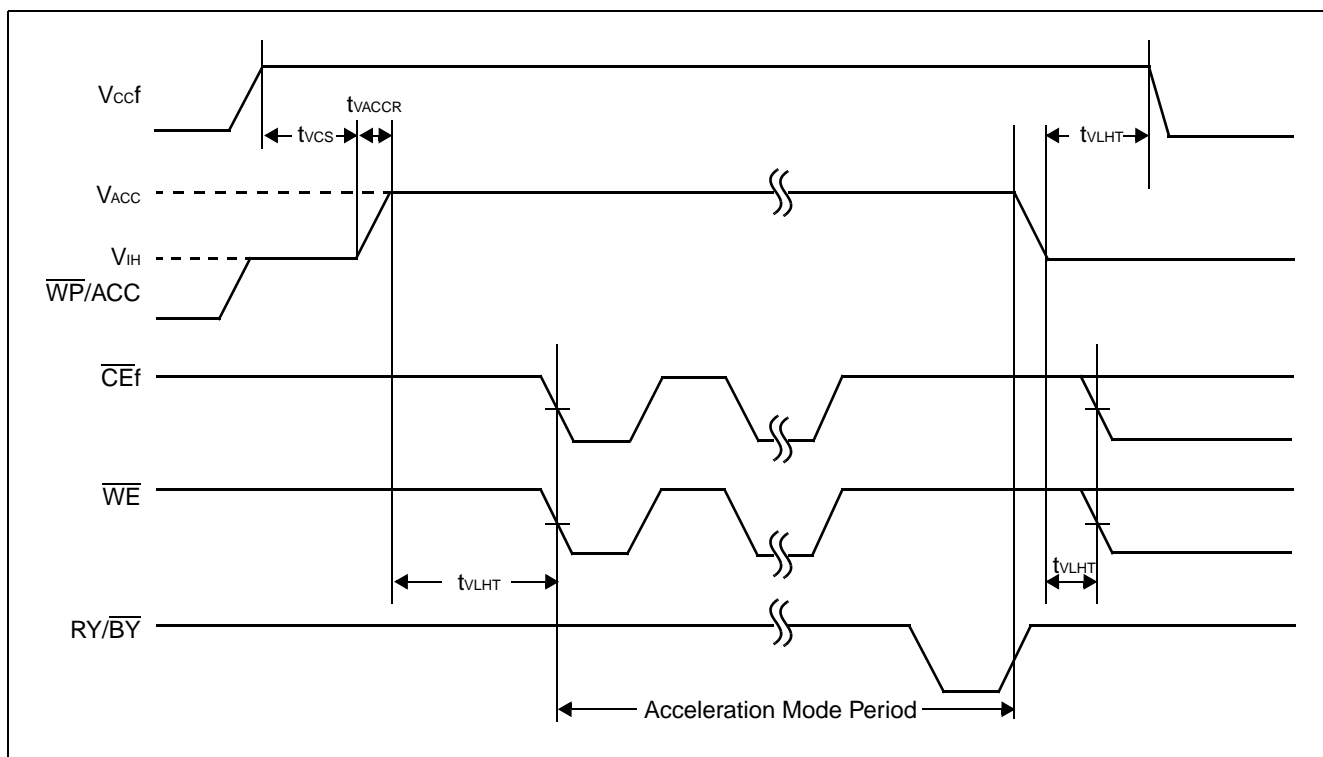


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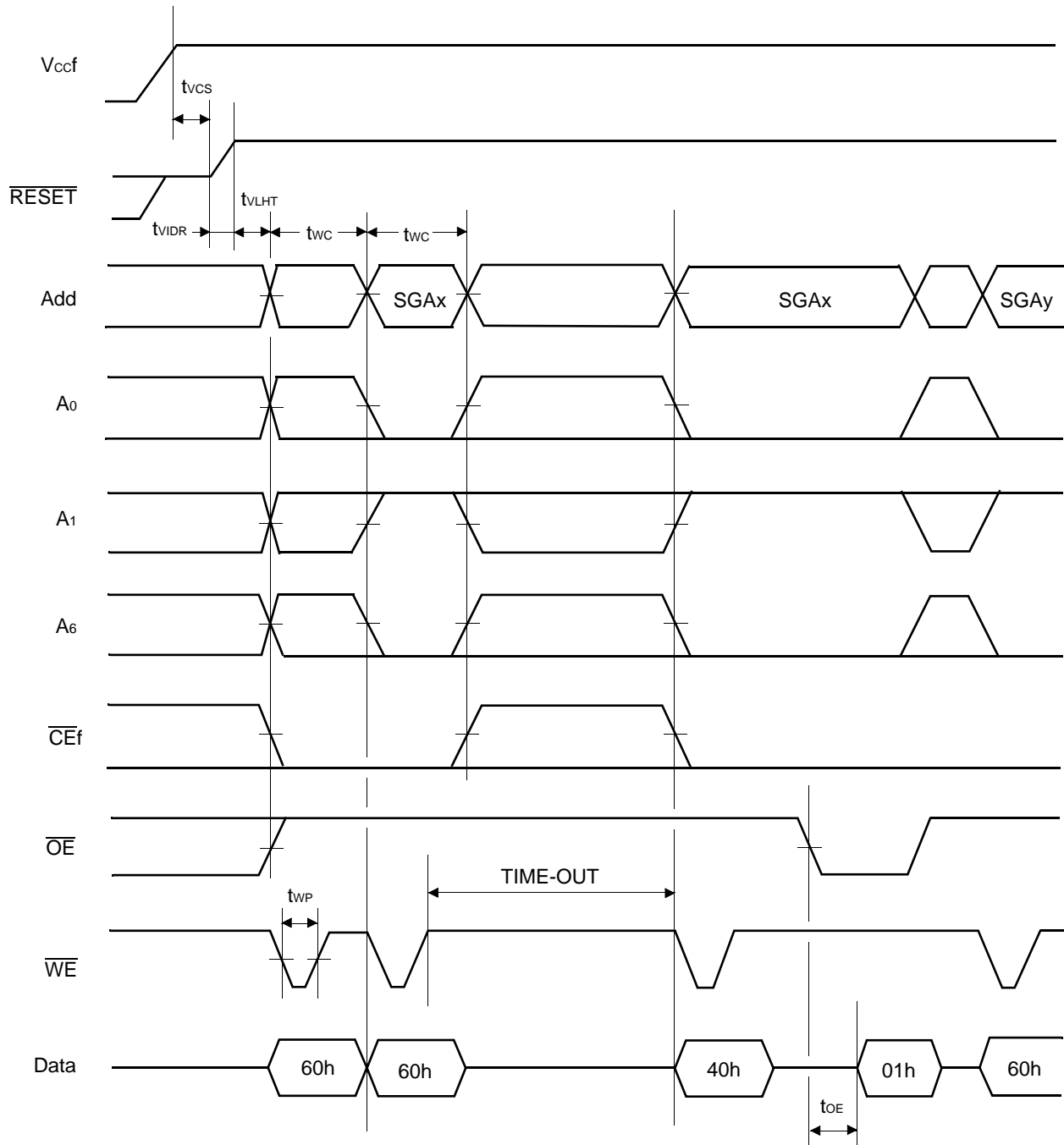
• Temporary Sector Unprotection (Flash)



• Acceleration Mode Timing Diagram (Flash)



• Extended Sector Protection (Flash)



$SGAx$: Sector Group Address to be protected
 $SGAy$: Next Group Sector Address to be protected
 TIME-OUT : Time-Out window = 250 μs (Min)

MB84VD2108XEM/2109XEM-70

2. Erase and Programming Performance (Flash)

| Parameter | Limit | | | Unit | Comment |
|-----------------------|---------|-----|-----|-------|--|
| | Min | Typ | Max | | |
| Sector Erase Time | — | 1 | 10 | s | Excludes programming time prior to erasure |
| Byte Programming Time | — | 8 | 300 | μs | Excludes system-level overhead |
| Word Programming Time | — | 16 | 360 | μs | Excludes system-level overhead |
| Chip Programming Time | — | — | 50 | s | Excludes system-level overhead |
| Erase/Program Cycle | 100,000 | — | — | cycle | |

■ 2M SRAM CHARACTERISTICS for MCP

1. AC Characteristics

• Read Cycle (SRAM)

| Parameter | Symbol | Value | | Unit |
|---|-----------|-------|-----|------|
| | | Min | Max | |
| Read Cycle Time | t_{RC} | 70 | — | ns |
| Address Access Time | t_{AA} | — | 70 | ns |
| Chip Enable ($\overline{CE1s}$) Access Time | t_{CO1} | — | 70 | ns |
| Chip Enable (CE2s) Access Time | t_{CO2} | — | 70 | ns |
| Output Enable Access Time | t_{OE} | — | 35 | ns |
| \overline{LB} , \overline{UB} to Output Valid | t_{BA} | — | 70 | ns |
| Chip Enable ($\overline{CE1s}$ Low and CE2s High) to Output Active | t_{COE} | 5 | — | ns |
| Output Enable Low to Output Active | t_{OEE} | 0 | — | ns |
| \overline{UB} , \overline{LB} Enable Low to Output Active | t_{BE} | 0 | — | ns |
| Chip Enable ($\overline{CE1s}$ High or CE2s Low) to Output High-Z | t_{OD} | — | 25 | ns |
| Output Enable High to Output High-Z | t_{ODO} | — | 25 | ns |
| \overline{UB} , \overline{LB} Output Enable to Output High-Z | t_{BD} | — | 25 | ns |
| Output Data Hold Time | t_{OH} | 10 | — | ns |

Note: Test Conditions

Output Load: 1 TTL gate and 30 pF

Input rise and fall times: 5 ns

Input pulse levels: 0.0 V to V_{CCS}

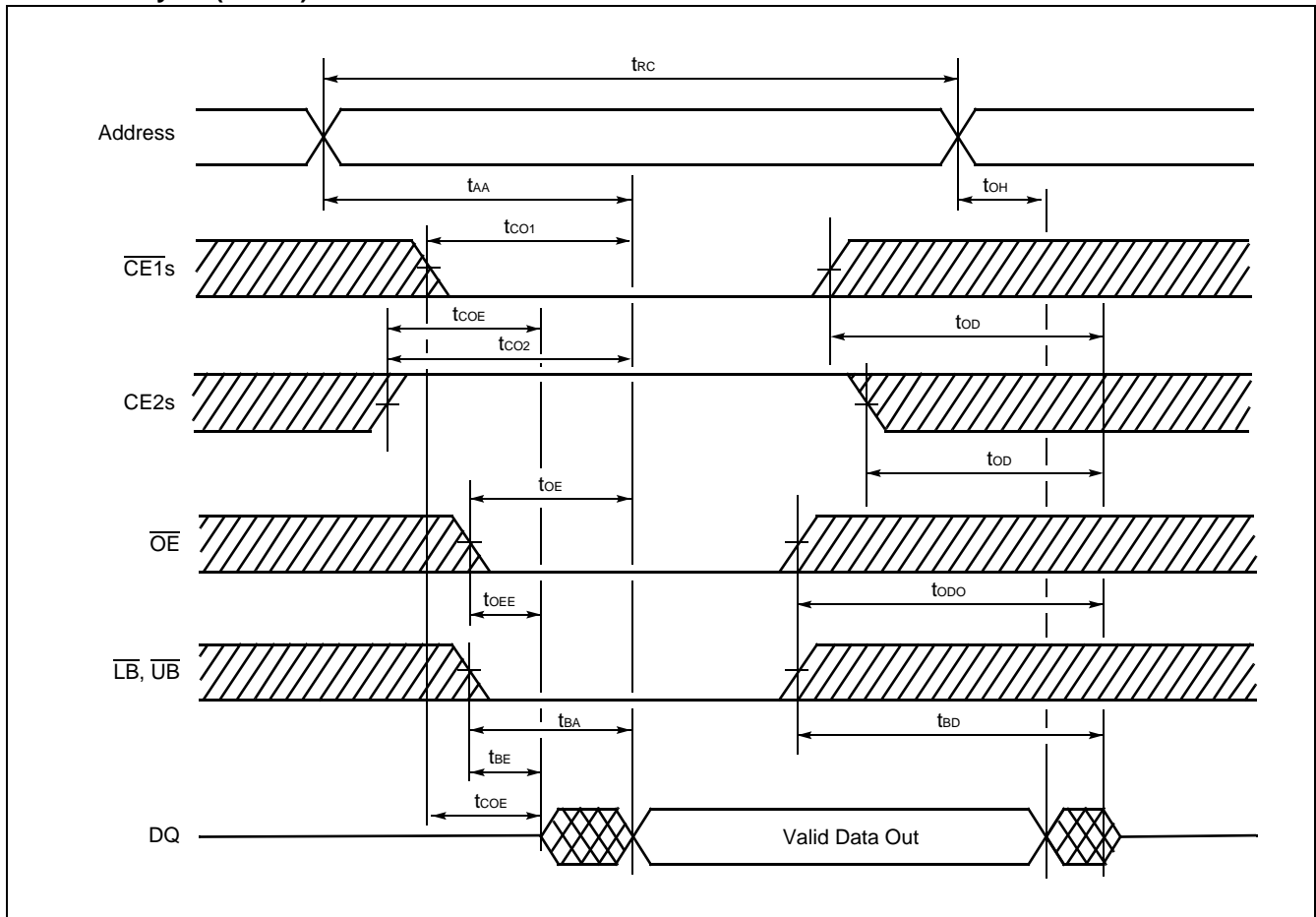
Timing measurement reference level

Input: $0.5 \times V_{CCS}$

Output: $0.5 \times V_{CCS}$

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• Read Cycle (SRAM)



Note : \overline{WE} remains "H" for the read cycle.

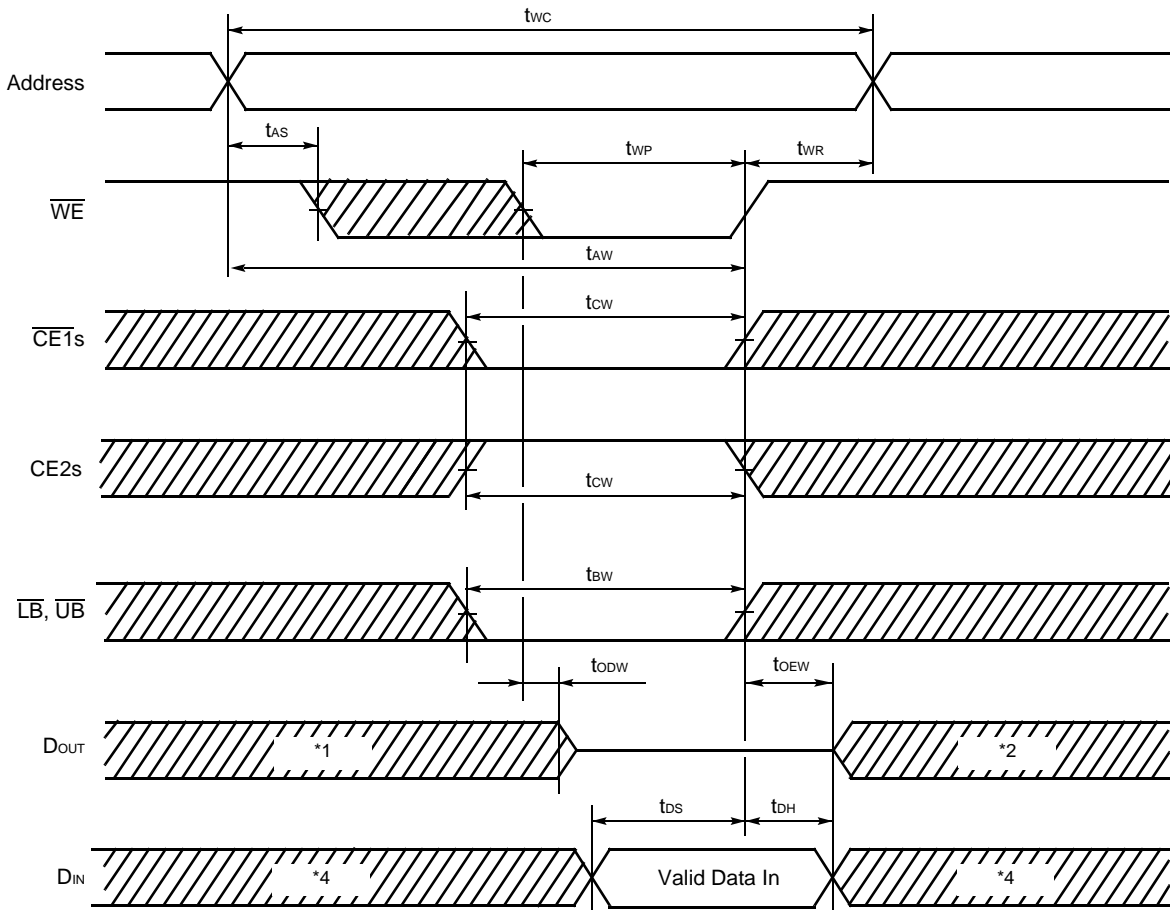
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• Write Cycle (SRAM)

| Parameter | Symbol | Value | | Unit |
|---|------------------|-------|-----|------|
| | | Min | Max | |
| Write Cycle Time | t _{WC} | 70 | — | ns |
| Write Pulse Width | t _{WP} | 50 | — | ns |
| Chip Enable to End of Write | t _{CW} | 55 | — | ns |
| Address valid to End of Write | t _{AW} | 55 | — | ns |
| \overline{UB} , \overline{LB} to End of Write | t _{BW} | 55 | — | ns |
| Address Setup Time | t _{AS} | 0 | — | ns |
| Write Recovery Time | t _{WR} | 0 | — | ns |
| \overline{WE} Low to Output High-Z | t _{ODW} | — | 25 | ns |
| \overline{WE} High to Output Active | t _{OEW} | 0 | — | ns |
| Data Setup Time | t _{DS} | 30 | — | ns |
| Data Hold Time | t _{DH} | 0 | — | ns |

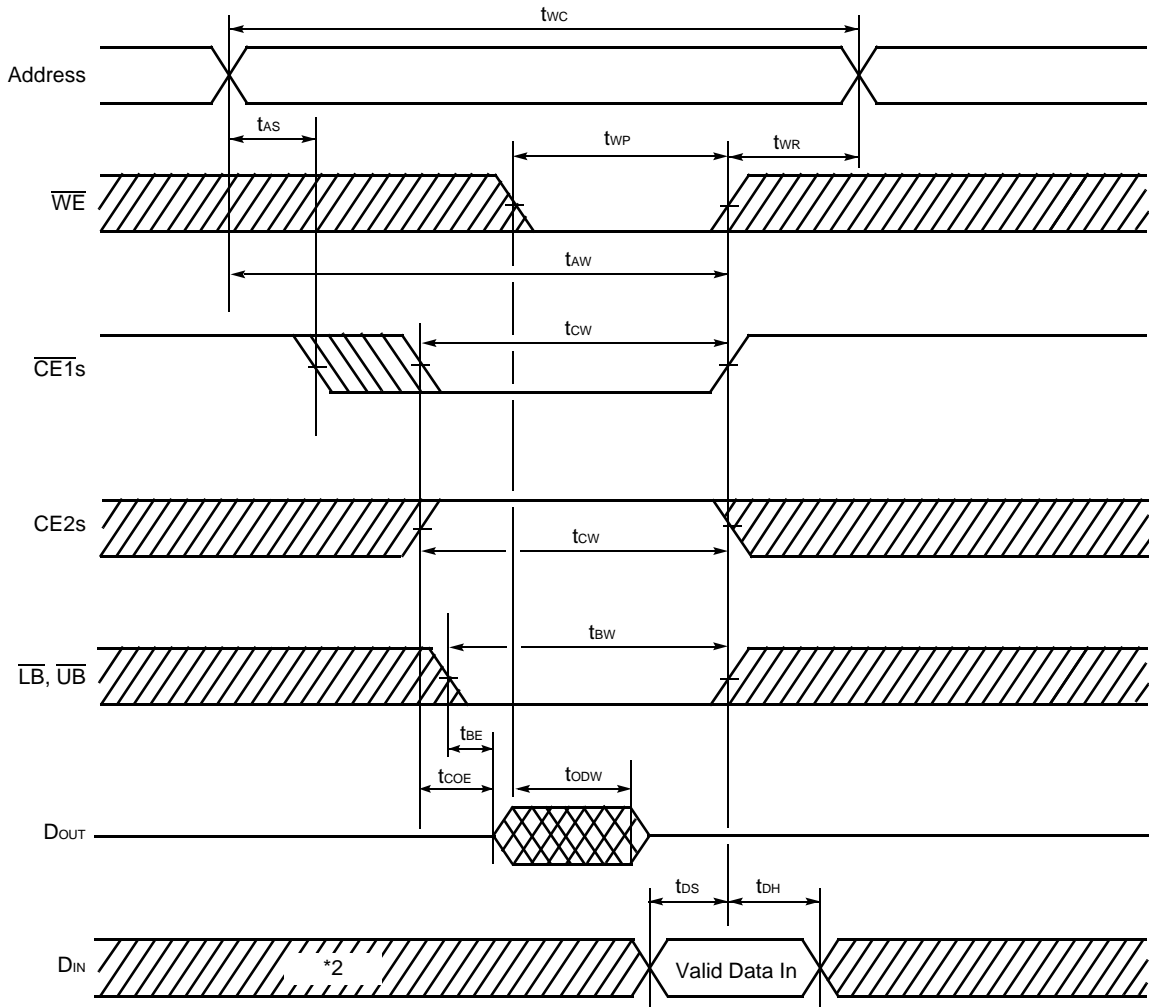
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• Write Cycle *3 (\overline{WE} control) (SRAM)



- *1 : If $\overline{CE1s}$ goes "L" (or $\overline{CE2s}$ goes "H") coincident with or after \overline{WE} goes "L", the output will remain at High-Z.
- *2 : If $\overline{CE1s}$ goes "H" (or $\overline{CE2s}$ goes "L") coincident with or before \overline{WE} goes "H", the output will remain at High-Z.
- *3 : If \overline{OE} is "H" during the write cycle, the outputs will remain at High-Z.
- *4 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

• Write Cycle *1 ($\overline{CE1s}$ control) (SRAM)

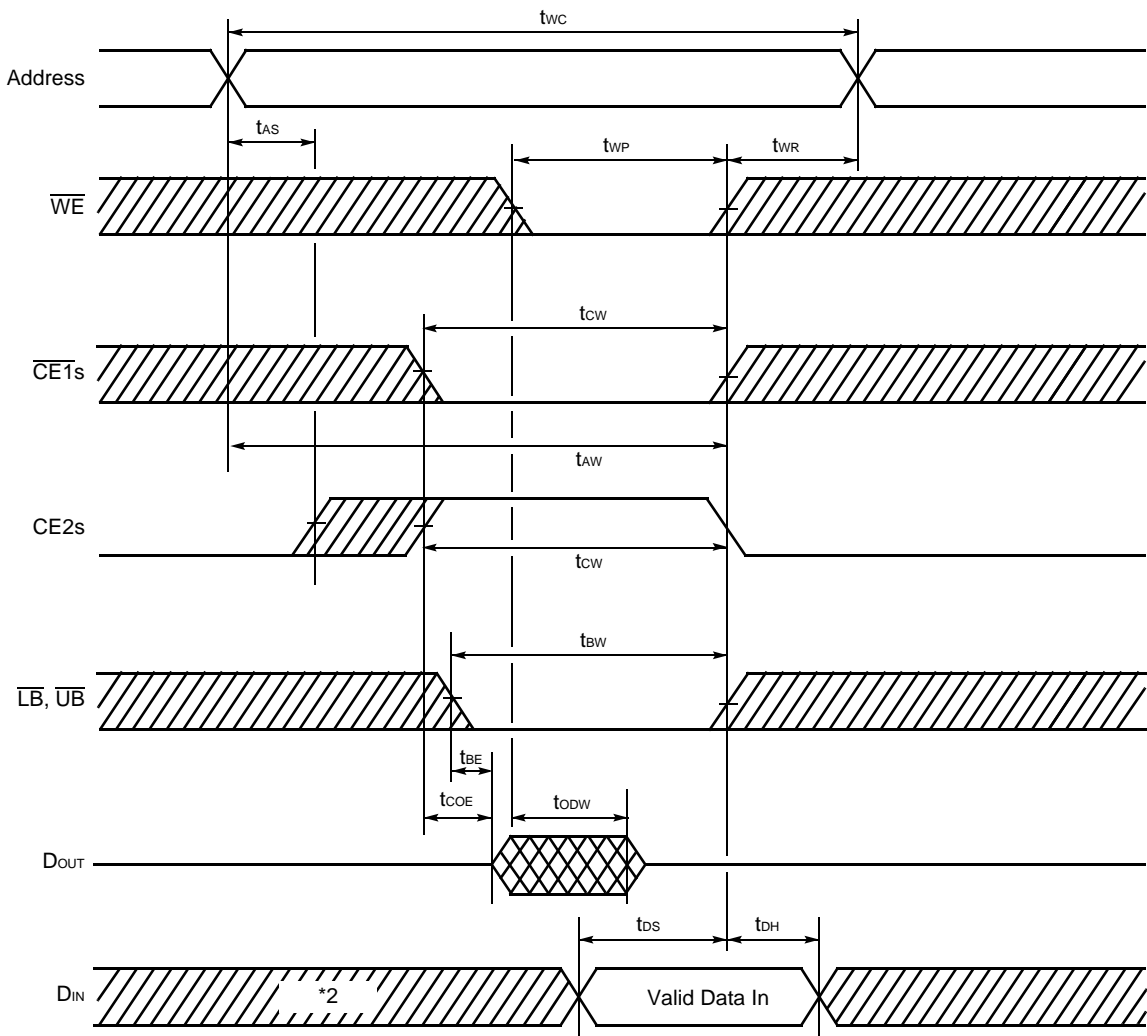


*1 : If \overline{OE} is "H" during the write cycle, the outputs will remain at High-Z.

*2 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

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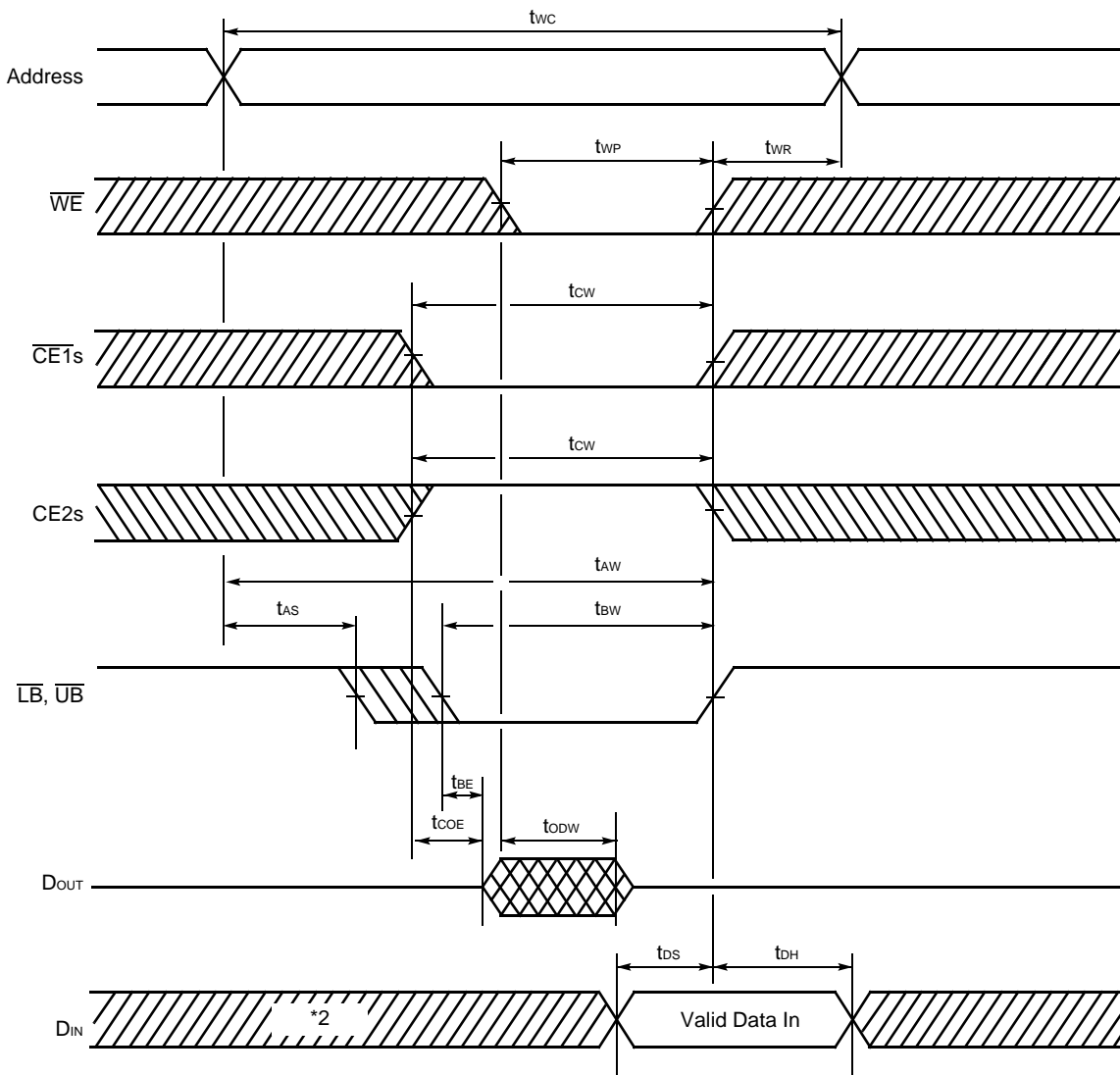
• Write Cycle *1 (CE2s Control) (SRAM)



*1 : If \overline{OE} is "H" during the write cycle, the outputs will remain at High-Z.

*2 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

• Write Cycle *1 (\overline{LB} , \overline{UB} Control) (SRAM)



*1 : If \overline{OE} is "H" during the write cycle, the outputs will remain at High-Z.

*2 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

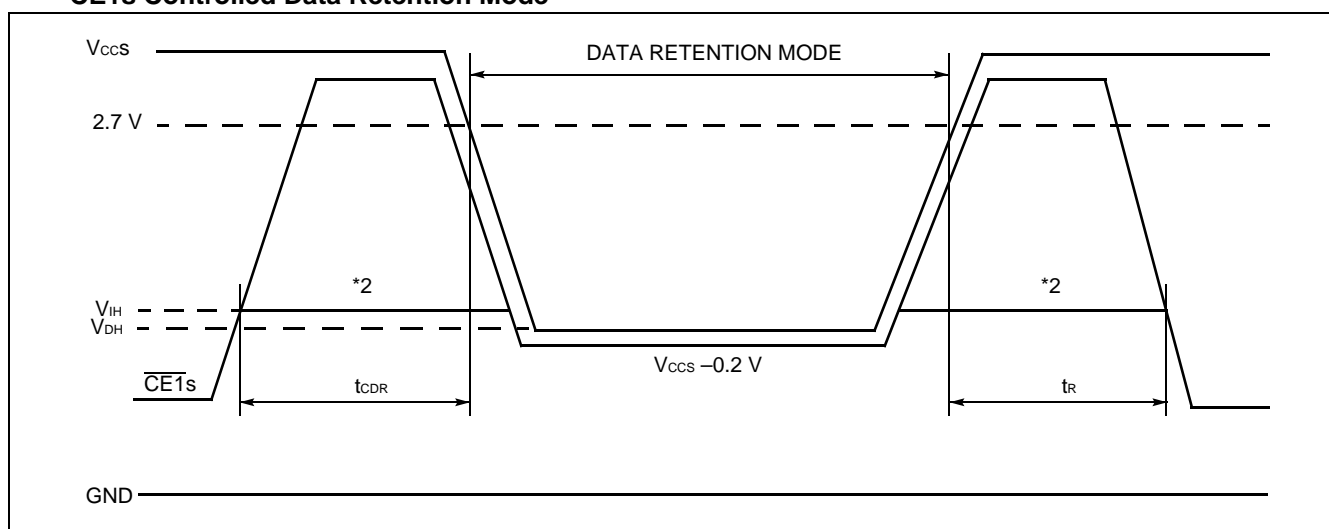
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2. Data Retention Characteristics (SRAM)

| Parameter | Symbol | Value | | | Unit |
|---|------------|----------|-----|-----|---------|
| | | Min | Typ | Max | |
| Data Retention Supply Voltage | V_{DH} | 1.5 | — | 3.3 | V |
| Standby Current | I_{DDs2} | — | 1 | 4 | μA |
| Chip Deselect to Data Retention Mode Time | t_{CDR} | 0 | — | — | ns |
| Recovery Time | t_r | t_{RC} | — | — | ns |

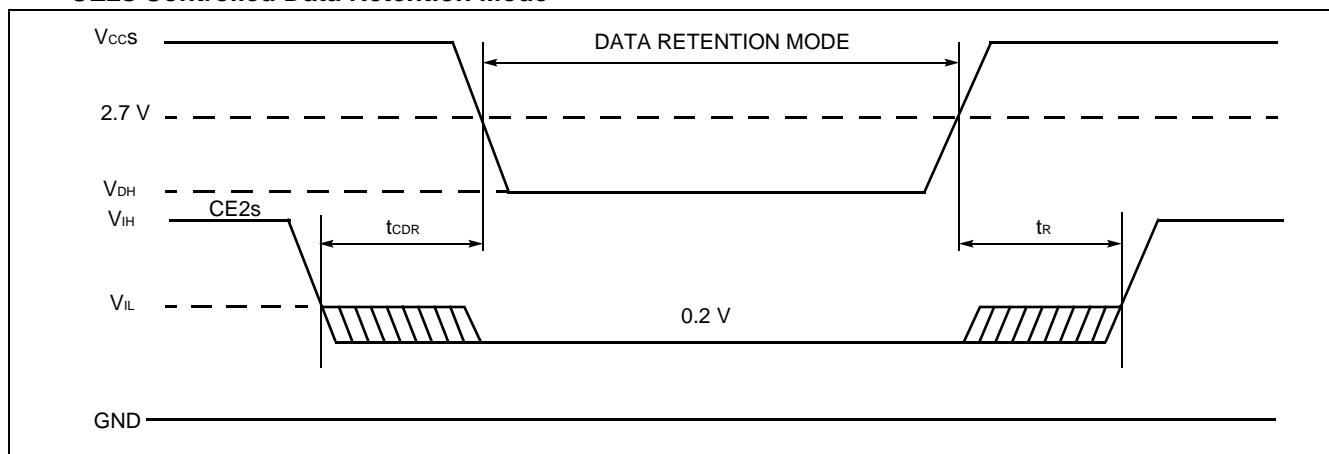
Note : t_{RC} : Read cycle time

• $\overline{CE1}$ s Controlled Data Retention Mode *1



- *1 : In $\overline{CE1}$ s controlled data retention mode, input level of $\overline{CE2}$ s should be fixed V_{ccs} to $V_{ccs}-0.2 V$ or V_{ss} to $0.2 V$ during data retention mode. Other input and input/output pins can be used between $-0.3 V$ to $V_{ccs}+0.3 V$.
- *2 : When $\overline{CE1}$ s is operating at the V_{IH} Min level (2.2 V), the standby current is given by I_{SB1s} during the transition of V_{ccs} from 3.3 V to 2.2 V.

• $\overline{CE2}$ s Controlled Data Retention Mode *



* : In $\overline{CE2}$ s controlled data retention mode, input and input/output pins can be used between $-0.3 V$ to $V_{ccs}+0.3 V$.

■ PIN CAPACITANCE

| Parameter | Symbol | Test Setup | Value | | Unit |
|-------------------------------------|-----------|---------------|-------|-----|------|
| | | | Typ | Max | |
| Input Capacitance | C_{IN} | $V_{IN} = 0$ | 11 | 14 | pF |
| Output Capacitance | C_{OUT} | $V_{OUT} = 0$ | 12 | 16 | pF |
| Control Pin Capacitance | C_{IN2} | $V_{IN} = 0$ | 14 | 16 | pF |
| \overline{WP}/ACC Pin Capacitance | C_{IN3} | $V_{IN} = 0$ | 17 | 20 | pF |

Note : Test conditions $T_A = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$

■ HANDLING OF PACKAGE

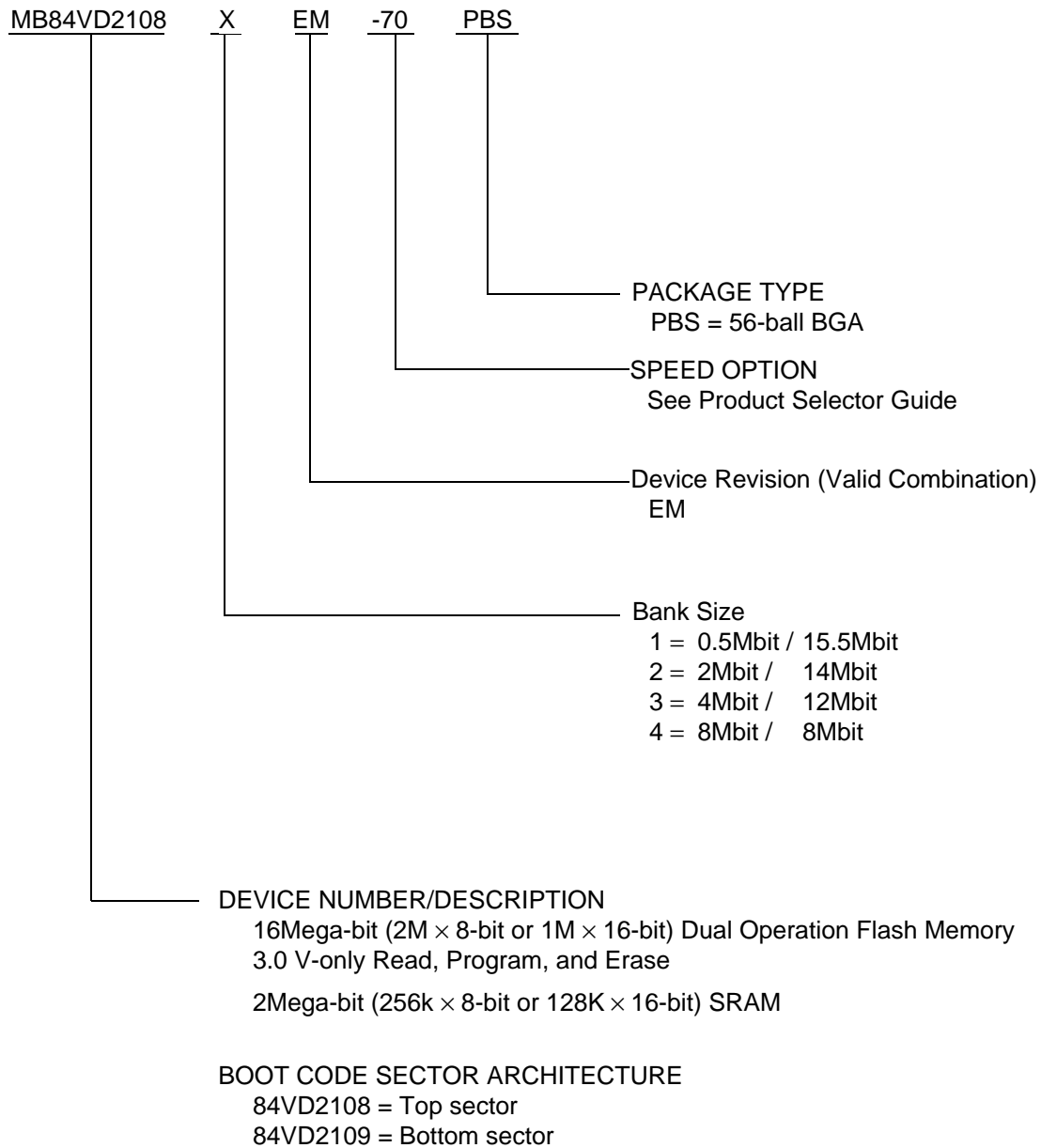
Please handle this package carefully since the sides of package create acute angles.

■ CAUTION

- The high voltage (V_{ID}) cannot apply to address pins and control pins except \overline{RESET} .
Exception is when autoselect and sector group protect function are used, then the high voltage (V_{ID}) can be applied to \overline{RESET} .
- Without the high voltage (V_{ID}), sector group protection can be achieved by using "Extended Sector Group Protection" command.

MB84VD2108XEM/2109XEM-70

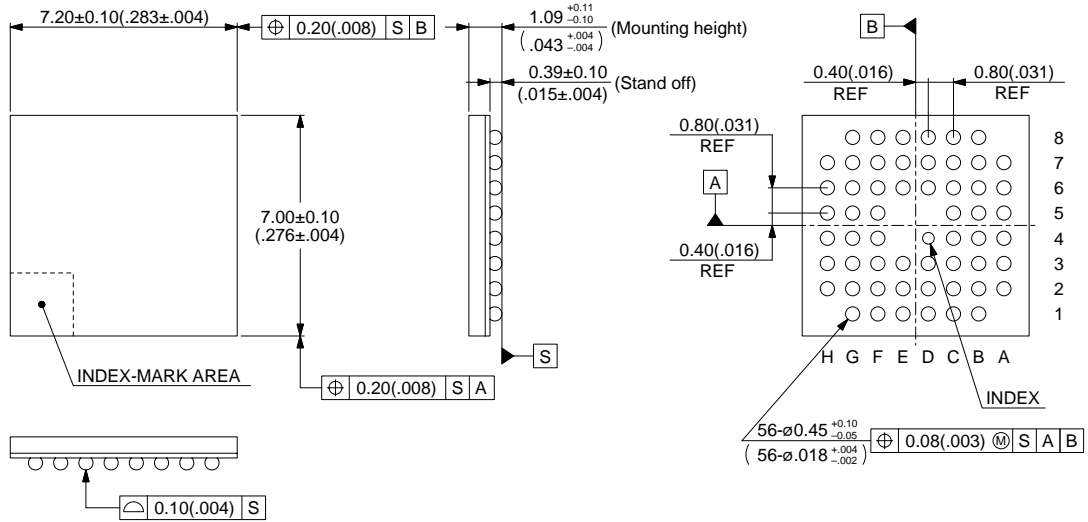
■ ORDERING INFORMATION



MB84VD2108XEM/2109XEM-70

■ PACKAGE DIMENSION

56-pin plastic FBGA
(BGA-56P-M02)



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Dimensions in mm (inches)

Note : The values in parentheses are reference values.

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