July 1997

SuperSPARC™-II MBus Modules

DATA SHEET — 75/85 MHz SuperSPARC-II + 1 MB E-Cache

DESCRIPTION

The STP5011D is the MBus module incorporating the latest SuperSPARC-II microprocessor. This module provides a CPU sub-system with the high performance superscalar SuperSPARC-II microprocessor (STP1021A) and the latest Secondary Cache controller (MXCC / STP1091). This module is designed with one megabyte (MB) of Secondary Cache and is targeted for high performance desktops, servers, and upgrades of the existing MBus based systems to higher performance levels. The SuperSPARC-II integrates a super scalar integer unit, an IEEE754 floating point unit, a SPARC Reference Memory Management Unit (MMU), and a total of 36 KBytes of instruction and data cache memory. The SuperSPARC-II is an IEEE JTAG 1149.1 compliant fully scannable design. The STP1021A uses the VBus to interface with the MXCC and the Secondary Cache memory. Along with the SuperSPARC-II CPU, the MXCC, and the synchronous SRAMs, the STP5011D module also consists of a voltage regulator module that maintains the supply voltage to the CPU and the MXCC within the required tolerance.

Features

- High performance 75, 85 MHz SuperSPARC-II CPU modules
- Implement 50 MHz MBus
- Function in all 40 MHz MBus systems
- Cache coherency support for multi-processing
- On-board voltage regulator module
- MBus compatible module design
- Fully tested CPU module
- 3.3" X 5.776" form factor
- MBus is implemented on a 100-pin Fujitsu / AMP Microstrip connector

Benefits

- Deliver 126 SPECint92, 121 SPECfp92 at 75 MHz, and 140 SPECint92, and 135 SPECfp92 at 85 MHz
- Significant performance gain over 40 MHz MBus
- Excellent performance upgrade for existing systems
- Allows a wide range of scalable systems to be built
- Eliminates an external voltage regulator
- Removes Customer's CPU module design burden
- Allows faster Time to Market
- Small Footprint
- High performance impedance controlled connector provides reliable signal integrity

TYPICAL STP5011D APPLICATIONS

The STP5011D is intended for use in a broad range of applications from uniprocessor desktop machines to large multiprocessor servers. STP5011D modules allow the existing 40 MHz and 50 MHz MBus customers an easy performance upgrade path proving the benefit of scalability of the MBus modules. A block diagram of a system with STP5011D interfacing directly with the rest of the system is shown below.

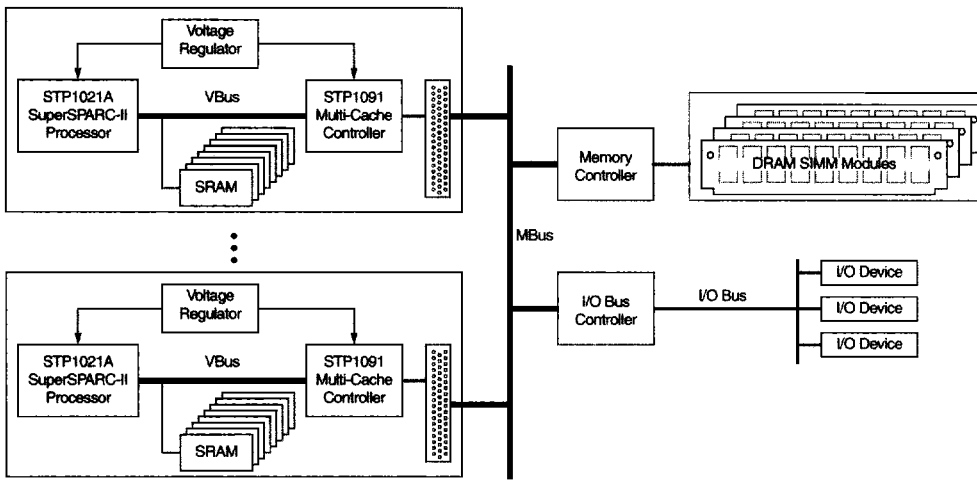


Figure 1. Typical STP5011D Uniprocessor / Multiprocessor System

MBus Description

MBus is a SPARC International standard bus designed to function as a processor-independent bus between one or more processors and memory. It is a 64-bit multiplexed high-performance bus. It is fully synchronous with all the transfers controlled by an MBus clock. It supports block transfers in sizes up to 128 bytes. All transactions on the MBus are arbitrated by an external arbiter. The arbitration algorithm is not included in the MBus definition to allow flexibility in system design. MBus is defined for uniprocessor and multiprocessor systems. The uniprocessor form of MBus is termed "Level1", and the multiprocessor version is called "Level2". STP5011D can operate in either Level1 or Level2.

Module PCB Board

The 12 layer module PCB is designed to minimize impedance mismatches between the components on the module and between the module and the rest of the system. The characteristic impedance specification is 50Ω ±10% on all the signal layers, and the signal propagation speed is 180ps/inch ±20ps/inch. The MCLK0 signal is an input to the module and the module adds a minimum offset of 2ns on the MCLK0 between the MBus connector and the MXCC. The offset is implemented by running a long serpentine trace between the connector and the MXCC. This offset is implemented for compliance with Sun Microsystem's SPARCstation 10 and SPARCstation 20 systems. The other unused MCLKs are terminmated on the module.The maximum total board thickness is 70 mil. The module has a form factor of 83.82mm (3.3") x 146.70mm (5.776").

MBus Connector

The MBus connector (AMP part number 121497-4) is a high performance impedance controlled (50Ω ±10%) connector. The connector has 100 signal pins and 20 additional pins (5 blades) for power and ground. The mating connector to be used on a system board can be ordered from AMP or Fujitsu. The MBus connector is highly reliable and can be installed easily. It has excellent electrical performance in terms of transmission line characteristics with low capacitance and inductance. The connector's 5 supply blades are divided into two separate power and three separate ground blades and each has 1 nH inductance.

Following is the MBus signal pinout of the connector.

Following is the MBus signal pin definitions for the connector. The three columns represent the three pins on the 100-pin micro-strip connector.

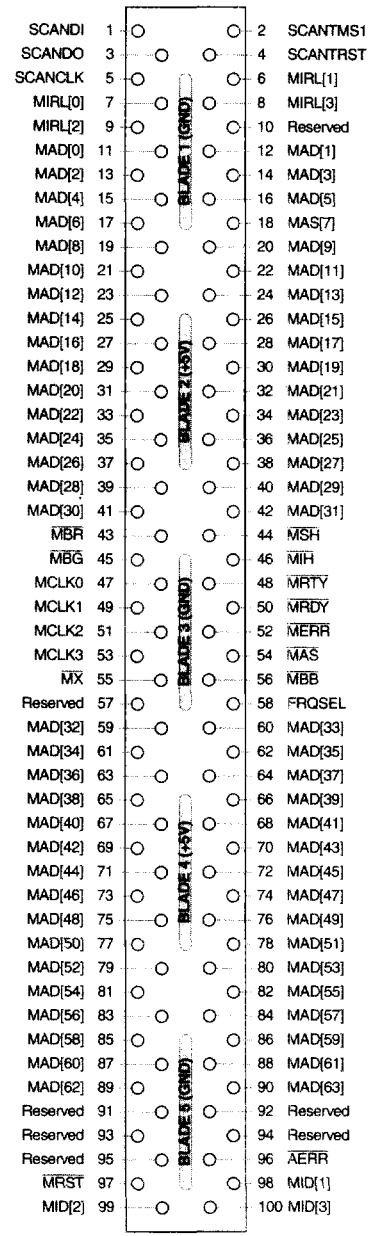


Figure 2. MBus Connector Pinout

MBus Mode Signals Description

Table 1 provides a description of all the STP5011D signals.

TABLE 1: Pin Descriptions - MBus Interface ($\overline{CCMODE}$ = H)

$\overline{AERR}$ [1]	O	In error mode, the STP5011D will perform an automatic watchdog reset. Error mode is entered when any exception is taken with traps disabled (PSR.ET=0). This signal is driven only when asserted; otherwise, it is three-stated. H = Normal operation. L = Error Mode.
FRQSEL	O	This signal, along with a jumper setting on the motherboard, is used by the SS20 system to determine the MBus speed. This signal is pulled low on the module. This allows the module to run at 50 MHz when the jumper on the mother board is set to 40/50 mode. In SS10s this module will run at 40 MHz.
$\overline{MX}$	I	Selects between MBus or XBus. H = X Bus is selected. L = MBus is selected.
MCLK[3:0]	I	MBus clock generated on the on the motherboard; only MCLK0 is used.
MAD[63:0]	I/O	Multiplexed Command/Data.
$\overline{MAS}$	I/O	MBus address strobe. Asserted by the bus master when an MBus command word (containing address and control information) is on MAD[63:0]. H = No command word. L = MBus command word on MAD[63:0].
$\overline{MBB}$	I/O	MBus busy. Asserted when there is any active transaction on MBus. H = MBus free. L = MBus busy.
$\overline{MBG}$	I	MBus grant. This is a dedicated (not bussed) signal from the MBus arbiter to this bus master. H = Not granted. The STP5011D may not initiate an MBus transaction. L = Granted. The STP5011D may initiate an MBus transaction as soon as MBus is free.
$\overline{MBR}$	O	MBus request. This is a dedicated (not bussed) signal from the STP5011D to the MBus arbiter. H = No request. L = Requesting to initiate a transaction on MBus.
$\overline{MERR}$	I	MBus error. Encoded along with $\overline{MRDY}$ and $\overline{MRTY}$ to indicate acknowledge type (the type of error response).

$\overline{MERR}$	$\overline{MRDY}$	$\overline{MRTY}$	Description
H	H	H	Idle Cycle
H	H	L	Relinquish and Retry
H	L	H	Valid Data Transfer
H	L	L	Reserved
L	H	H	Bus Error (ERROR1)
L	H	L	Timeout Error (ERROR2)
L	L	H	Uncorrectable Error (ERROR3)
L	L	L	Retry

TABLE 1: Pin Descriptions - MBus Interface ($\overline{\text{CCMODE}}$ = H) (Continued)

MID[3:1]	I	MBus Module ID. The identifier of this MBus device. Usually hardwired by the system. MID3 is the Most Significant Bit (MSB). MID[0] is connected to Ground on the module.
$\overline{\text{MIH}}$	I/O	Memory inhibit. Asserted by a snooping cache when it notices a coherent read of cache block it owns. Memory responds to this signal by ignoring the request. H = No memory inhibit. L = Inhibit memory. The snooping cache which asserted $\overline{\text{MIH}}$ will respond with the data in place of memory.
MIRL[3:0]	I	Interrupt request level. This field specifies the level of the highest priority interrupt request that is currently pending. If MIRL3-MIRL0 = 0000, no interrupts are pending. Level 15 (MIRL3-MIRL0 = 1111) is a NMI (disable all traps) Level 14 Highest maskable interrupt Level 1 Lowest maskable interrupt Level 0 No interrupts are pending
$\overline{\text{MRDY}}$	I/O	MBus ready. Encoded along with $\overline{\text{MERR}}$ and $\overline{\text{MRTY}}$ to indicate acknowledgment type (the type of error response). See table in $\overline{\text{MERR}}$ description.
$\overline{\text{MRTY}}$	I	MBus retry. Encoded along with $\overline{\text{MERR}}$ and $\overline{\text{MRDY}}$ to indicate acknowledgment type (the type of error response). See table in $\overline{\text{MERR}}$ description.
$\overline{\text{MSH}}$ [1]	I/O	Memory shared. Asserted by a snooping cache when it notices a coherent read of a cache block it is caching. Both caches will mark the data as shared. H = No sharing. L = Shared data.
$\overline{\text{MRST}}$	I	Reset In. This causes an external reset for the STP5011D. At power-on, $\overline{\text{RSTIN}}$ must be held low for at least 100 ms to all allow the PLL to stabilize. If the PLL is known to be stable, $\overline{\text{RSTIN}}$ may be asserted for as short as 8 cycles. Any time Vcc is not within specification both SCANTMS2 (pin 4) and $\overline{\text{MRST}}$ (pin 97) must be asserted to avoid internal and external driver fights. Both internal and external driver fights might damage the chips. H = Normal operation. L = The STP5011D is externally reset.
Reserved	N/A	These pins are not used by the module. The module does not drive these pins and does not expect them to be driven. Leave these pins floating.
SCANCLK	I	JTAG test clock input.
SCANDI	I	JTAG test data input.
SCANDO	O	JTAG test data output.
SCANTMS1	I	JTAG test mode select input.
$\overline{\text{SCANTRST}}$	I	JTAG test reset input.

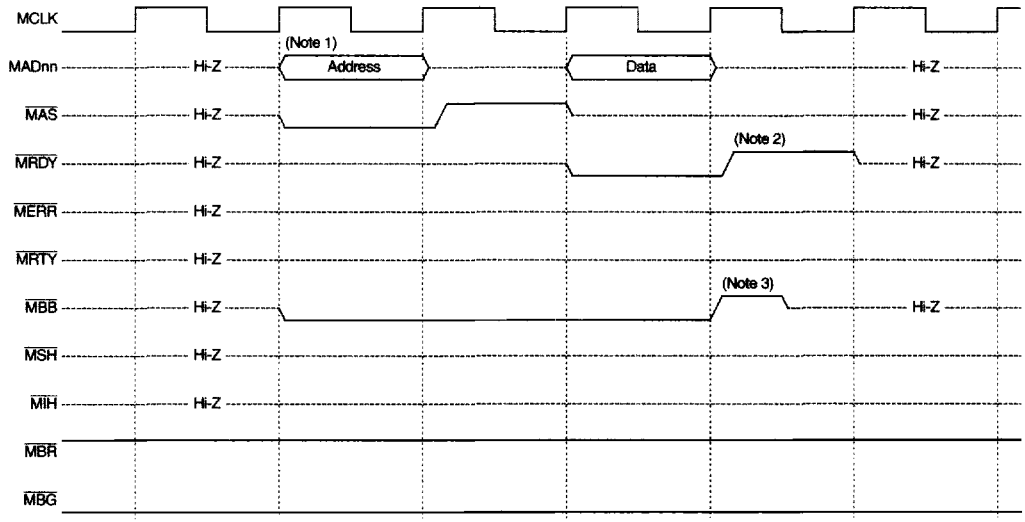
1. These pins have an open drain.

MBus Timing

The MBus read, write and invalidate operations are explained in the following section.

MBus Single Read

The single read cycle transfers a byte, half-word, word, or a double-word. Big-endian word ordering is used (the least significant bytes in a word appear on the high bits of the bus according to SPARC standard). *Figure 3* shows an MBus single read operation.

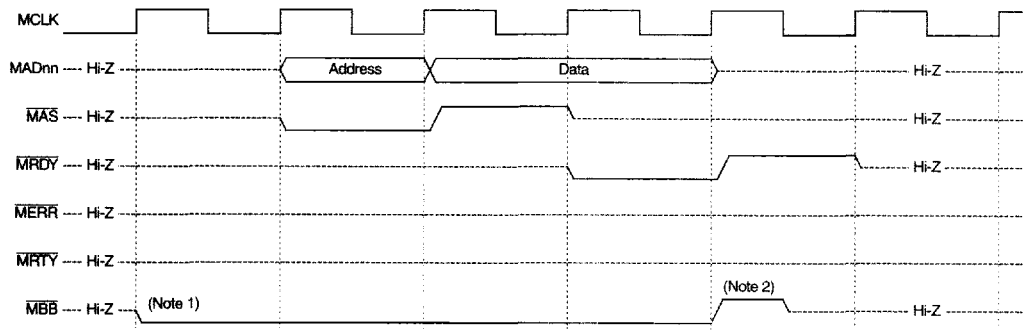


Notes: 1. MADnn lines are held to their previously driven state by system bus holders.
2. Control lines (MAS, MRDY, MERR, MRTY) are driven inactive for one clock before being released.
3. MBB is driven high for half clock cycle before being released.

Figure 3. MBus Single Read

MBus Single Write

Single write operations are queued in the store buffer. As soon as the module receives a bus grant, the transactions will be issued on the bus. The processor will not wait during this time, unless the buffer fills. Bytes, half-words, words, and double words may all be stored, with big-endian ordering. Any errors are reported as deferred data store errors. *Figure 4* shows an MBus single write operation.



Notes: 1. MBB is driven active one cycle before MAS during write and CI cycles.
2. MBB is driven inactive for half clock cycle before being released.

Figure 4. MBus Single Write

MBus Burst Read

Figure 5 shows a 32-byte burst read operation. A read operation can be performed on any size of data transfer that is specified by the SIZE bits. Read transactions support wrapping (critical-word- first ordering). Transactions involving fewer than eight bytes will have undefined data on the unused bytes.

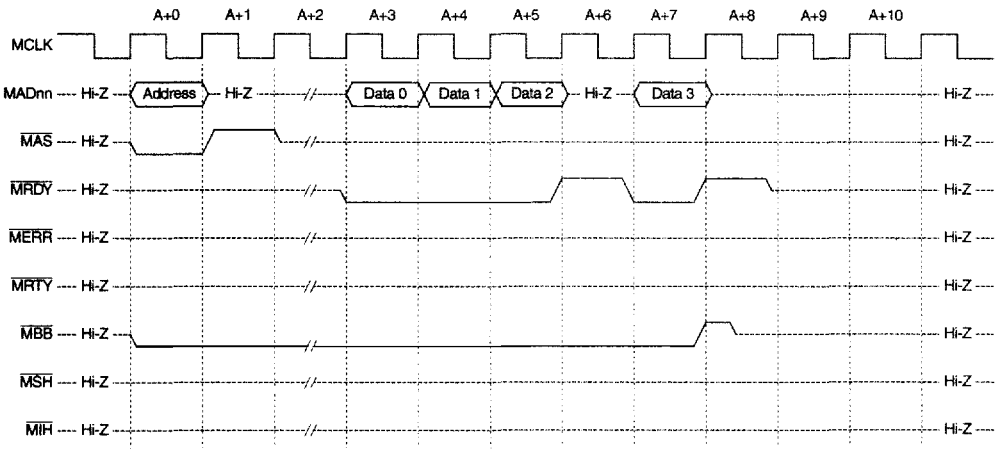
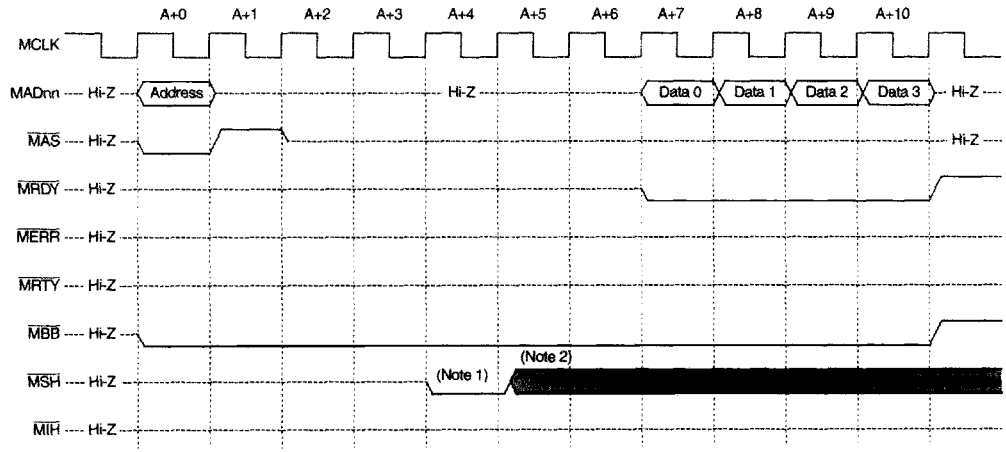


Figure 5. MBus Burst Read

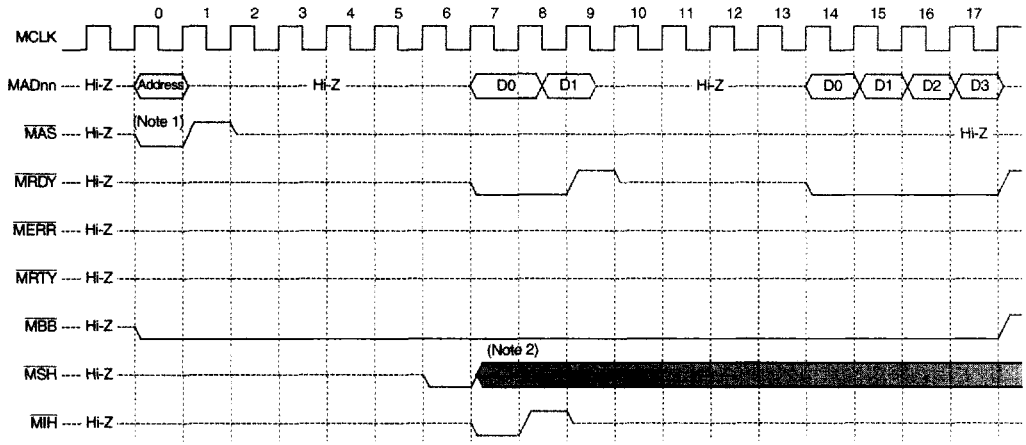
MBus Coherent Read

Coherent Read (CR) transactions are used to read data from the current owner. The owner may be memory or another cache. CR will be used for all on-board data cache load misses and all on-board instruction cache misses. If another cache owns the data, it will respond by asserting the $\overline{MIH}$ signal and providing the data. All CR transactions use critical-word-first ordering. The double-word that is needed first will be the starting address of the transaction. Double-words from memory must be returned in modulo 32-byte address order. Once the needed data arrives, the processor will use it immediately. *Figure 6* shows an MBus coherent read of shared data. Any processor that has a valid cached copy of data referenced by CR transactions must assert the $\overline{MSH}$ signal to indicate that the information is shared. The module can accept the assertion of $\overline{MSH}$ at any time until receipt of the first data word. If the data is owned by another cache, the module will ignore any data ready responses until four cycles beyond the assertion of $\overline{MIH}$. This allows memory controllers to begin transmitting data sooner. Memory controllers must not respond with data until a time equal to the maximum $\overline{MIH}$ assertion delay for any cache in the system. *Figure 7* shows an MBus coherent read of owned data.



Notes: 1. $\overline{MSH}$ may occur from A+2 to A+7.
2. $\overline{MSH}$ is an open drain signal. It is not driven inactive. The system pull-up resistor returns it to an inactive level.

Figure 6. MBUS Coherent Read of Shared Data



Notes: 1. Device is not the Master.
2. MSH is an open drain signal. It is not driven inactive. The system pull-up resistor returns it to an inactive level.

Figure 7. MBUS Coherent Read of Owned Data

MBus Coherent Invalidate

A Coherent Invalidate (CI) operation can only be performed on a block (32 bytes). All CI operations will be snooped by all snooping caches. If a Coherent Invalidate operation hits in a cache, that copy will be invalidated immediately, regardless of its state. Memory is responsible for the acknowledgment of the CI transaction. *Figure 8* shows a CI operation.

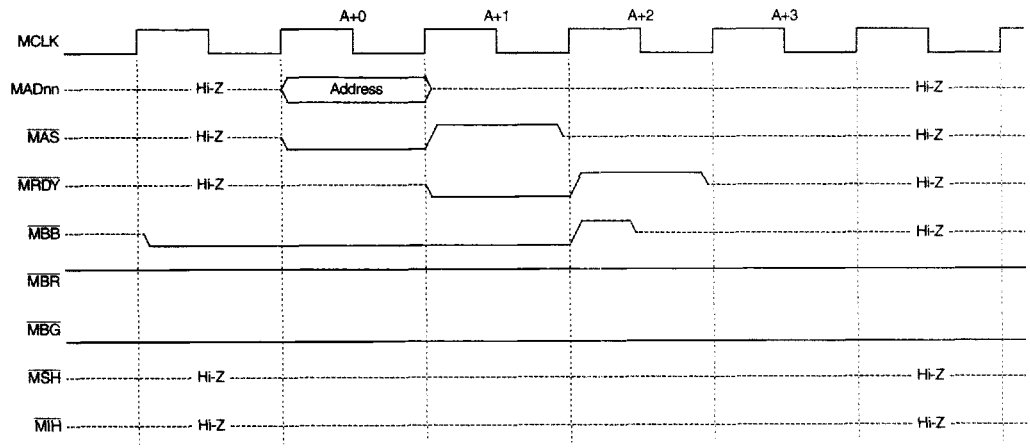


Figure 8. MBus Coherent Invalidate

Coherent Read and Invalidate

Since the MBus supports a write-invalidate type of cache-consistency protocol, a special Coherent Read and Invalidate (CRI) transaction that combines a CR transaction with the CI transaction was included to reduce the number of MBus Coherent transactions. Caches that are performing CR transactions with the knowledge that they intend to immediately modify the data can issue this transaction. Each CRI transaction will be snooped by all system caches. If the address hits and the cache does not own the block, that cache immediately invalidate its copy of this block, no matter what state the data was in. If the address hits and the cache owns the block, the block will assert $\overline{\text{MIH}}$ and supply the data. When the data has been successfully supplied, the cache will then invalidate its copy of this block. $\overline{\text{MSH}}$ is not driven during the CRI transaction.

Coherent Write and Invalidate

A Coherent Write and Invalidate transaction combines a block write transaction with a CI transaction. Each Coherent Write and Invalidate transaction will be snooped by all system caches. If the address hits, caches will invalidate their copies of this block, no matter what state the data was in. Neither $\overline{\text{MIH}}$ nor $\overline{\text{MSH}}$ is asserted for Coherent Write and Invalidate transactions. *Figure 9* shows a Coherent Write and Invalidate operation.

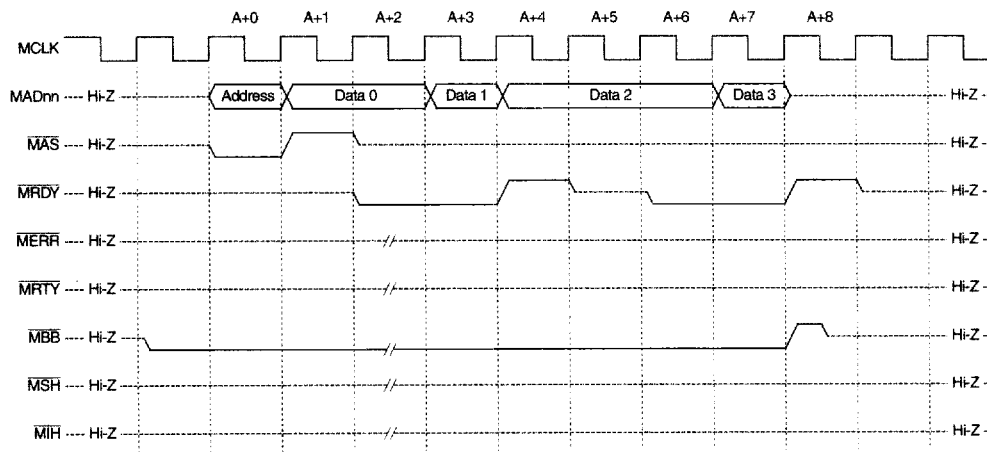


Figure 9. MBus Coherent Write and Invalidate

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

V_{CC}	Supply voltage range	0 to 6	V
V_I	Input voltage range	-0.5 to V_{CC} + 0.5	V
V_O	Output voltage range	-0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature	-65 to 150	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute -maximum-rated conditions may affect device reliability.

Recommended Operating Conditions

V_{CC}	Supply voltage		4.75	5.0	5.25	V
V_{SS}	Ground		–	0	–	V
V_{IH}	Input high voltage		2.2	–	V_{CC} + 0.3	V
V_{IL}	Input low voltage		-0.3	–	0.8	V
I_{OH}	Output high current		–	–	-2.0	mA
I_{OL}	Output low current	All outputs except $\overline{MSH}$	–	–	2.2	mA
		$\overline{MSH}$	–	–	8.0	mA
T_A	Operating ambient temperature		0	–	40 [1]	°C

1. Maximum ambient temperature indicates that the maximum case temperature (T_C) of 85 °C is not exceeded on STP1021A at 10,000 feet altitude.

Power Consumption

The SuperSPARC-II module has a programmable output dc-dc voltage regulator on-board, and it can operate with a 5.0V ± 5% external power supply. The output of the regulator is programmed to be 5.0V ± 50 mV. The average power consumption of the 85 MHz module with the SuperSPARC-II and MXCC operating at 5.05 V, and the SRAMs and other components including the regulator operating at 5.25 V is 35.4 Watts. The I_{CC} given in the DC Characteristics is the current at the input to the module.

DC Characteristics

V_{OH}	Output high voltage [1]	I_{OH} = Max, V_{CC} = Min	2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = Max, V_{CC} = Max	–	–	0.4	V
I_{CC}	Supply current	V_{CC} = 5.25, VBUS = 85 MHz, MBus = 50 MHz $t_{W(VCLK)}$ or $t_{W(MCLK)}$ = Min	–	6.75	[2]	A
		V_{CC} = 5.25, VBUS = 75 MHz, MBus = 50 MHz $t_{W(VCLK)}$ or $t_{W(MCLK)}$ = Min		6.25	[3]	A
I_{CCQ}	Quiescent power supply current	V_{CC} = Max, V_I = V_{SS} or V_{CC}	–	–	425	mA
I_{OZ}	High-impedance output current	V_{CC} = Max, V_O = 2.4V	–	–	20	µA
		V_{CC} = Max, V_O = 0.4V	–	–	-20	µA
C_I	Input capacitance [4]		–	–	10	pF
C_O	Output capacitance [4]		–	–	15	pF

1. Open drain pins $\overline{AERR}$ and $\overline{MSH}$ are not driven high.
2. A 100ms peak I_{CC} is 20% more than the average.
3. A 100ms peak I_{CC} is 20% more than the average.
4. This specification is provided as an aid to board design. This specification is not assured during manufacturing testing.

Timing Specifications

This section provides the timing specifications of the module. All Mbus signals are TTL level signals. The signals should be measured at Low = 0.8 V, and High = 2.0 V. The threshold for clock is 1.5 V for the purposes of making timing measurements and calculations. For timing purpose the Mbus signal are grouped into Address/Data signals, Bussed signals, and Point-to-Point signals.

- Address/Data lines are: MAD[63:0].
- Bussed control signals are: $\overline{MBB}$, $\overline{MAS}$, $\overline{MERR}$, $\overline{MRTY}$, $\overline{MRDY}$, $\overline{MIH}$, $\overline{MSH}$.
- Point-to-Point control signals are: $\overline{MBR}$, $\overline{MBG}$. These Point-to-Point signals are unique to a module.
- $\overline{MX}$, and MID[3:1] are static signals and have no specified timing. MID[0] is connected to Ground on the module. MIRL[3:0] are asynchronous signals.

AC Characteristics: Module Timing - Setup and Hold

t_{SU}(MAD)	MBus MAD lines setup to MCLK	MAD[63:0]	3.8	–	ns
t_{SU}(MC)	MBus bused setup to MCLK	$\overline{MAS}$, $\overline{MERR}$, $\overline{MRTY}$, $\overline{MRDY}$, $\overline{MBB}$, $\overline{MSH}$, $\overline{MIH}$	4.0	–	ns
t_{SU}(MIRL)	MBus IRL[3:0] setup to MCLK	MIRL[3:0]	5.0	–	ns
t_{SU}(MBG)	MBus point-to-point setup to MCLK	$\overline{MBG}$	4.8	–	ns
t_H(MAD)	MBus MAD lines hold from MCLK	MAD[63:0]	3.5	–	ns
t_H(MC)	MBus bused hold from MCLK	$\overline{MAS}$, $\overline{MRDY}$, $\overline{MBB}$, $\overline{MERR}$, $\overline{MRTY}$, $\overline{MSH}$, $\overline{MIH}$	3.5	–	ns
t_H(MIRL)	MBus point-to-point hold from MCLK	MIRL[3:0]	3.5	–	ns
t_H(MBG)	MBus Point-to-point hold from MCLK	$\overline{MBG}$	3.5	–	ns

AC Characteristics: Module Timing - Switching Characteristics [1] [2]

t_P(MAD)	Propagation delay, MCLK to MBus MAD[63:0]	–	15.2	ns
t_P(MC)	Propagation delay, MCLK to MBus control $\overline{MAS}$, $\overline{MRDY}$, $\overline{MBB}$, $\overline{MIH}$, $\overline{MSH}$	–	14.2	ns
t_P(MBR)	Propagation delay, MCLK to MBus point-to-point $\overline{MBR}$	–	15.9	ns
t_{OH}(MAD)	Output hold time, MCLK to MBus MAD[63:0]	3.5 [3]	–	ns
t_{OH}(MC)	Output hold time, MCLK to MBus control $\overline{MAS}$, $\overline{MRDY}$, $\overline{MBB}$, $\overline{MIH}$, $\overline{MSH}$	4.5	–	ns
t_{OH}(MBR)	Output hold time, MCLK to MBus point-to-point $\overline{MBR}$	4.6	–	ns

1. The above specification is for a lumped capacitive load of 50pF.
2. The timing specification is based on Spice simulations.
3. MAD[63:0] output hold time is shorter compared to other signals.

Clock Timing [1]

t_w(MBUS CLK)	MBUS CLK pulse duration (50 MHz)	20	–	–	ns
	MBUS CLK duty cycle	25	50	75	%
t_w (SCAN CLK)	SCAN CLK pulse duration (10 MHz)	100	–	–	ns
	SCAN CLK duty cycle	–	50	–	%

1. This is for the PLL enabled. If the PLL is disabled, the part supports a fully static design. The timing parameters are not assured, since this is not tested.

JTAG and Miscellaneous Timing - Setup and Hold

t_{su}(SCAN TRST)	Setup to VCLK	$\overline{\text{SCANTRST}}$ (synchronous) [1]	20	–	ns
t_{su}(SCAN DI)	JTAG setup to SCAN CLK	SCANDI	20	–	ns
t_{su}(SCANTMS)	JTAG setup to SCAN CLK	SCANTMS	20	–	ns
t_h(SCAN TRST)	Hold from VCLK	$\overline{\text{SCANTRST}}$ (synchronous) [1]	20	–	ns
t_h(SCAN DI)	JTAG hold from SCAN CLK	SCANDI	20	–	ns
t_h(SCANTMS)	JTAG hold from SCAN CLK	SCANTMS	20	–	ns

1. SCANRESET can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

JTAG and Miscellaneous Timing - Switching Characteristics

t_p(SCANDO)	SCAN CLK (falling edge) to SCANDO	2.5	20	ns

MECHANICAL SPECIFICATIONS

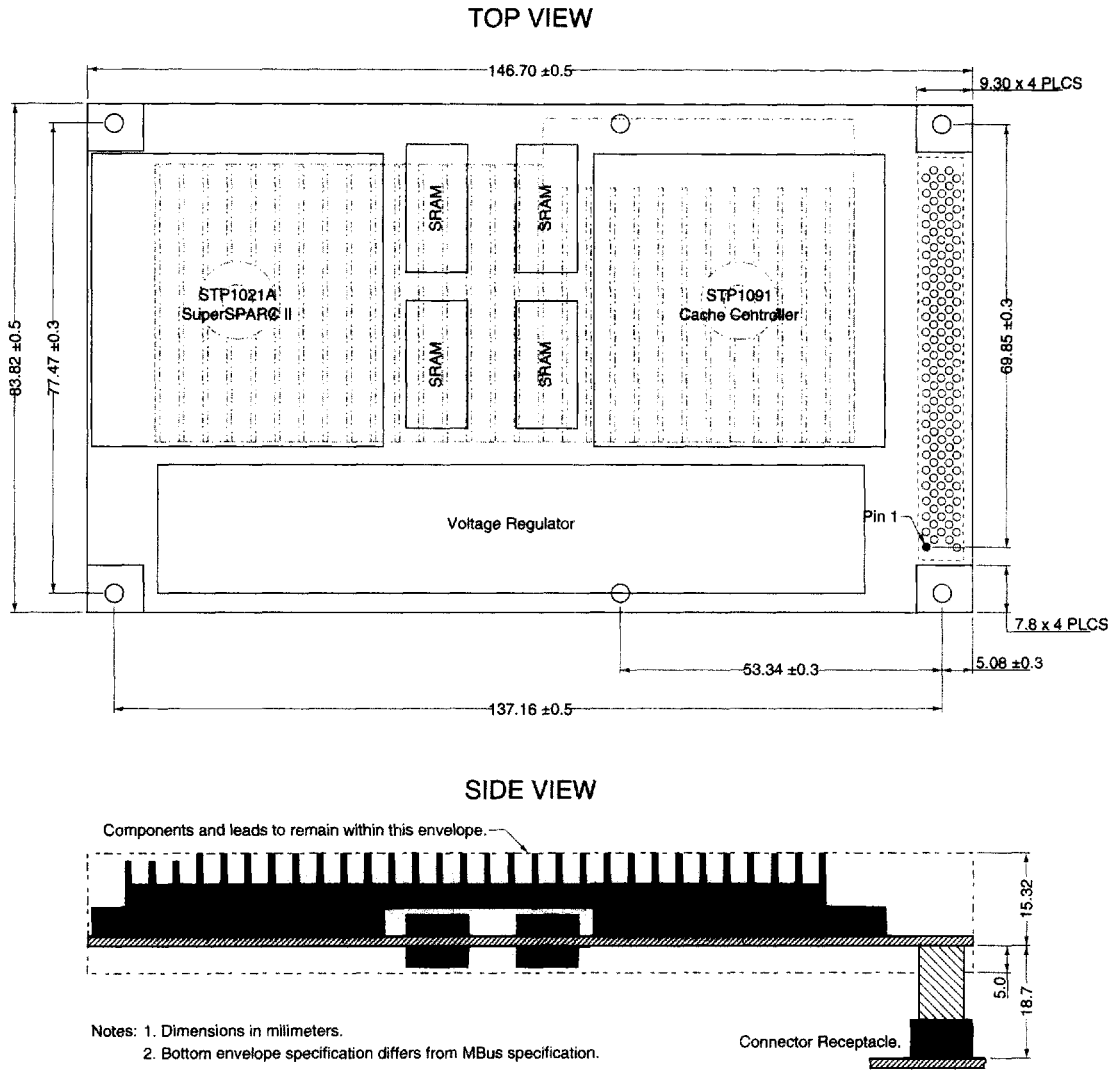
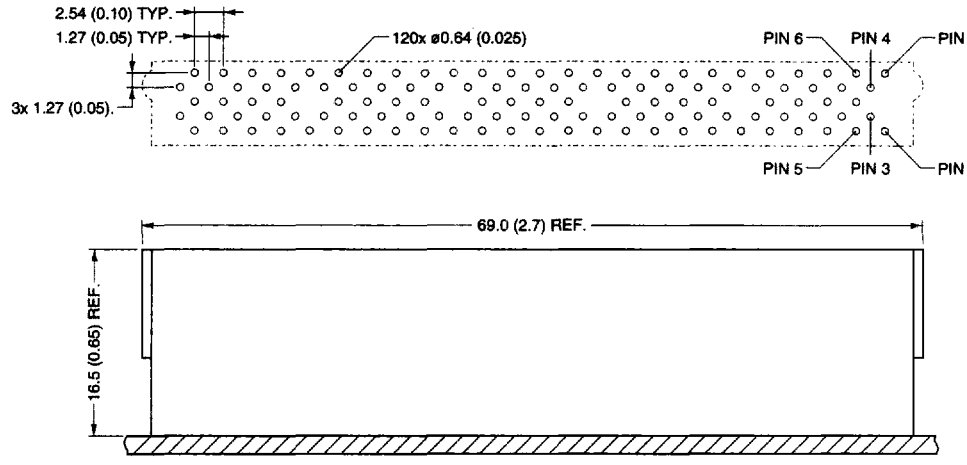


Figure 10. CPU Module Dimensions



Notes: 1. Dimension in Inches. Dimensions in parenthesis in mm.
2. Connector part number: AMP 121354-4 or Fujitsu MCN-264P100-G/C.
3. For complete connector specifications, contact the manufacturer.

Figure 11. MBUS Connector Dimensions

ENVIRONMENTAL, SHOCK AND VIBRATION SPECIFICATION

Operating Humidity	5% to 95% RH
Nonoperating Humidity	95% RH
Operating Altitude	63kPa, 10 C to 40 C
Nonoperating Altitude	17.3kPa, 0 C
Operating Shock	6 G, 11 msec, half-sine, 10 impacts/face
Nonoperating Shock	35 G, 11 msec, half-sine, 3 impacts/face
Operating Vibration	0.3 G peak, 2 sweeps of 5 to 500 to 5 Hz
Nonoperating Vibration	1.2 G peak, 2 sweeps of 5 to 500 to 5 Hz

The following additional test are performed during Engineering Qualification.

Operating Temp. Soak Test	-5 C to 75 C, 20 C/min., 8 hrs. at each extreme.
Nonoperating Temp. Soak Test	-40 C to 125 C, 20 C/min., 8 hrs at each extreme.
Operating Temp. Cycle Test	Twenty cycles of 0 to 60 °C, 20 °C / min., with ten minutes of dwell at 0 °C and 60 °C respectively.
Non-operating Temp. Cycle Test	Twenty cycles of -40 to 90 °C, 20m°C/min, with ten minutes of dwell at -40 °C and 90 °C respectively.
Non Operating Tri-Axial Random Vibration 20 to 2 kHz bandwidth	- 25 GRMS measured at center of test board for 10 minutes at 40, 25 and 85 °C
Operating Tri-axial Random Vibration 20 to 2 kHz bandwidth	- 25 GRMS measured at center of test board for 10 minutes at 0, 25 and 60 °C
Power Cycling tests	Apply voltage for 5 seconds on and 5 seconds off during twenty cycles of 0 to 60 °C, 20 °C/min., with five minutes of dwell at 0, 25 and 60 °C respectively.
Solder Reliability Tests	Non powered temperature cycling of 0 to 100 °C, 20 °C per minute change rate, 10 minute dwells at 0 °C and 100 °C, for 1000 cycles.

Note: The temperature and vibration, values and methodologies are derived from a combination of industrial component manufacture tests, Mil-Std 883 tests, IEC Tests, and from tests performed in Sun's Stress Lab.

THERMAL SPECIFICATIONS

The maximum junction temperature specification for the STP1021A is 100 °C, which is equivqlent to the maxiumum case temperature (TC) of 85 °C for STP 1021A. TC can be obtained from the following relationship:

$$T_C = T_A + P_D + \theta_{CA}$$

where:

T_A is the ambient air temperature.

P_D is the power dissipation.

θ_{CA} is the case-to air temperature for the CPU with straight fin-type heat sink. The values for the θ_{CA} are listed in the following table, "Thermal Resistance":

Thermal Resistance

θ_{CA} (°C/W)	4.8	3.5	2.8	2.3	2.0

ORDERING INFORMATION

STP5011DMBUS-75	75 MHz & 85 MHz	SuperSPARC-II module running at 75 MHz and 85 MHz

Document Part Number: STP5011D