NEC

MOS INTEGRATED CIRCUIT
μPD4616112

16M-BIT CMOS MOBILE SPECIFIED RAM
1M-WORD BY 16-BIT

Description

The μPD4616112 is a high speed, low power, 16,777,216 bits (1,048,576 words by 16 bits) CMOS mobile specified RAM featuring low power static RAM compatible function and pin configuration.

The μPD4616112 is fabricated with advanced CMOS technology using one-transistor memory cell.

The μPD4616112 is packed in 48-pin TAPE FBGA.

Features

- 1,048,576 words by 16 bits organization
- Fast access time: 80, 90 ns (MAX.)
- Byte data control: /LB (I/O0 - I/O7), /UB (I/O8 - I/O15)
- Low voltage operation: V_{CC} = 2.6 to 3.0 V
- Operating ambient temperature: T_A = –20 to +70 °C
- Output Enable input for easy application
- Chip Enable input: /CS pin
- Standby Mode input: MODE pin
- Standby Mode1: Normal standby (Memory cell data hold valid)
- Standby Mode2: Memory cell data hold invalid

Product name	Access time ns (MAX.)	Operating supply Voltage	Operating ambient temperature °C	Supply current	
				At operating mA (MAX.)	At standby μA (MAX.)
μPD4616112-BCxx	80, 90	2.6 to 3.0	–20 to +70	35	100 / 10

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The mark <R> shows major revised points.

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The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

Ordering Information

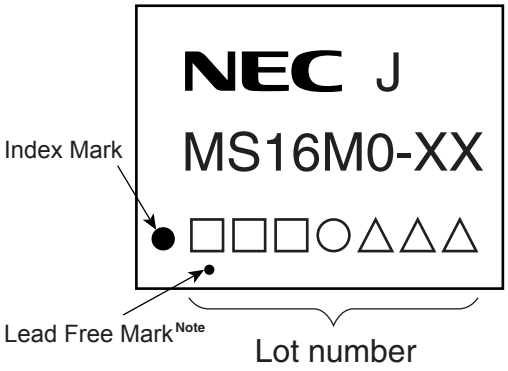
	Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark
	μPD4616112F9-BC80-BC2	48-pin TAPE FBGA (8 x 6)	80	2.6 to 3.0	–20 to +70	BC version
	μPD4616112F9-BC90-BC2		90			
<R>	μPD4616112F9-BC80-BC2-A		80			
<R>	μPD4616112F9-BC90-BC2-A		90			

<R> **Remark** Products with -A at the end of the part number are lead-free products.

Marking Image

Part number	Marking (XX)
μPD4616112F9-BC80-BC2	B1
μPD4616112F9-BC90-BC2	B2
<R> μPD4616112F9-BC80-BC2-A	B1
<R> μPD4616112F9-BC90-BC2-A	B2

<R>



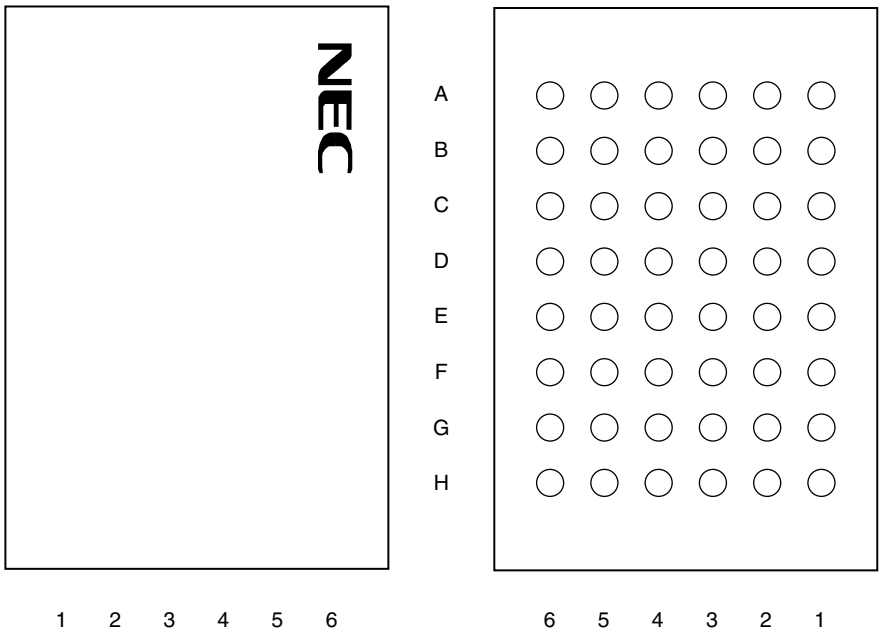
Note The lead free mark is shown in the case of lead-free products.

Pin Configuration

/xxx indicates active low signal.

48-pin TAPE FBGA (8 x 6)

Top View **Bottom View**



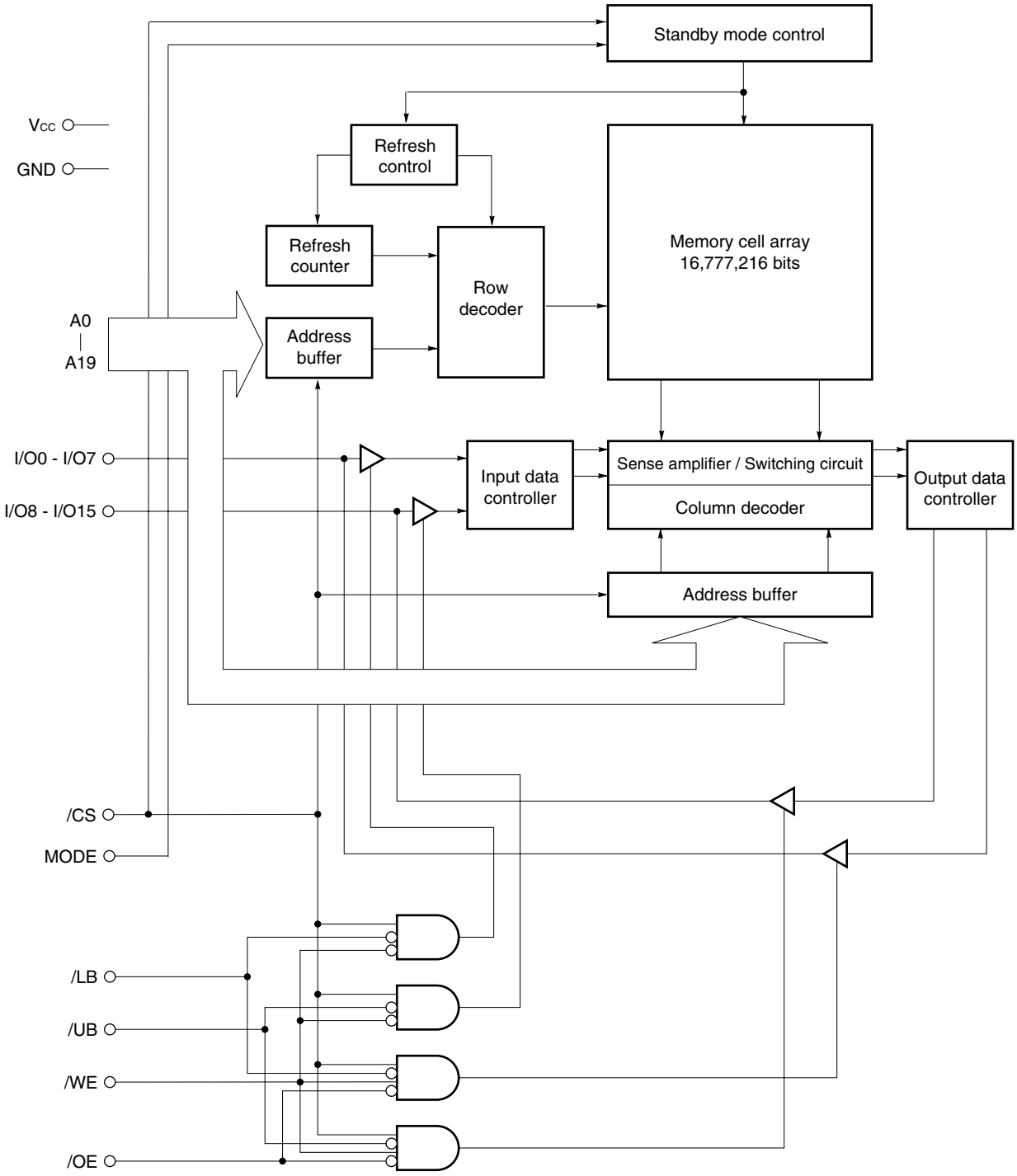
	1	2	3	4	5	6
A	/LB	/OE	A0	A1	A2	MODE
B	I/O8	/UB	A3	A4	/CS	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	GND	I/O11	A17	A7	I/O3	V_{CC}
E	V_{CC}	I/O12	GND	A16	I/O4	GND
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	A19	A12	A13	/WE	I/O7
H	A18	A8	A9	A10	A11	GND

	6	5	4	3	2	1
A	MODE	A2	A1	A0	/OE	/LB
B	I/O0	/CS	A4	A3	/UB	I/O8
C	I/O2	I/O1	A6	A5	I/O10	I/O9
D	V_{CC}	I/O3	A7	A17	I/O11	GND
E	GND	I/O4	A16	GND	I/O12	V_{CC}
F	I/O6	I/O5	A15	A14	I/O13	I/O14
G	I/O7	/WE	A13	A12	A19	I/O15
H	GND	A11	A10	A9	A8	A18

A0 - A19 : Address inputs
I/O0 - I/O15 : Data inputs / outputs
/CS : Chip Select
MODE : Standby mode
/WE : Write enable
/OE : Output enable
/LB, /UB : Byte data select
V_{CC} : Power supply
GND : Ground

Remark Refer to **Package Drawing** for the index mark.

Block Diagram



Truth Table

/CS	MODE	/OE	/WE	/LB	/UB	Mode	I/O		Supply current
							I/O0 - I/O7	I/O8 - I/O15	
H	H	×	×	×	×	Not selected (Standby Mode 1)	High impedance	High impedance	I_{SB1}
H	L	×	×	×	×	Not selected (Standby Mode 2)	High impedance	High impedance	I_{SB2}
L	H	H	H	×	×	Output disable	High impedance	High impedance	I_{CCA}
		L	H	L	L	Word read	D_{OUT}	D_{OUT}	
				L	H	Lower byte read	D_{OUT}	High impedance	
				H	L	Upper byte read	High impedance	D_{OUT}	
				H	H	Output disable	High impedance	High impedance	
		×	L	L	L	Word write	D_{IN}	D_{IN}	
				L	H	Lower byte write	D_{IN}	High impedance	
				H	L	Upper byte write	High impedance	D_{IN}	
				H	H	Write abort	High impedance	High impedance	

Caution MODE pin must be fixed to High except Standby Mode 2.

Remark ×: V_{IH} or V_{IL}

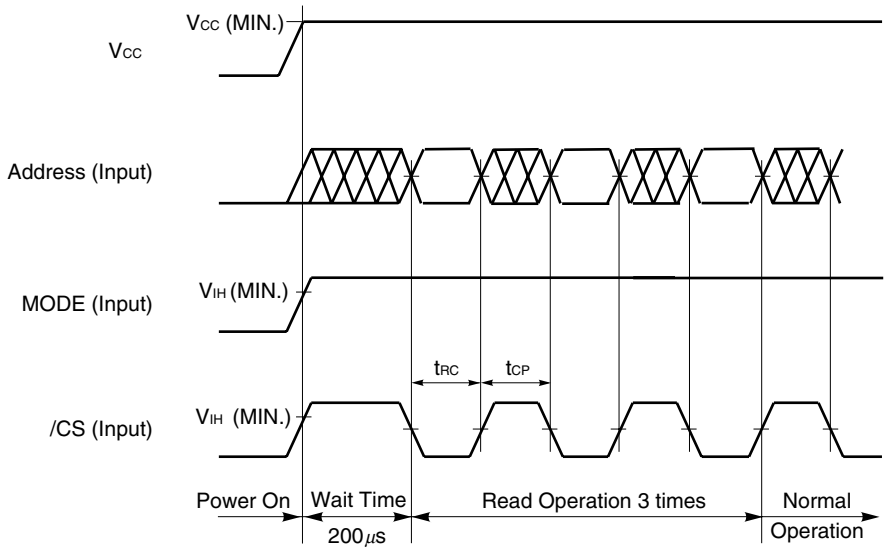
Initialization

The μPD4616112 is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, before turning on the power, a 200 μs or longer wait time must precede any signal toggling.

(2) After the wait time, read operation must be performed at least 3 times. After that, it can be normal operation.

Initialization Timing Chart



Cautions 1. Following power application, make MODE and /CS high level during the wait time interval.

2. Following power application, make MODE high level during the wait time and three read operations.

3. The read operation must satisfy the specs described on page 10 (Read Cycle (BC Version)).

4. The address is don't care (V_{IH} or V_{IL}) during read operation.

5. Read operation must be executed with toggled the /CS pin.

6. To prevent bus contention, it is recommended to set /OE to high level.

7. Do not input data to the I/O pins if /OE is low level during a read operation.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 Note to +3.3	V
Input / Output voltage	V_T		–0.5 Note to V_{CC} + 0.4 (3.3 V MAX).	V
Operating ambient temperature	T_A		–20 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –1.0 V (MIN.) (Pulse width: 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD4616112-BCxx		Unit
			MIN.	MAX.	
Supply voltage	V_{CC}		2.6	3.0	V
High level input voltage	V_{IH}		0.8V_{CC}	V_{CC}+0.3	V
Low level input voltage	V_{IL}		–0.3 Note	0.2V_{CC}	V
Operating ambient temperature	T_A		–20	+70	°C

Note –0.5 V (MIN.) (Pulse width: 30 ns)

Capacitance (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			8	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN}: Input voltage

$V_{I/O}$: Input / Output voltage

2. These parameters are not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

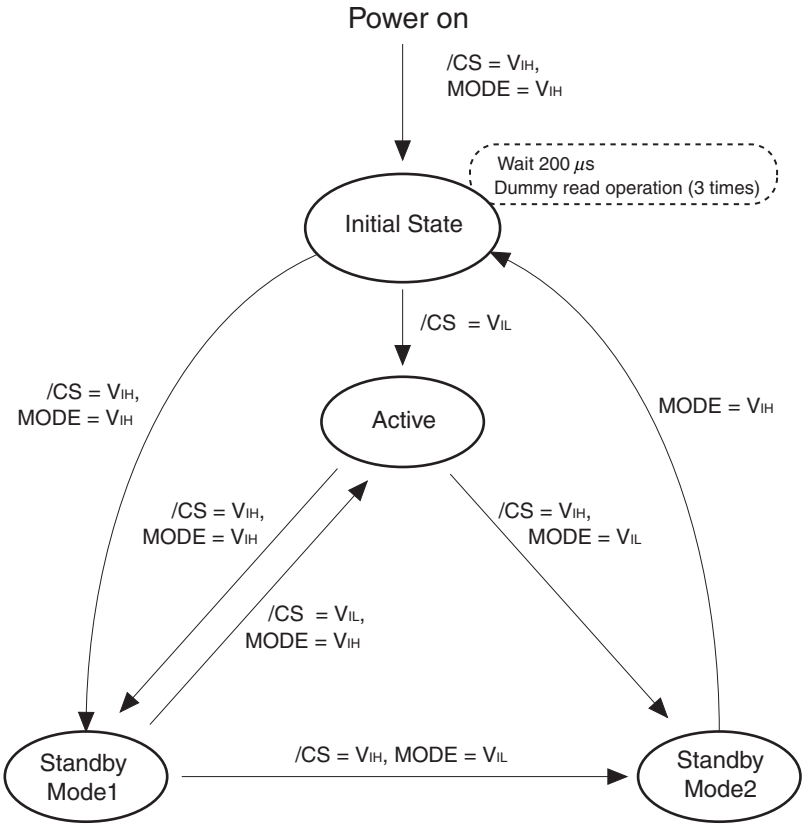
Parameter	Symbol	Test condition	μPD4616112-BCxx			Unit
			MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CS = V_{IH} or /WE = V_{IL} or /OE = V_{IH}	–1.0		+1.0	μA
Operating supply current	I_{CCA}	/CS = V_{IL}, Minimum cycle time, $I_{I/O}$ = 0 mA			35	mA
Standby supply current	I_{SB1}	/CS ≥ V_{CC} – 0.2 V, MODE ≥ V_{CC} – 0.2 V			100	μA
	I_{SB2}	/CS ≥ V_{CC} – 0.2 V, MODE ≤ 0.2 V			10	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA	0.8V_{CC}			V
Low level output voltage	V_{OL}	I_{OL} = 1 mA			0.2V_{CC}	V

Remarks 1. V_{IN}: Input voltage

$V_{I/O}$: Input / Output voltage

2. These DC characteristics are in common regardless of product classifications.

Standby Mode State Machine



Standby Mode Characteristics

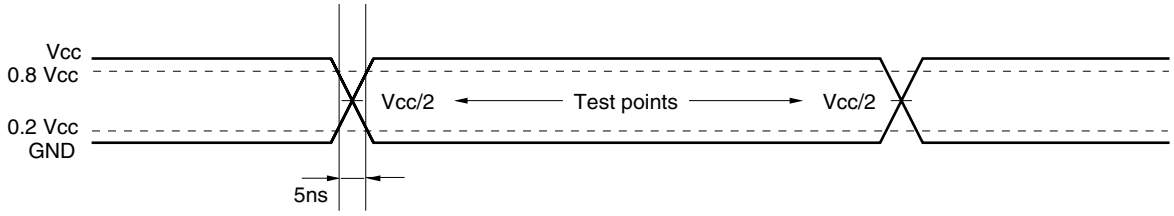
Standby Mode	Memory Cell Data Hold	Standby Supply Current (μA)
Mode 1	Valid	100 (I_{SB1})
Mode 2	Invalid	10 (I_{SB2})

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

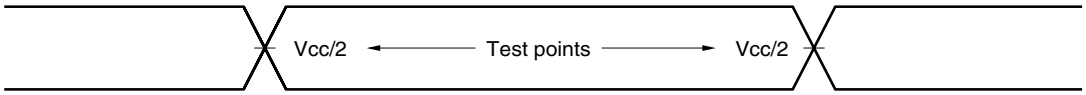
AC Test Conditions

[μPD4616112-BC80, μPD4616112-BC90]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



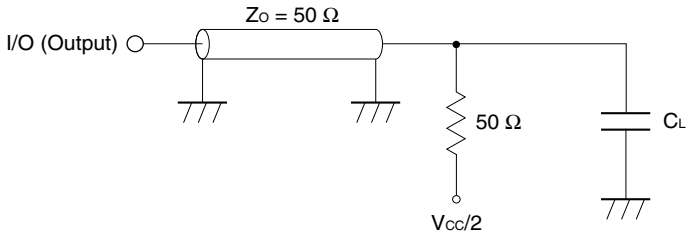
Output Load

AC characteristics directed with the note should be measured with the output load shown in **Figure 1**.

Figure 1

C_L: 50 pF

5 pF (t_{CLZ}, t_{OLZ}, t_{BLZ}, t_{CHZ}, t_{OHZ}, t_{BHZ}, t_{WHZ}, t_{OW})



Read Cycle (BC version)

Parameter	Symbol	μPD4616112-BC80		μPD4616112-BC90		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	80	10,000	90	10,000	ns	1
Identical address read cycle time	t_{RC1}	80	10,000	90	10,000	ns	2
Address skew time	t_{SKEW}		10		20	ns	3
/CS pulse width	t_{CP}	10		10		ns	
Address access time	t_{AA}		80		90	ns	4
/CS access time	t_{ACS}		80		90	ns	
/OE to output valid	t_{OE}		35		40	ns	5
/LB, /UB to output valid	t_{BA}		35		40	ns	
Output hold from address change	t_{OH}	10		10		ns	
/CS to output in low impedance	t_{CLZ}	10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	5		5		ns	
/CS to output in high impedance	t_{CHZ}		25		25	ns	
/OE to output in high impedance	t_{OHZ}		25		25	ns	
/LB, /UB to output in high impedance	t_{BHZ}		25		25	ns	

Notes 1. One read cycle (t_{RC}) must satisfy the minimum value ($t_{RC(MIN.)}$) and maximum value ($t_{RC(MAX.)}$ = 10 μs). t_{RC} indicates the time from the /CS low level input point or address change start point, whichever is later, to the /CS high level input point or the next address change start point, whichever is earlier. As a result, there are the following four conditions for t_{RC}.

1) Time from address change start point to /CS high level input point (address access)
2) Time from address change start point to next address change start point (address access)
3) Time from /CS low level input point to next address change start point (/CS access)
4) Time from /CS low level input point to /CS high level input point (/CS access)

2. The identical address read cycle time (t_{RC1}) is the cycle time of one read operation when performing continuous read operations toggling /OE , /LB, and /UB with the address fixed and /CS low level. Perform settings so that the sum (t_{RC}) of the identical address read cycle times (t_{RC1}) is 10 μs or less.

3. t_{SKEW} indicates the following three types of time depending on the condition.

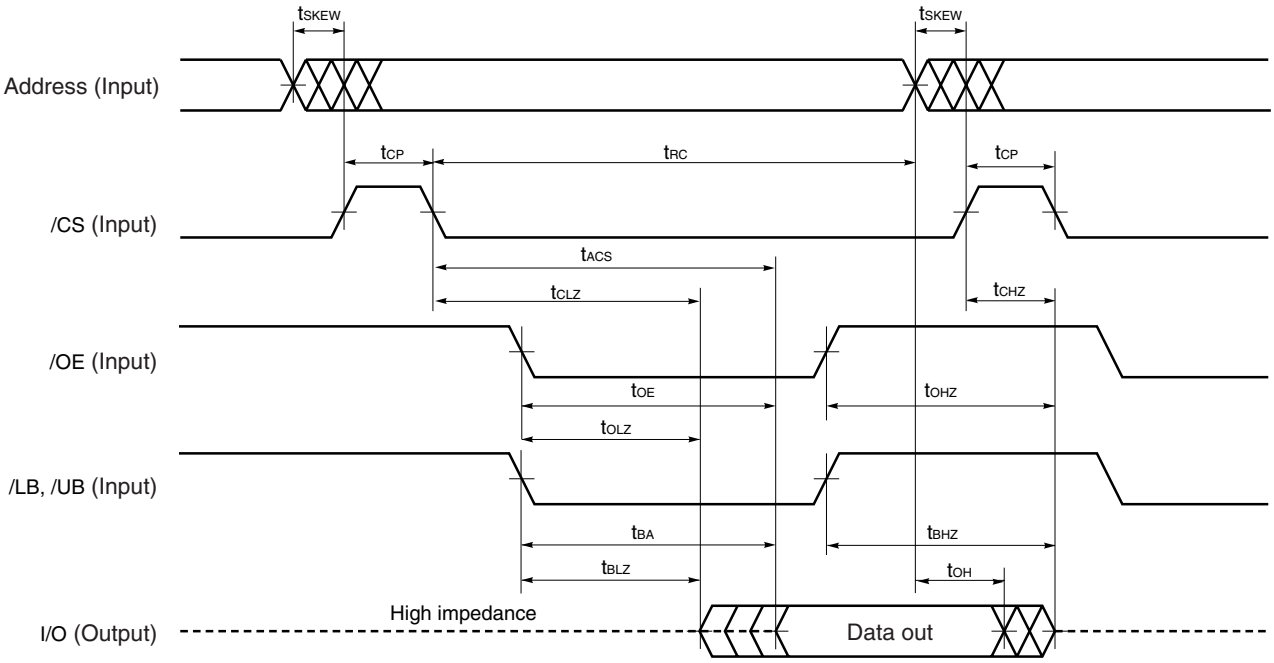
1) When switching /CS from high level to low level, t_{SKEW} is the time from the /CS low level input point until the next address is determined.
2) When switching /CS from low level to high level, t_{SKEW} is the time from the address change start point to the /CS high level input point.
3) When /CS is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

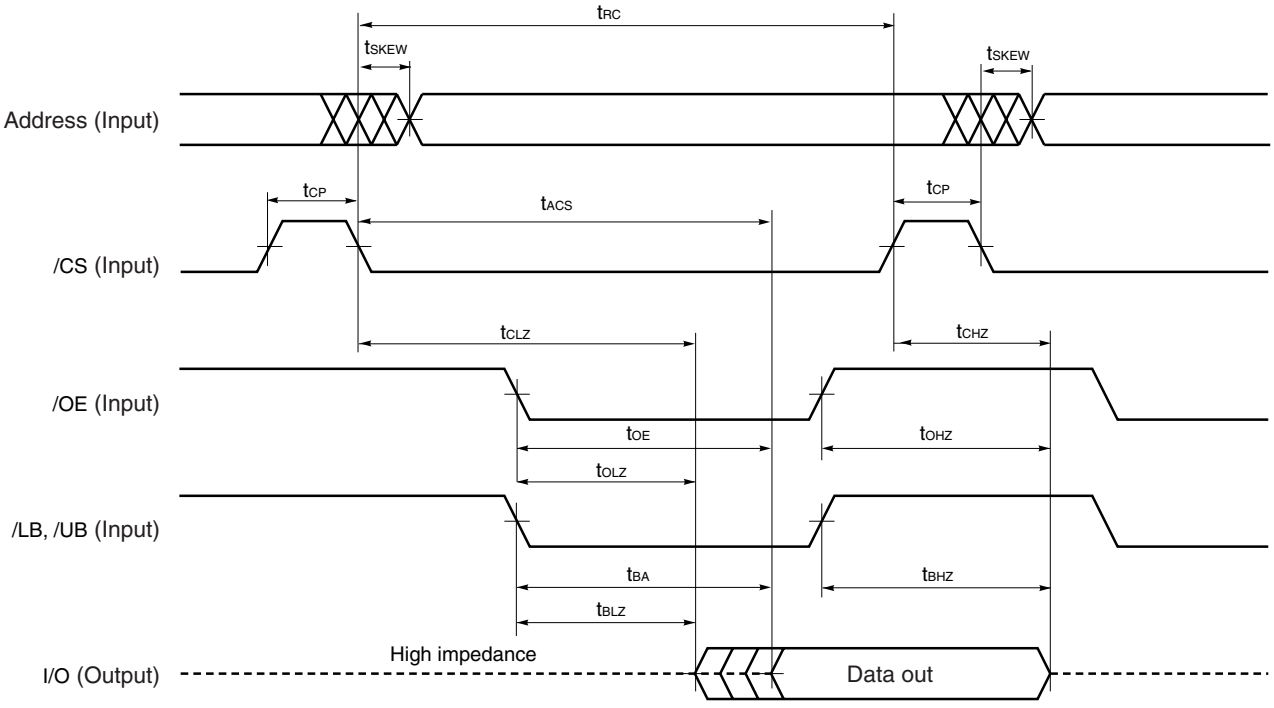
Since specs are defined for t_{SKEW} only when /CS is active, t_{SKEW} is not subject to limitations when /CS is switched from high level to low level following address determination, or when the address is changed after /CS is switched from low level to high level.

4. Regarding t_{AA} and t_{ACS}, only t_{AA} is satisfied during address access (refer to 1) and 2) of **Note 1**), and only t_{ACS} is satisfied during /CS access (refer to 3) of **Note 1**).

5. Regarding t_{BA} and t_{OE}, only t_{BA} is satisfied if /OE becomes active later than /UB and /LB, and only t_{OE} is satisfied if /UB and /LB become active before /OE.

Read Cycle Timing Chart 1

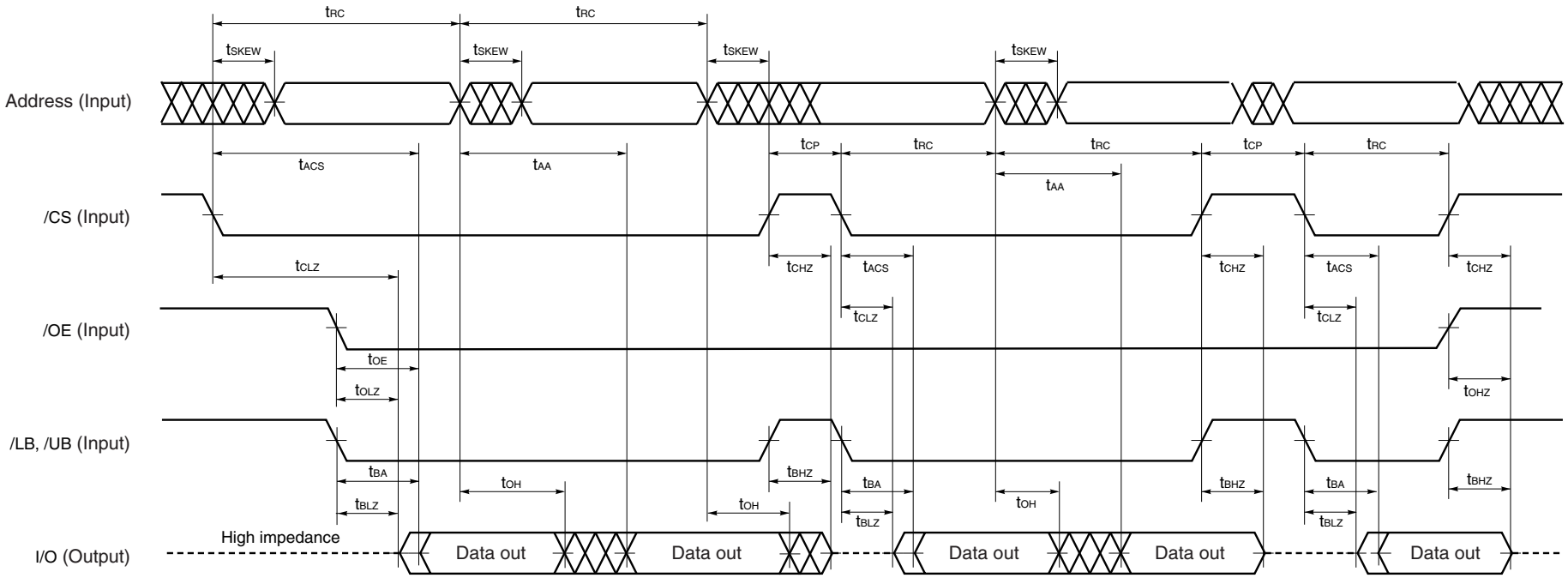




Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Remark In read cycle, /WE should be fixed to High.

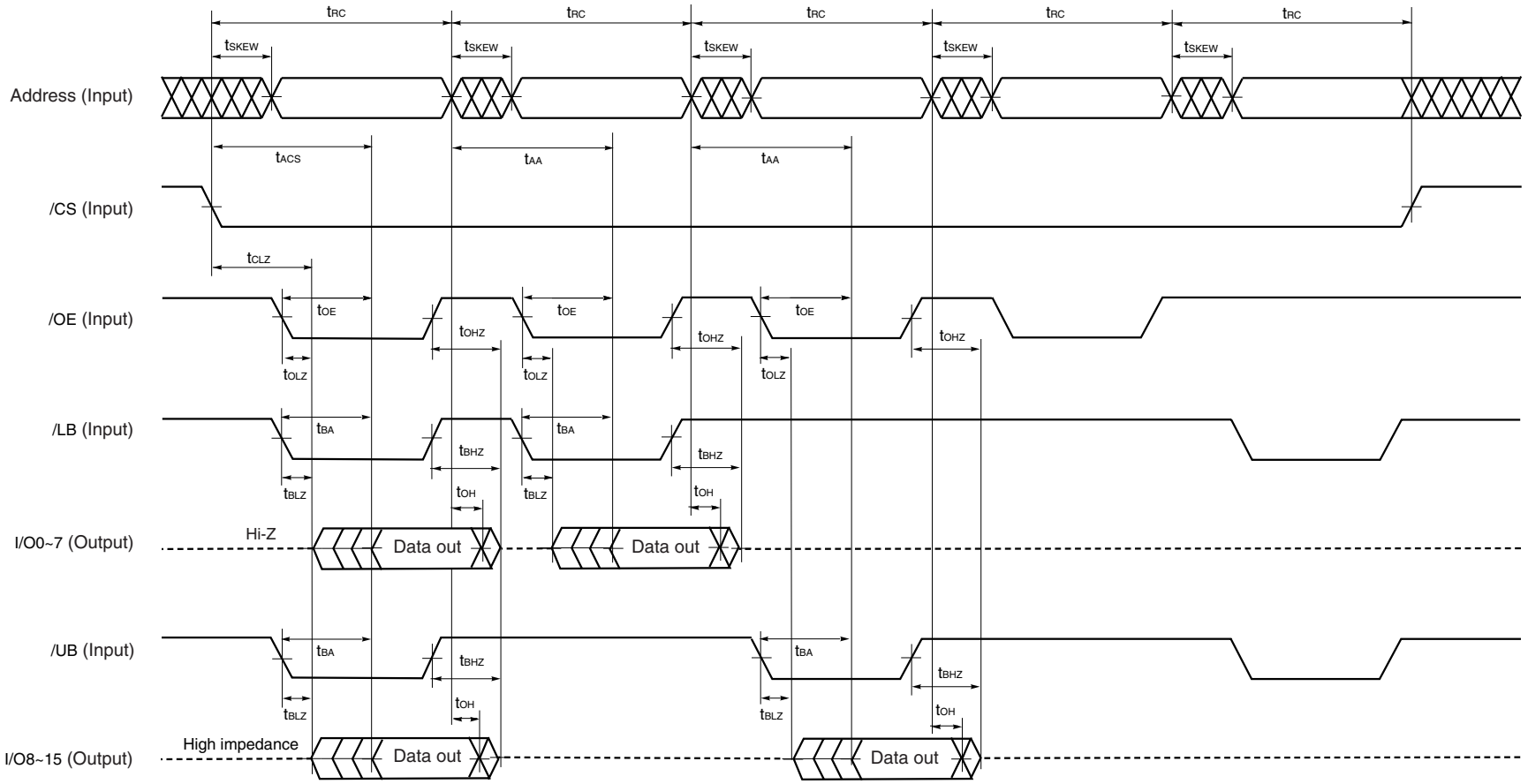
Read Cycle Timing Chart 2



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Remark In read cycle, /WE should be fixed to High.

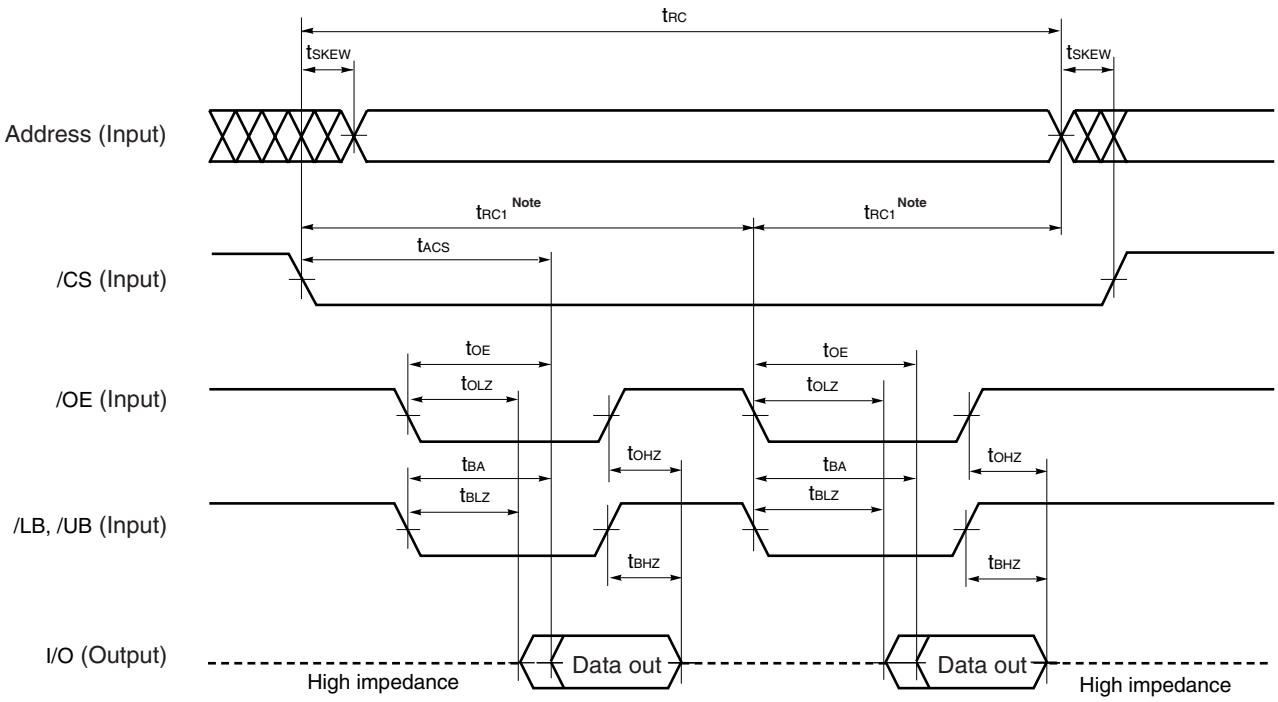
Read Cycle Timing Chart 3



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Remark In read cycle, /WE should be fixed to High.

Read Cycle Timing Chart 4



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Note To perform a continuous read toggling /OE, /UB, and /LB with /CS low level at an identical address, make settings so that the sum (t_{RC}) of the identical address read cycle times (t_{RC1}) is 10 μs or less.

Remark In read cycle, /WE should be fixed to High.

Write Cycle (BC version)

Parameter	Symbol	μPD4616112-BC80		μPD4616112-BC90		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	80	10,000	90	10,000	ns	1
Identical address write cycle time	t_{WC1}	80	10,000	90	10,000	ns	2
Address skew time	t_{SKEW}		10		20	ns	3
/CS to end of write	t_{CW}	40		50		ns	4
/LB, /UB to end of write	t_{BW}	30		35		ns	
Address valid to end of write	t_{AW}	35		45		ns	
Write pulse width	t_{WP}	30		35		ns	
Write recovery time	t_{WR}	20		20		ns	5
/CS pulse width	t_{CP}	10		10		ns	
Address setup time	t_{AS}	0		0		ns	
Byte write hold time	t_{BWH}	20		20		ns	
Data valid to end of write	t_{DW}	20		25		ns	
Data hold time	t_{DH}	0		0		ns	
/OE to output in low impedance	t_{OLZ}	5		5		ns	
/WE to output in high impedance	t_{WHZ}		25		25	ns	
/OE to output in high impedance	t_{OHZ}		25		25	ns	
Output active from end of write	t_{OW}	5		5		ns	

Notes 1. One write cycle (t_{WC}) must satisfy the minimum value ($t_{WC(MIN.)}$) and the maximum value ($t_{WC(MAX.)}$ = 10 μs).

t_{WC} indicates the time from the /CS low level input point or address change start point, whichever is after, to the /CS high level input point or the next address change start point, whichever is earlier. As a result, there are the following four conditions for t_{WC}.

1) Time from address change start point to /CS high level input point
2) Time from address change start point to next address change start point
3) Time from /CS low level input point to next address change start point
4) Time from /CS low level input point to /CS high level input point

2. The identical address read cycle time (t_{WC1}) is the cycle time of one write cycle when performing continuous write operations with the address fixed and /CS low level, changing /LB and /UB at the same time, and toggling /WE, as well as when performing a continuous write toggling /LB and /UB. Make settings so that the sum (t_{WC}) of the identical address write cycle times (t_{WC1}) is 10 μs or less.

3. t_{SKEW} indicates the following three types of time depending on the condition.

1) When switching /CS from high level to low level, t_{SKEW} is the time from the /CS low level input point until the next address is determined.
2) When switching /CS from low level to high level, t_{SKEW} is the time from the address change start point to the /CS high level input point.
3) When /CS is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CS is active, t_{SKEW} is not subject to limitations when /CS is switched from high level to low level following address determination, or when the address is changed after /CS is switched from low level to high level.

4. Definition of write start and write end

	/CS	/WE	/LB, /UB	Status
Write start pattern 1	H to L	L	L	If /WE, /LB, /UB are low level, time when /CS changes from high level to low level
Write start pattern 2	L	H to L	L	If /CS, /LB, /UB are low level, time when /WE changes from high level to low level
Write start pattern 3	L	L	H to L	If /CS, /WE are low level, time when /LB or /UB changes from high level to low level
Write end pattern 1	L	L to H	L	If /CS, /WE, /LB, /UB are low level, time when /WE changes from low level to high level
Write end pattern 2	L	L	L to H	When /CS, /WE, /LB, /UB are low level, time when /LB or /UB changes from low level to high level

5. Definition of write end recovery time (t_{WR})

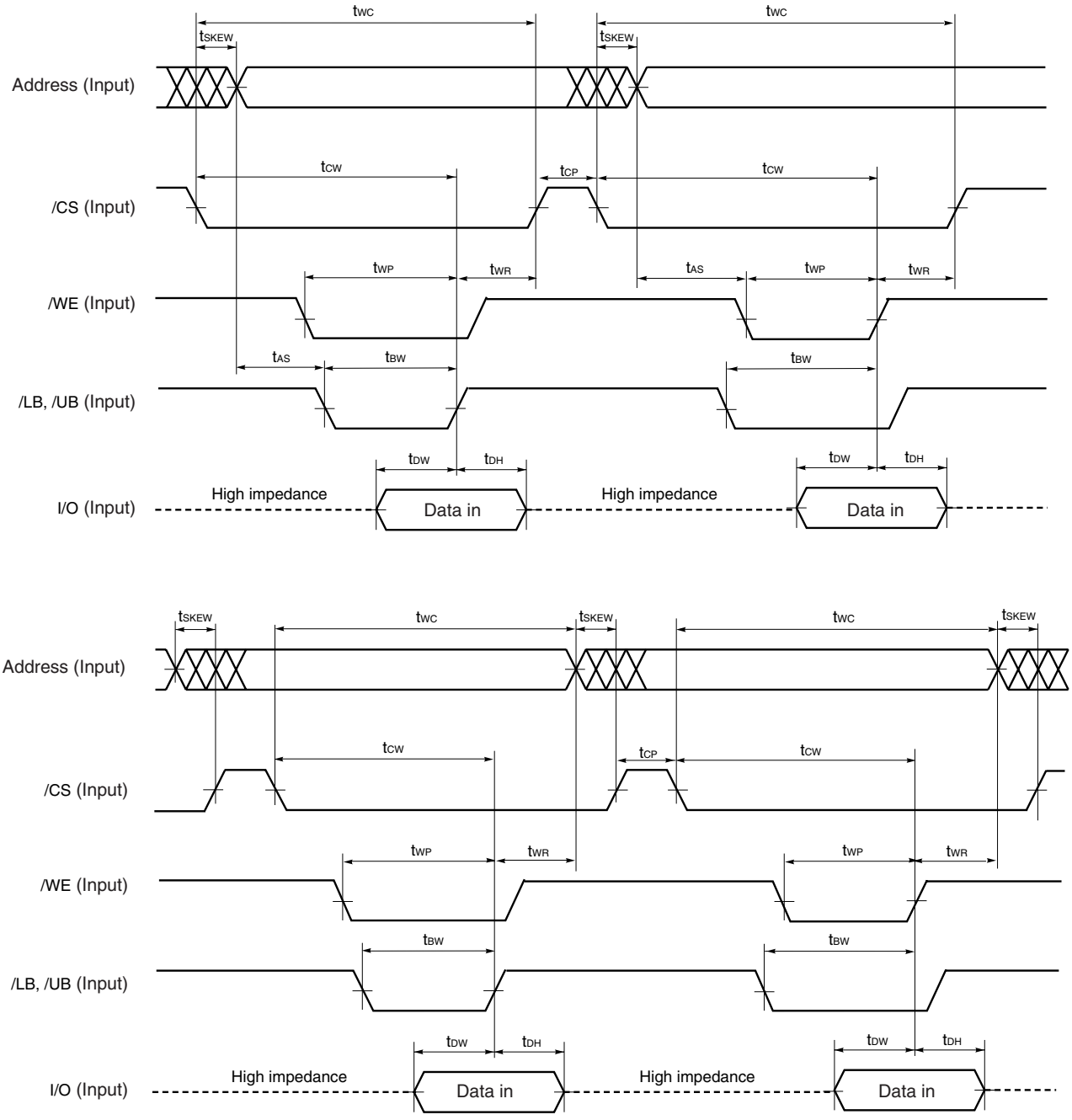
1) Time from write end to address change start point, or from write end to /CS high level input point

2) When /CS, /LB, /UB are low level and continuously written to the identical address, time from /WE high level input point to /WE low level input point

3) When /CS, /WE are low level and continuously written to the identical address, time from /LB or /UB high level input point, whichever is later, to /LB or /UB low level input point, whichever is earlier.

4) When /CS is low level and continuously written to the identical address, time from write end to point at which /WE , /LB, or /UB starts to change from high level to low level, whichever is earliest.

Write Cycle Timing Chart 1



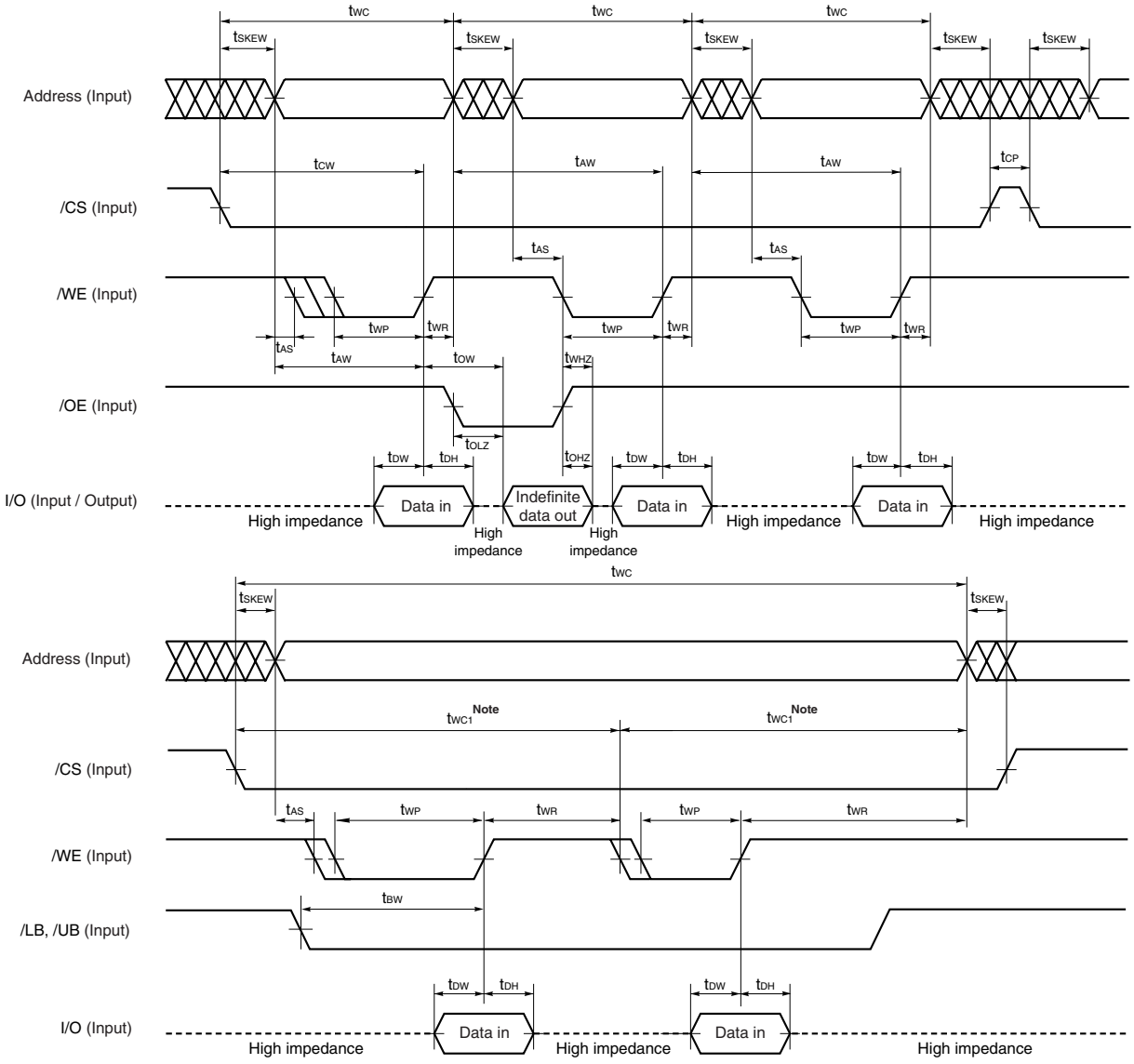
Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

<R> **Write Cycle Timing Chart 2 (/WE Controlled)**



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

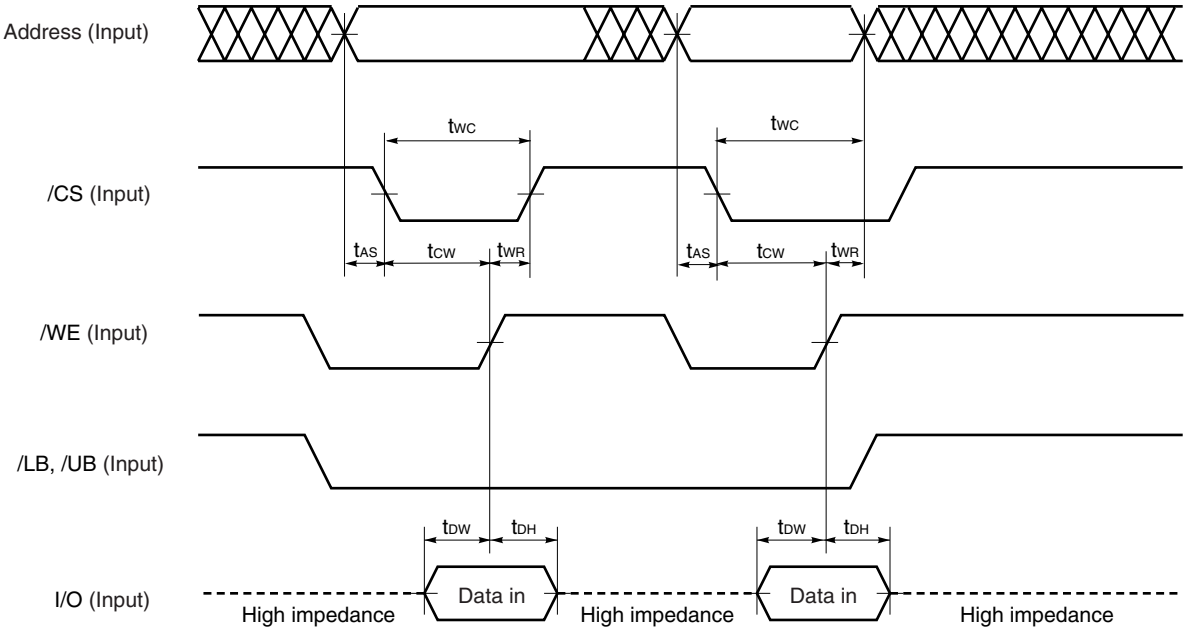
3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

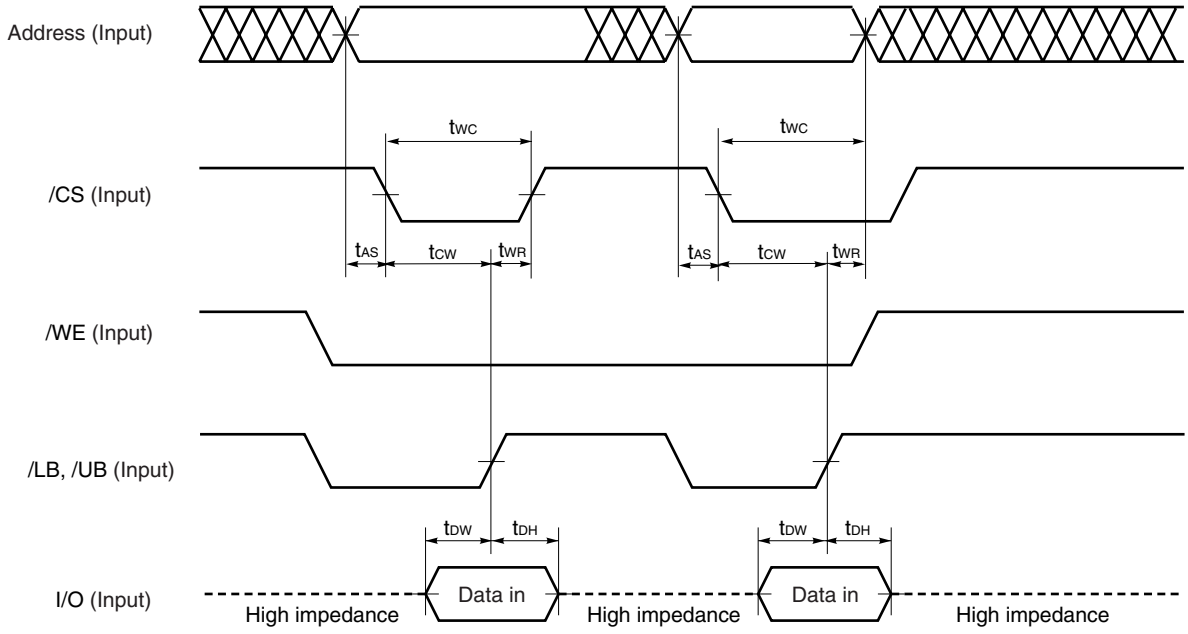
Note If /LB and /UB are changed at the same time with /CS low level and a continuous write operation toggling /WE is performed, make settings so that the sum (t_{WC}) of the identical address write cycle time (t_{WC1}) is 10 μs or less.

Remarks 1. Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

2. When /WE is at Low, the I/O pins are always high impedance. When /WE is at High, read operation is executed. Therefore /OE should be at High to make the I/O pins high impedance.

Write Cycle Timing Chart 3 (/CS Controlled)





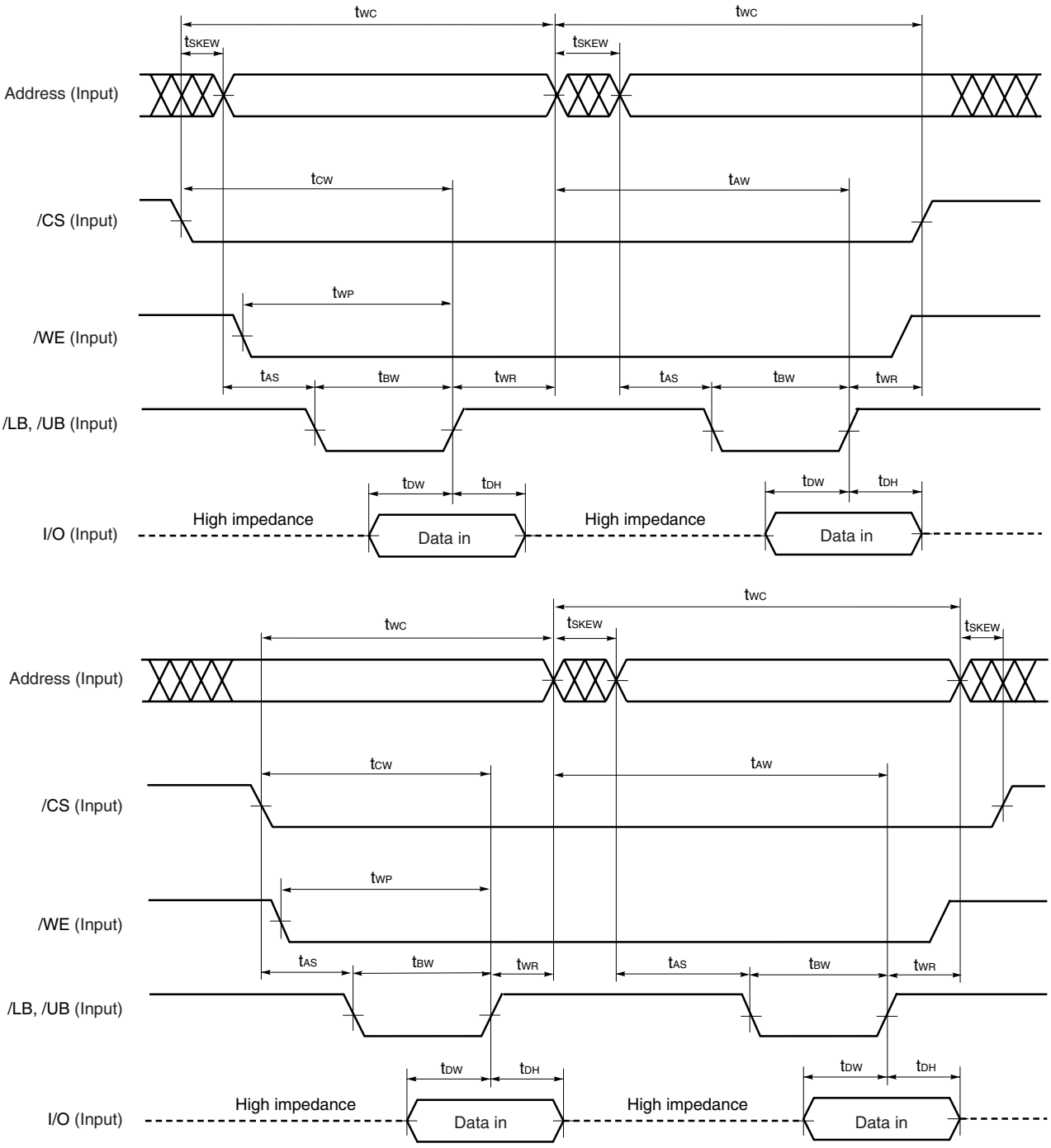
Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Write Cycle Timing Chart 4 (/LB, /UB Controlled 1)



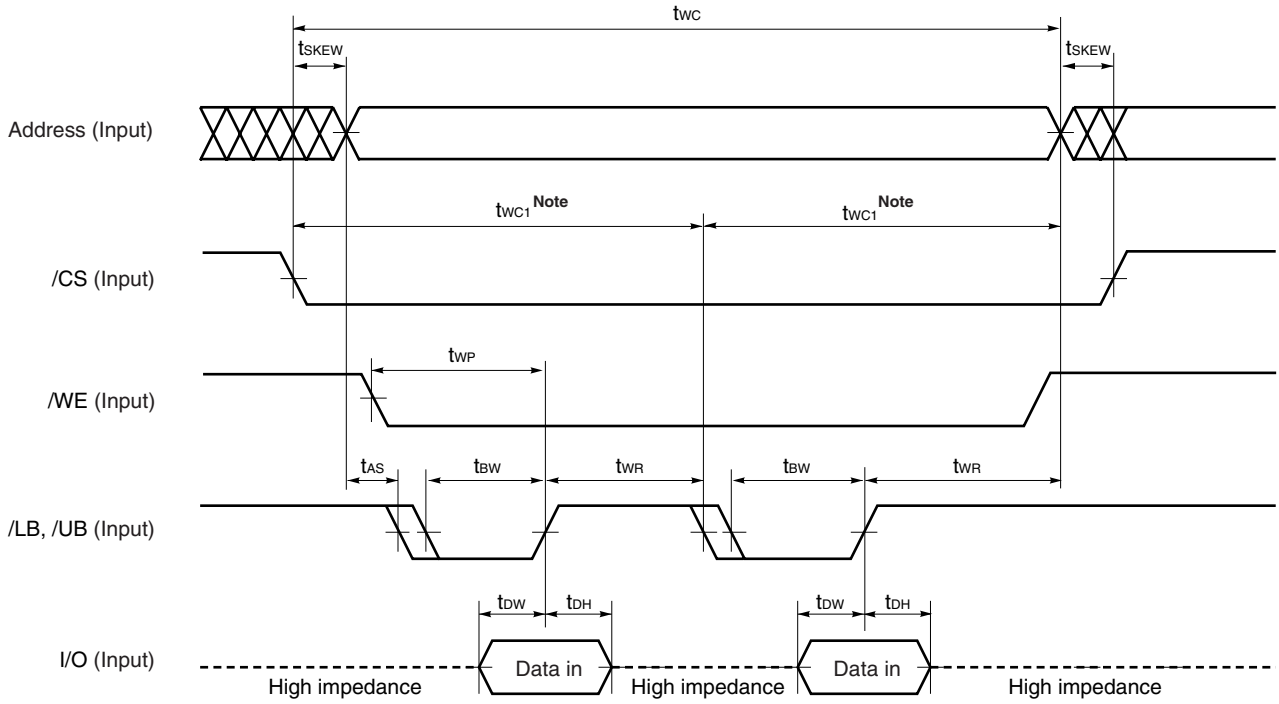
Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Write Cycle Timing Chart 5 (/LB, /UB Controlled 2)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

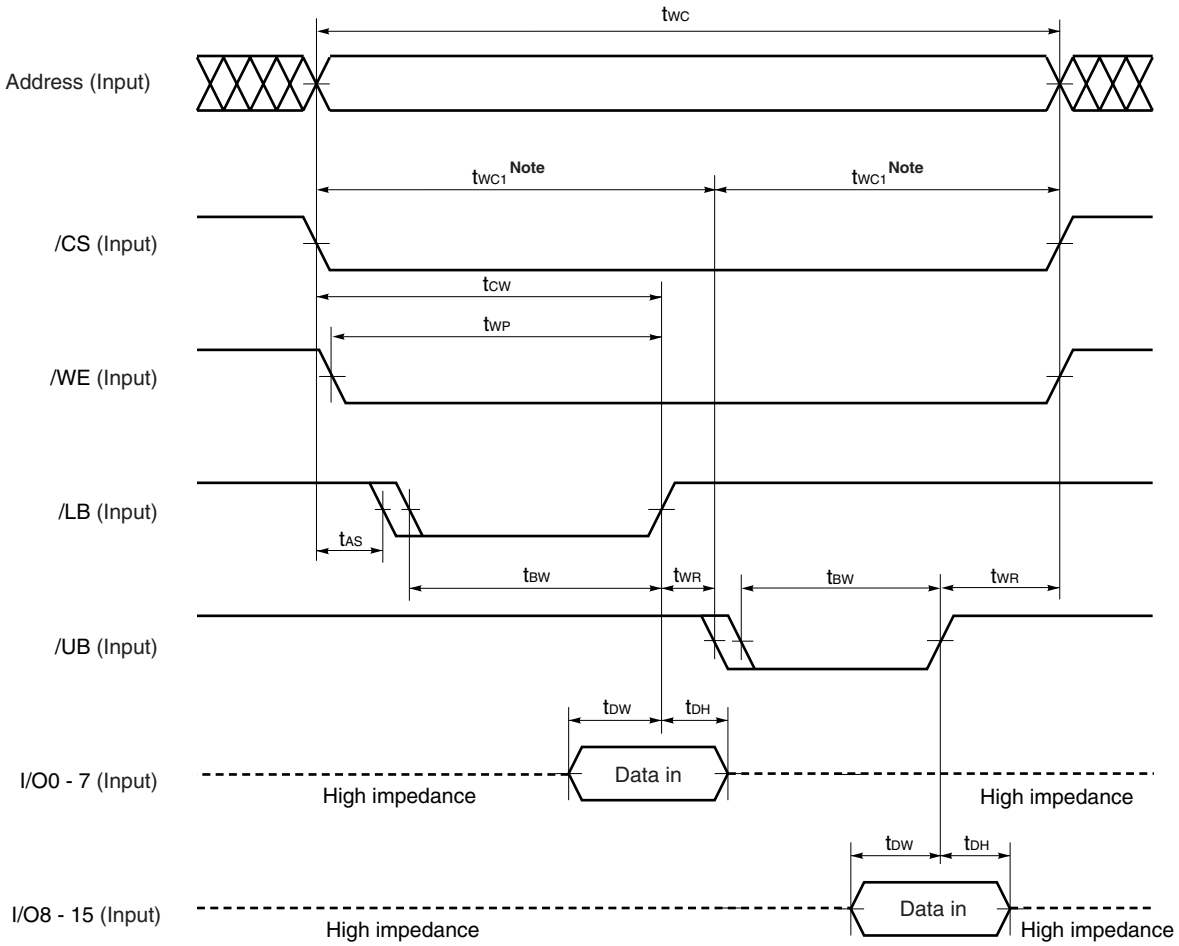
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Note If /LB and /UB are changed at the same time with /CS low level and a continuous write operation toggling /WE is performed, make settings so that the sum (t_{WC}) of the identical address write cycle time (t_{WC1}) is 10 μs or less.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Write Cycle Timing Chart 6 (/LB, /UB Independent Controlled 1)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

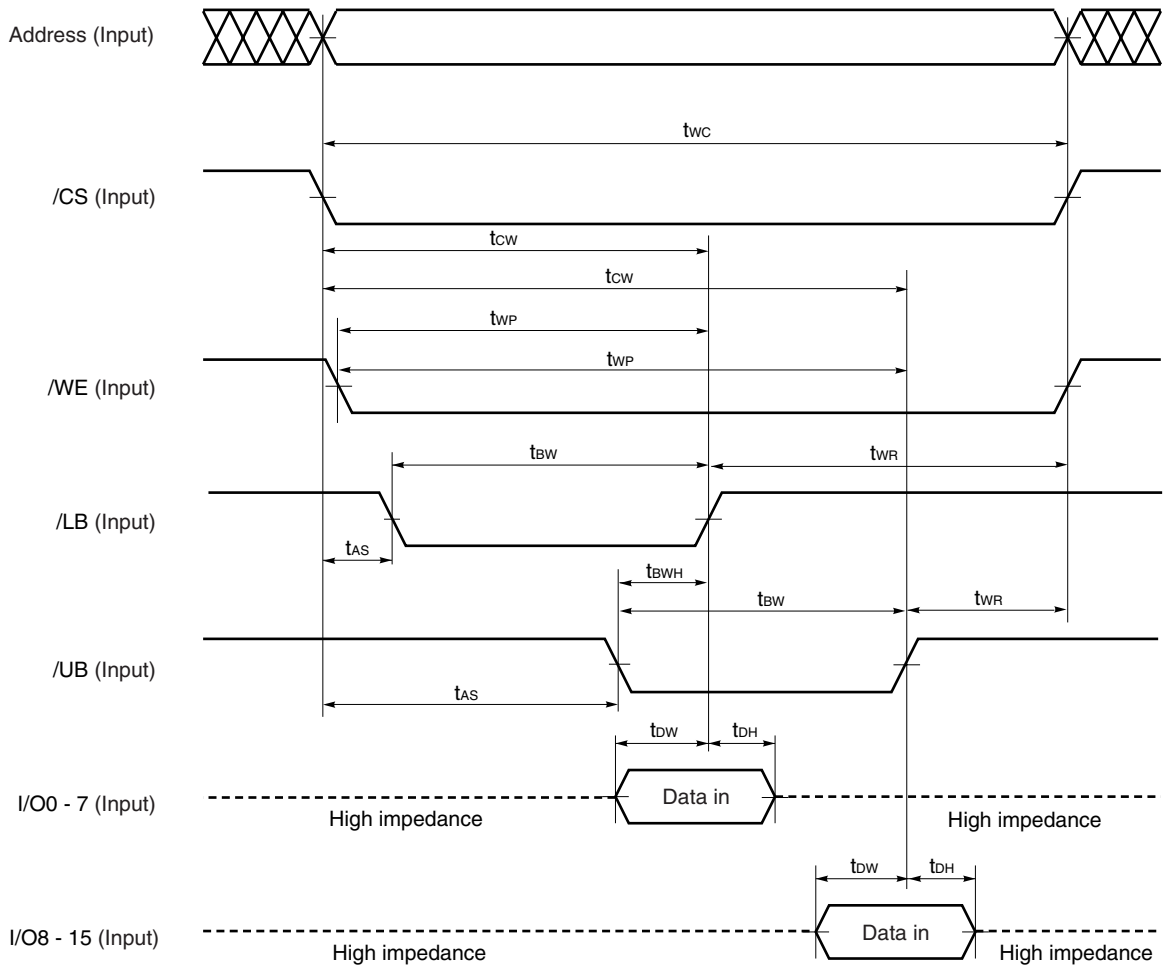
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Note If /LB and /UB are changed at the same time with /CS low level and a continuous write operation toggling /WE is performed, make settings so that the sum (t_{WC}) of the identical address write cycle time (t_{WC1}) is 10 μs or less.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Write Cycle Timing Chart 7 (/LB, /UB Independent Controlled 2)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

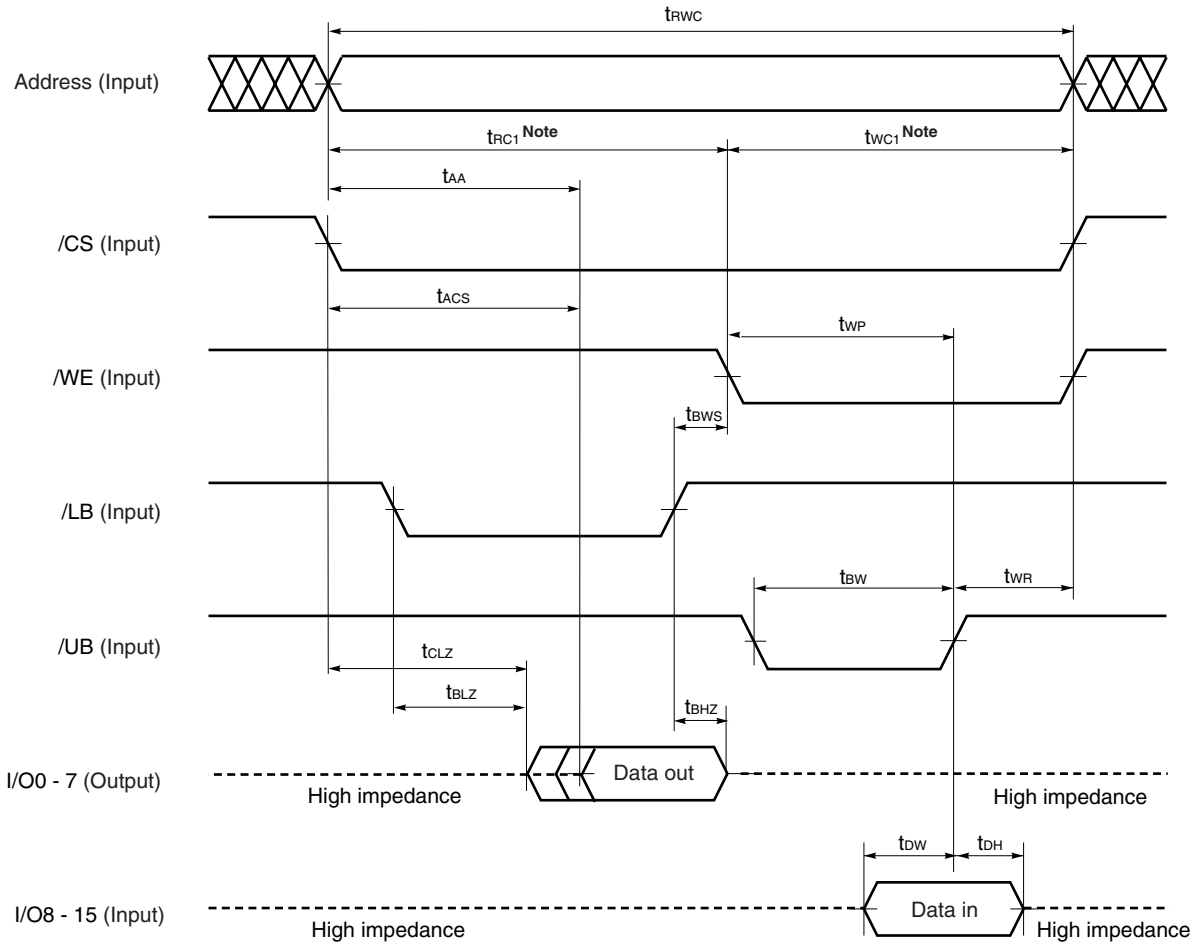
Read Write Cycle (BC version)

Parameter	Symbol	MIN.	MAX.	Unit	Notes
Read write cycle time	t_{RWC}		10,000	ns	1, 2
Byte write setup time	t_{BWS}	20		ns	
Byte read setup time	t_{BRS}	20		ns	

Notes 1. Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CS low level, or when a write is performed using /LB following a read using /UB.

2. Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a read is performed at the identical address using /UB following a write using /LB with /CS low level, or when a read is performed using /LB following a write using /UB.

Read Write Cycle Timing Chart 1 (/LB, /UB Independent Controlled 1)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

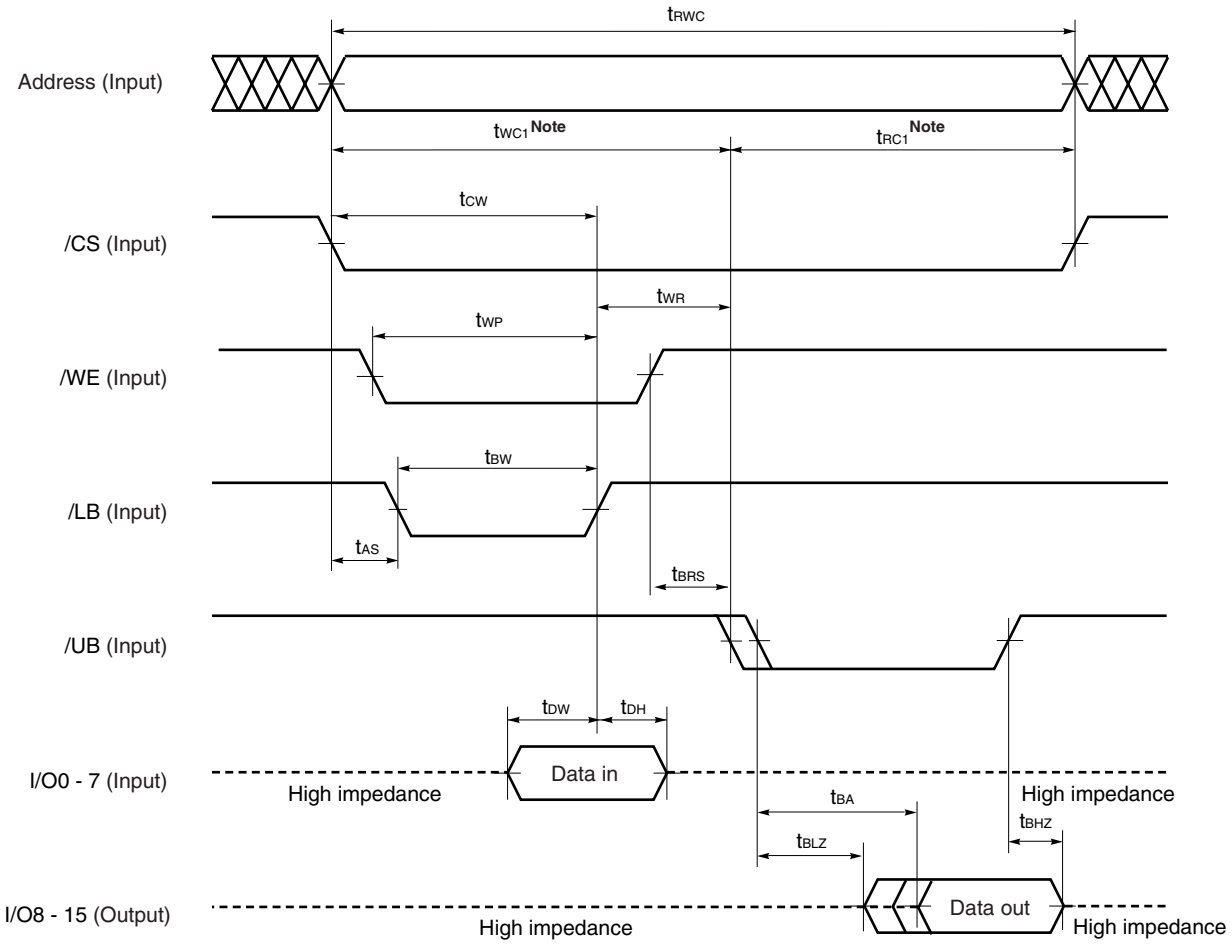
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}), none of the data can be guaranteed.

Note Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CS low level, or when a write is performed using /LB following a read using /UB.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Read Write Cycle Timing Chart 2 (/LB, /UB Independent Controlled 2)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

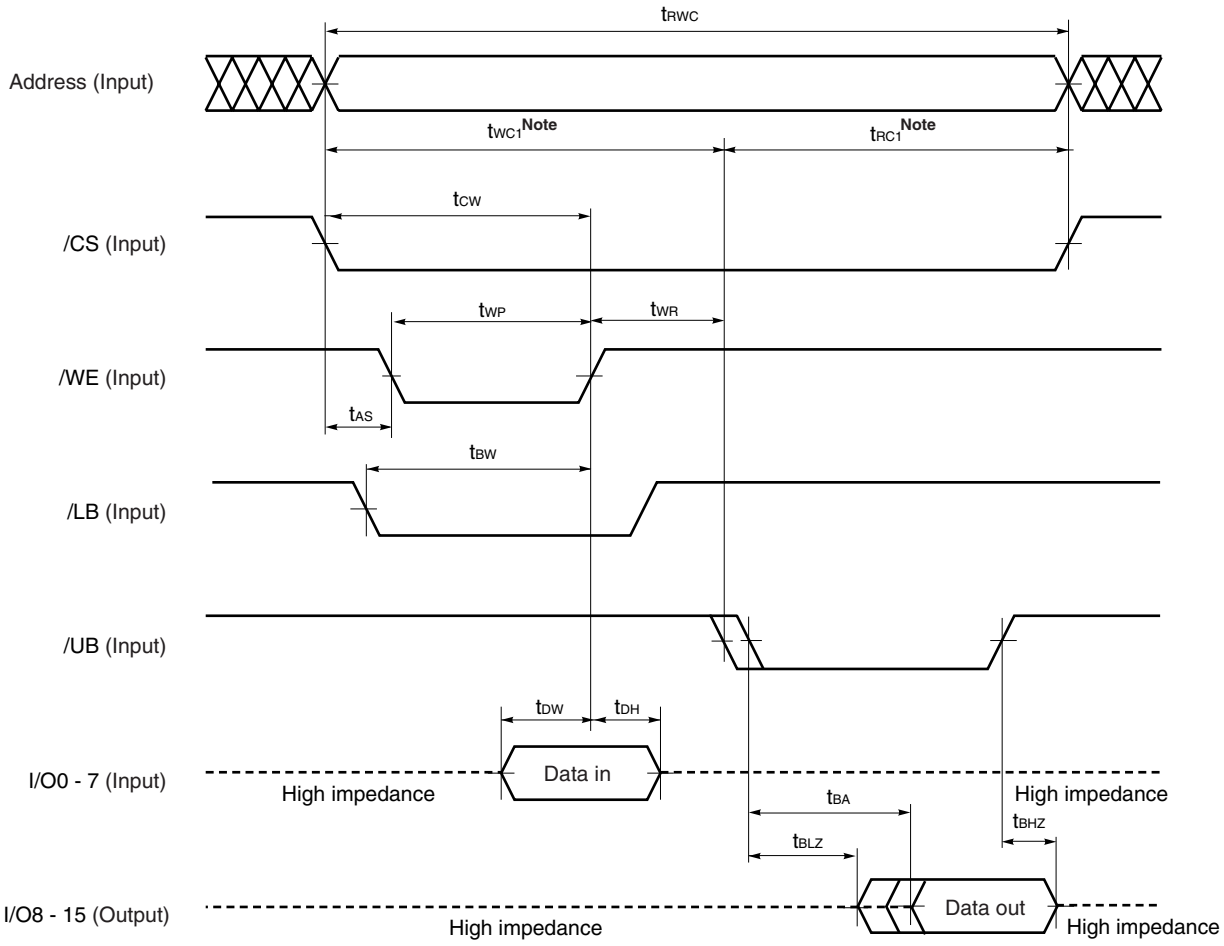
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}), none of the data can be guaranteed.

Note Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CS low level, or when a write is performed using /LB following a read using /UB.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Read Write Cycle Timing Chart 3 (/LB, /UB Independent Controlled 3)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

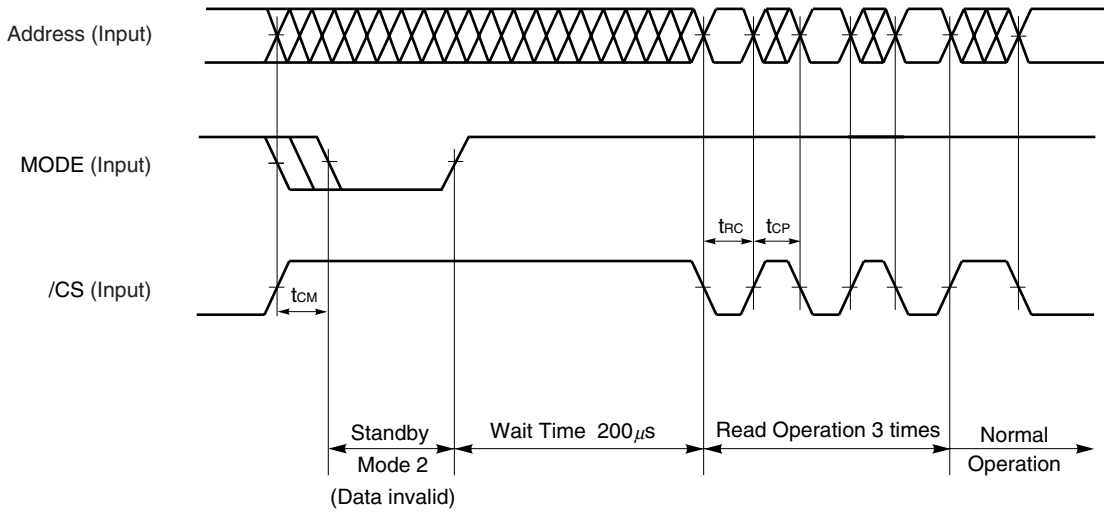
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}), none of the data can be guaranteed.

Note Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CS low level, or when a write is performed using /LB following a read using /UB.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Standby Mode 2 entry and recovery Timing Chart



Parameter	Symbol	MIN.	MAX.	Unit	Note
/CS High to MODE Low	t_{CM}	0		ns	

Cautions 1. Make MODE and /CS high level during the wait time.

2. Make MODE high level during the wait time and three read operations.

3. The read operation must satisfy the specs described on page 10 (Read Cycle (BC Version)).

4. The read operation address can be either V_{IH} or V_{IL}.

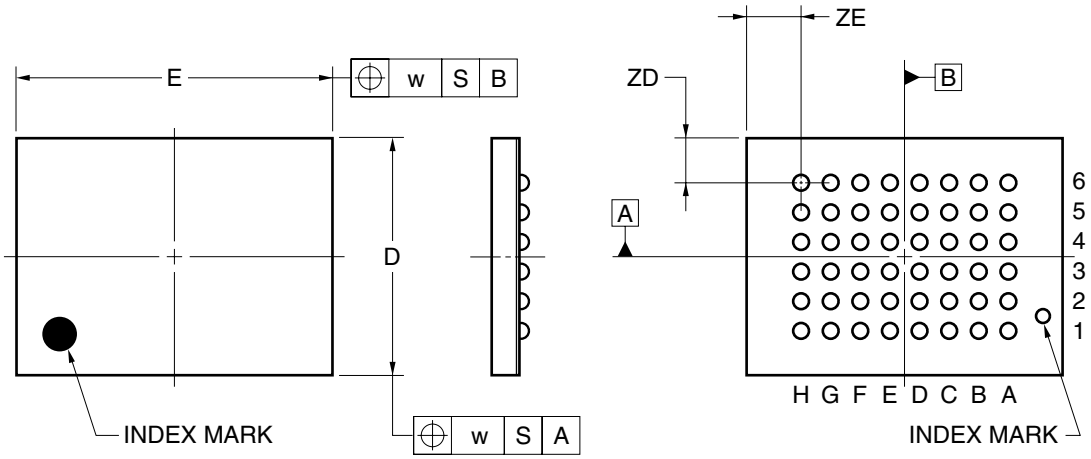
5. Perform reading by toggling /CS.

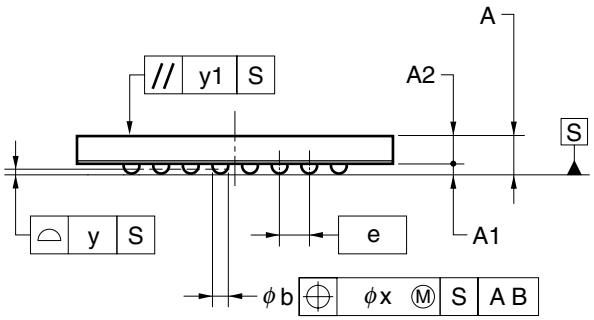
6. To prevent bus contention, it is recommended to set /OE to high level.

7. Do not input data to the I/O pins if /OE is low level during a read operation.

Package Drawing

48-PIN TAPE FBGA (8x6)





ITEM	MILLIMETERS
D	6.0±0.1
E	8.0±0.1
w	0.2
e	0.75
A	0.94±0.10
A1	0.24±0.05
A2	0.70
b	0.40±0.05
x	0.08
y	0.1
y1	0.2
ZD	1.125
ZE	1.375

P48F9-75-BC2

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD4616112.

Type of Surface Mount Device

μPD4616112F9-BCxx-BC2 : 48-pin TAPE FBGA (8 x 6)

<R> μPD4616112F9-BCxx-BC2-A : 48-pin TAPE FBGA (8 x 6)

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
6th edition/ Feb. 2006	p.2	p.2	Addition	Ordering Information	Lead-free products have been added
	p.2	p.2	Modification	Marking Image	Marking Image has been modified
	p.18	p.18	Modification	Write Cycle Timing Chart 2	Timing Chart has been modified
	p.30	p.30	Addition	Recommended Soldering Conditions	Lead-free products have been added

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

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