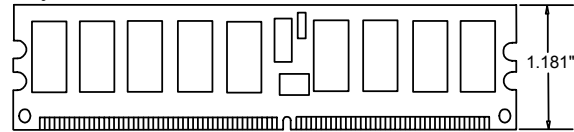
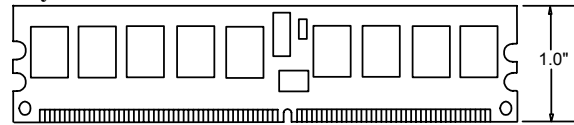


**256MB - W1D32M72R8**  
**512MB - W1D64M72R8**  
**1GB - W1D128M72R8**  
**2GB - W1D256M72R8 (Preliminary\*)**

**Features:**

- 240-pin Registered ECC DDR2 SDRAM Dual-In-Line Memory Module for DDR2-400 and DDR2-533
- JEDEC standard VDD=1.8V (+/- 0.1V) power supply
- One rank 256MB, 512MB, 1GB, and 2GB
- Modules are built with 18 x8 DDR2 SDRAM devices in a 60-ball FBGA package
- ECC error detection and correction
- Programmable CAS Latency of 3 and 4; Burst Length of 4 and 8
- Auto Refresh and Self Refresh Mode
- OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)
- SPD (Serial Presence Detect) with EEPROM
- All input/output are SSTL\_18 compatible
- All contacts are gold plated
- One clock delay for register

**Figure 1: Available layouts**
**Layout A:**

**Layout B:**


Front view of double-sided DIMM (see detail physical dimensions at the back)

**Speed Grades:**

Speed Grade	-5	-3.75	Units
Module Speed Grade	PC2-3200	PC2-4200	
Speed @ CL3	400	-	MHz
Speed @ CL4	400	533	MHz
Speed @ CL5	-	533	MHz

Note: See Product ordering for full naming guide

**Description:**

The following specification covers the W1D32M72R8, W1D64M72R8, W1D128M72R8, and W1D256M72R8 family of Single-Rank Registered ECC DDR2 modules using x8 FBGA SDRAMs. Please reference Figure 1 for available layout configurations and the product ordering guide on the final page of this specification for available options including speed grade and silicon manufacturer.

**Address Summary Table:**

	256MB	512MB	1GB	2GB
Module Configuration	32M x 72	64M x 72	128M x 72	256M x 72
Refresh	8k	8K	8K	8K
Device Configuration	32M x 8 (9 components)	64M x 8 (9 components)	128M x 8 (9 components)	256M x 8 (9 components)
Row Addressing	A0-A13	A0-A13	A0-A14	A0-A14
Column Addressing	A0-A9	A0-A9	A0-A9	A0-A9
Module Rank	1	1	1	1

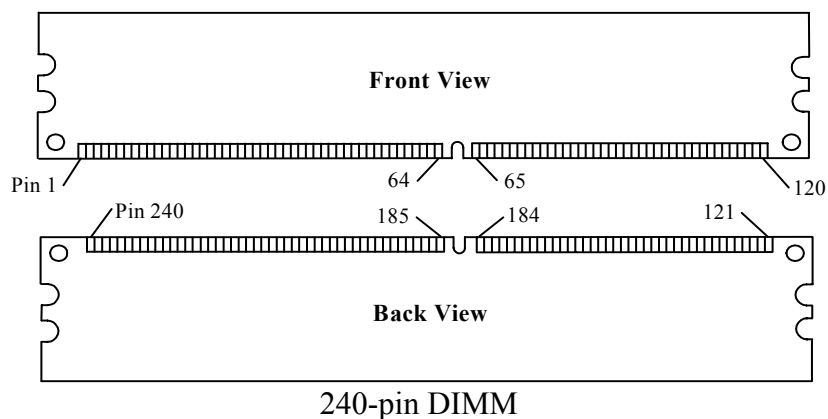
**\*Specifications are for reference purposes only and are subject to change by Wintec without notice.**

**Pin Configuration:**

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	31	DQ19	61	A4	91	VSS	121	VSS	151	VSS	181	VDDQ	211	DM5/DQS14
2	VSS	32	VSS	62	VDDQ	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NC/DQS14#
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	VSS
4	DQ1	34	DQ25	64	VDD	94	VSS	124	VSS	154	VSS	184	VDD	214	DQ46
5	VSS	35	VSS	KEY		95	DQ42	125	DM0/DQS9	155	DM3/DQS12	KEY		215	DQ47
6	DQS0#	36	DQS3#	65	VSS	96	DQ43	126	NC/DQS9#	156	NC/DQS12#	185	CK0	216	VSS
7	DQS0	37	DQS3	66	VSS	97	VSS	127	VSS	157	VSS	186	CK0#	217	DQ52
8	VSS	38	VSS	67	VDD	98	DQ48	128	DQ6	158	DQ30	187	VDD	218	DQ53
9	DQ2	39	DQ26	68	NC	99	DQ49	129	DQ7	159	DQ31	188	A0	219	VSS
10	DQ3	40	DQ27	69	VDD	100	VSS	130	VSS	160	VSS	189	VDD	220	RFU
11	VSS	41	VSS	70	A10/AP	101	SA2	131	DQ12	161	CB4	190	BA1	221	RFU
12	DQ8	42	CB0	71	BA0	102	NC.TEST <sup>1</sup>	132	DQ13	162	CB5	191	VDDQ	222	VSS
13	DQ9	43	CB1	72	VDDQ	103	VSS	133	VSS	163	VSS	192	RAS#	223	DM6/DQS15
14	VSS	44	VSS	73	WE#	104	DQS6#	134	DM1/DQS10	164	DM8/DQS17	193	S0#	224	NC/DQS15#
15	DQS1#	45	DQS8#	74	CAS#	105	DQS6	135	NC/DQS10#	165	NC/DQS17#	194	VDDQ	225	VSS
16	DQS1	46	DQS8	75	VDDQ	106	VSS	136	VSS	166	VSS	195	ODT0	226	DQ54
17	VSS	47	VSS	76	S1#	107	DQ50	137	RFU	167	CB6	196	A13	227	DQ55
18	RESET#	48	CB2	77	ODT1	108	DQ51	138	RFU	168	CB7	197	VDD	228	VSS
19	NC	49	CB3	78	VDDQ	109	VSS	139	VSS	169	VSS	198	VSS	229	DQ60
20	VSS	50	VSS	79	VSS	110	DQ56	140	DQ14	170	VDDQ	199	DQ36	230	DQ61
21	DQ10	51	VDDQ	80	DQ32	111	DQ57	141	DQ15	171	CKE1	200	DQ37	231	VSS
22	DQ11	52	CKE0	81	DQ33	112	VSS	142	VSS	172	VDD	201	VSS	232	DM7/DQS16
23	VSS	53	VDD	82	VSS	113	DQS7#	143	DQ20	173	A15	202	DM4/DQS13	233	NC/DQS16#
24	DQ16	54	A16,BA2	83	DQS4#	114	DQS7	144	DQ21	174	A14	203	NC/DQS13#	234	VSS
25	DQ17	55	NC	84	DQS4	115	VSS	145	VSS	175	VDDQ	204	VSS	235	DQ62
26	VSS	56	VDDQ	85	VSS	116	DQ58	146	DM2/DQS11	176	A12	205	DQ38	236	DQ63
27	DQS2#	57	A11	86	DQ34	117	DQ59	147	NC/DQS11#	177	A9	206	DQ39	237	VSS
28	DQS2	58	A7	87	DQ35	118	VSS	148	VSS	178	VDD	207	VSS	238	VDDSPD
29	VSS	59	VDD	88	VSS	119	SDA	149	DQ22	179	A8	208	DQ44	239	SA0
30	DQ18	60	A5	89	DQ40	120	SCL	150	DQ23	180	A6	209	DQ45	240	SA1
				90	DQ41							210	VSS		

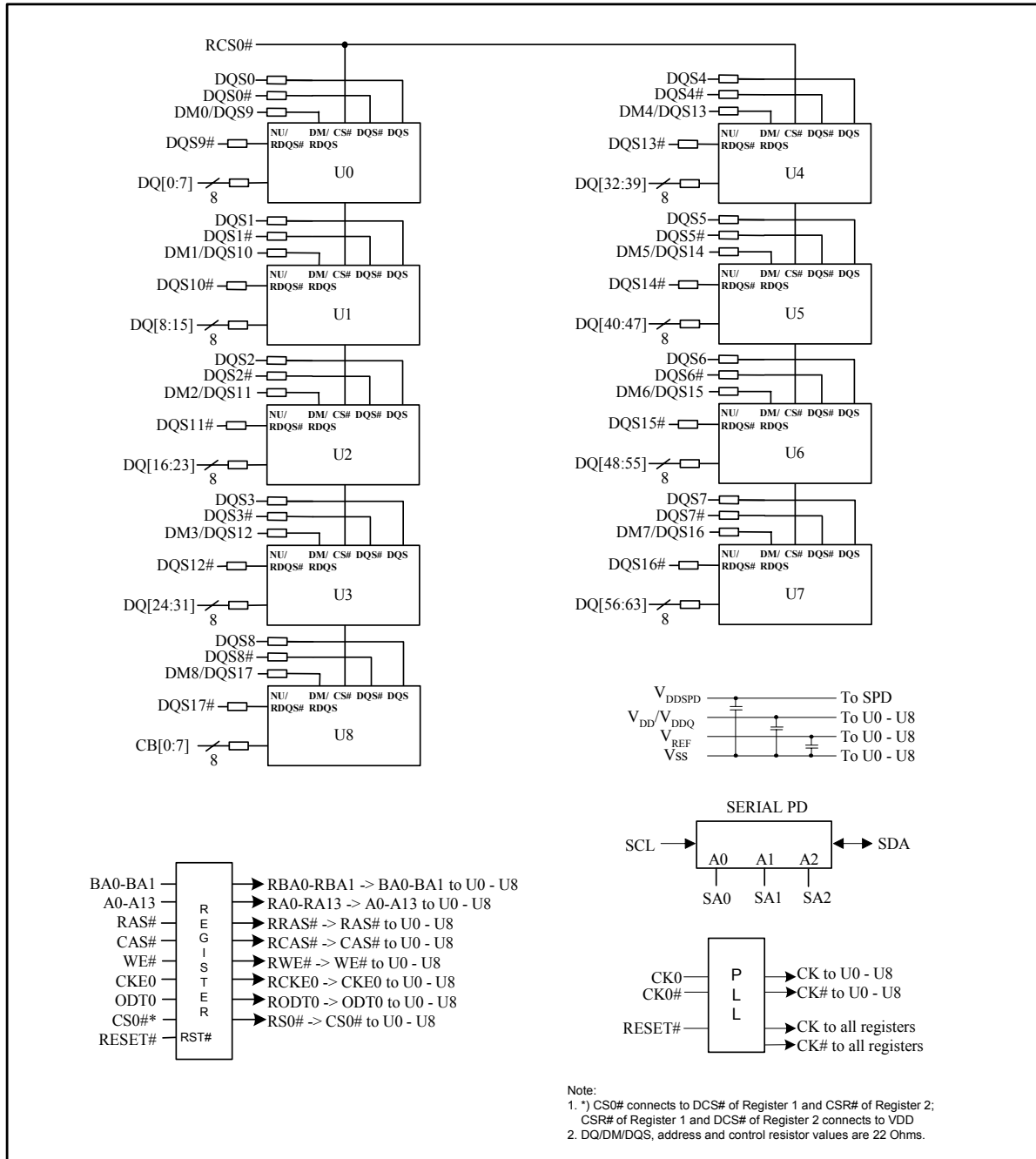
NC - No Connect, RFU - Reserved for Future Use

1. The Test pin (Pin 102) is reserved for bus analysis and is not connected on normal memory modules
2. CKE1 and S1# pin are used for dual-rank Registered DIMM
3. A13 (Pin 196) is for 512MB and above DIMM.

**Pin Locations:**


**Functional Block Diagram:**

Single Rank 32M x 72 (256MB), 64M x 72 (512MB), 128M x 72 (1GB), and 256M x 72 (2GB) DDR2 Registered SDRAM DIMM (x8 organization)



**Absolute Maximum Ratings:**

Exposure to stresses greater than these absolute maximum rating conditions for extended periods may affect reliability of the module.

Symbol	Parameter	Min	Max	Units
$V_{DD}$	$V_{DD}$ supply voltage relative to $V_{SS}$	-1.0	2.3	V
$V_{DDQ}$	$V_{DDQ}$ supply voltage relative to $V_{SS}$	-0.5	2.3	V
$V_{DDL}$	$V_{DDL}$ supply voltage relative to $V_{SS}$	-0.5	2.3	V
$V_{IN}, V_{OUT}$	Voltage on any pin relative to $V_{SS}$	-0.5	2.3	V
$T_{STG}$	Storage temperature ( $T_{case}$ )	-55	+100	°C
$T_{OPR}$	Operating Temperature (Ambient)	0	+55	°C
$I_{IL}$	Input Leakage Current; Any input $0V \leq V_{IN} \leq 0.95V$	-5	5	$\mu A$
$I_{OL}$	Output Leakage Current; $0V \leq V_{OUT} \leq V_{DDQ}$ ; DQS and ODT are disabled	-5	5	$\mu A$

**DC Operating Conditions:**

Parameter	Symbol	Min	Nom	Max	Units	Notes
Supply Voltage	$V_{DD}$	1.7	1.8	1.9	V	1
$V_{DDL}$ Supply Voltage	$V_{DDL}$	1.7	1.8	1.9	V	4
I/O Supply Voltage	$V_{DDQ}$	1.7	1.8	1.9	V	4
I/O Reference Voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2
I/O Termination Voltage (system)	$V_{TT}$	$V_{REF} - 40$	$V_{REF}$	$V_{REF} + 40$	mV	3

NOTE:

- $V_{DD}$  and  $V_{DDQ}$  must keep track of each other.  $V_{DDQ}$  cannot exceed the value of  $V_{DD}$
- $V_{REF}$  is expected to equal  $V_{DDQ}/2$  of the transmitting device and to track variations in the DC level of the same
- $V_{TT}$  is not applied directly to the device.  $V_{TT}$  is a system supply for signal termination resistors, is expected to be set equal to  $V_{REF}$  and must track variations in the DC level of  $V_{REF}$
- $V_{DDQ}$  must tracks  $V_{DD}$ ; and  $V_{DDL}$  tracks  $V_{DD}$

**Input/Output Capacitance:**

$V_{DD} = +1.8V \pm 0.1V$ ,  $V_{DDQ} = +1.8V \pm 0.1V$ ,  $V_{REF} = V_{SS}$ ,  $f = 100MHz$ ,  $0^\circ C < T_{OPR} < +55^\circ C$ ,  $V_{OUT}(DC) = V_{DDQ}/2$

Parameter	Symbol	Min	Max	Units
Input Capacitance: $CK, \overline{CK}$	CCK	1.0	2.0	pF
Delta Input Capacitance: $CK, \overline{CK}$	CDCK	-	0.25	pF
Input Capacitance: BA0, BA1, A0-A12, $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , CKE, ODT	CI	1.0	2.0	pF
Delta Input Capacitance: BA0, BA1, A0-A12, $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , CKE, ODT	CDI	-	0.25	pF
Input/Output Capacitance: DQs, DQS, DM, NF	CIO	3.0	4.0	pF
Delta Input/Output Capacitance: DQs, DQS, DM, NF	CDIO	-	0.5	pF

**IDD Specifications and Conditions (256MB - 32Mx8, 9 components):**

Symbol	Parameter	DRAM IC Manufacturer*	-5 DDR2-400	-3.75 DDR2-533	Units
IDD0	Operating Current	MT	675	720	mA
		INF	N/A	N/A	mA
		SAM	1265	1420	mA
IDD1	Operating Current	MT	765	810	mA
		INF	N/A	N/A	mA
		SAM	1330	1540	mA
IDD2P	Precharge Power-Down Current	MT	32	45	mA
		INF	N/A	N/A	mA
		SAM	495	535	mA
IDD2Q	Precharge Quiet Standby Current	MT	189	225	mA
		INF	N/A	N/A	mA
		SAM	665	715	mA
IDD2N	Precharge Standby Current	MT	225	270	mA
		INF	N/A	N/A	mA
		SAM	670	730	mA
IDD3P	Active Power-Down Standby Current MRS(12) = 0	MT	135	171	mA
		INF	N/A	N/A	mA
		SAM	720	750	mA
	Active Power-Down Standby Current MRS(12) = 1	MT	63	81	mA
		INF	N/A	N/A	mA
		SAM	365	375	mA
IDD3N	Active Standby Current	MT	288	351	mA
		INF	N/A	N/A	mA
		SAM	1065	1180	mA
IDD4W	Operating Current Burst Write	MT	1125	1440	mA
		INF	N/A	N/A	mA
		SAM	1635	2115	mA
IDD4R	Operating Current Burst Read	MT	990	1260	mA
		INF	N/A	N/A	mA
		SAM	1520	1840	mA
IDD5B	Burst Auto-Refresh Current	MT	1485	1530	mA
		INF	N/A	N/A	mA
		SAM	1900	2005	mA
IDD6	Self Refresh Current	MT	27	27	mA
		INF	N/A	N/A	mA
		SAM	485	555	mA
IDD7	Operating Current	MT	2070	2160	mA
		INF	N/A	N/A	mA
		SAM	2885	2975	mA

Note:

DRAM IC Manufacturer\* - MT = Micron, INF = Infineon, SAM=Samsung

**IDD Specifications and Conditions (512MB - 64Mx8, 9 components):**

Symbol	Parameter	DRAM IC Manufacturer*	-5 DDR2-400	-3.75 DDR2-533	Units
IDD0	Operating Current	MT	TBD	TBD	mA
		INF	745	918	mA
		SAM	1265	1420	mA
IDD1	Operating Current	MT	TBD	TBD	mA
		INF	790	1008	mA
		SAM	1330	1540	mA
IDD2P	Precharge Power-Down Current	MT	TBD	TBD	mA
		INF	286	369	mA
		SAM	495	535	mA
IDD2Q	Precharge Quiet Standby Current	MT	TBD	TBD	mA
		INF	475	603	mA
		SAM	665	715	mA
IDD2N	Precharge Standby Current	MT	TBD	TBD	mA
		INF	538	639	mA
		SAM	670	730	mA
IDD3P	Active Power-Down Standby Current MRS(12) = 0	MT	TBD	TBD	mA
		INF	367	477	mA
		SAM	720	750	mA
	Active Power-Down Standby Current MRS(12) = 1	MT	TBD	TBD	mA
		INF	295	378	mA
		SAM	365	375	mA
IDD3N	Active Standby Current	MT	TBD	TBD	mA
		INF	565	693	mA
		SAM	1065	1180	mA
IDD4W	Operating Current Burst Write	MT	TBD	TBD	mA
		INF	925	1188	mA
		SAM	1725	2340	mA
IDD4R	Operating Current Burst Read	MT	TBD	TBD	mA
		INF	880	1143	mA
		SAM	1655	2020	mA
IDD5B	Burst Auto-Refresh Current	MT	TBD	TBD	mA
		INF	1330	1503	mA
		SAM	2125	2275	mA
IDD6	Self Refresh Current	MT	TBD	TBD	mA
		INF	36	36	mA
		SAM	490	560	mA
IDD7	Operating Current	MT	TBD	TBD	mA
		INF	1420	1593	mA
		SAM	3020	3155	mA

Note:

DRAM IC Manufacturer\* - MT = Micron, INF = Infineon, SAM=Samsung

**Electrical Characteristics and AC Timings:**
 $V_{DD} = +1.8V \pm 0.1V, V_{DDQ} = +1.8V \pm 0.1V, V_{REF} = V_{SS}, f = 100MHz, 0^{\circ}C < T_{OPR} < +55^{\circ}C, V_{OUT}(DC) = V_{DDQ}/2$ 

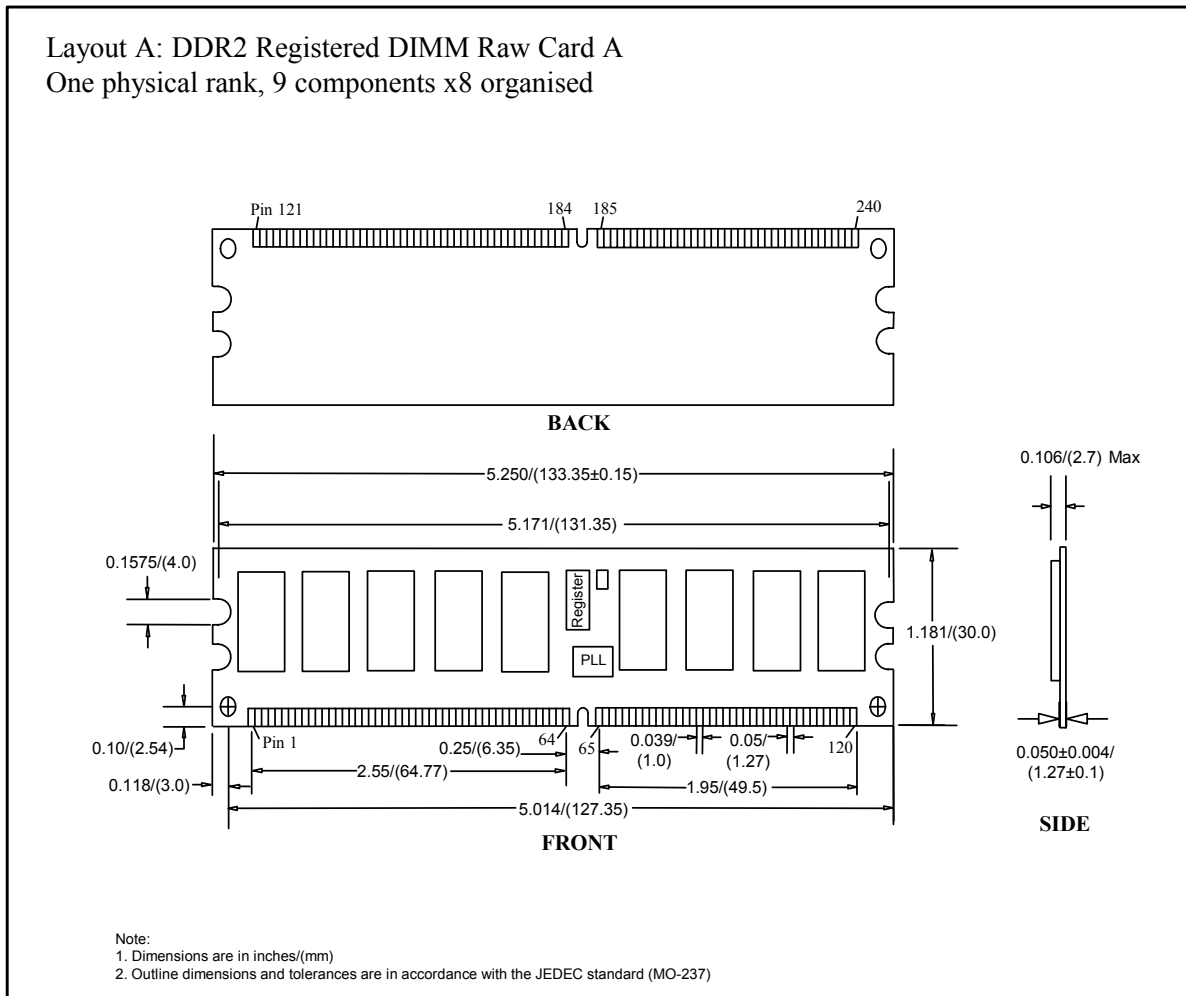
Parameter	Symbol	-5 DDR2-400		-3.75 DDR2-533		Units	
		MIN	MAX	MIN	MAX		
DQ output access time from $CK/\overline{CK}$	tAC	-600	+600	-500	+500	ps	
DQS output access time from $CK/\overline{CK}$	tDQSCK	-500	+500	-450	+450	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	MIN (tCH, tCL)	-	MIN (tCH, tCL)	-	ps	
Clock cycle time	tCK	CL=3	5,000	8,000	5,000	8,000	ps
		CL=4 & 5	5,000	8,000	3,750	8,000	ps
DQ and DM input hold time	tDH	400	-	350	-	ps	
DQ and DM input setup time	tDS	400	-	350	-	ps	
Control & Address input pulse width for each input	tIPW	0.6	-	0.6	-	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK	
Data-out high-impedance time from $CK/\overline{CK}$	tHZ	-	tACmax	-	tACmax	ps	
Data-out low-impedance time from $CK/\overline{CK}$	tLZ	tACmin	tACmax	tACmin	tACmax	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	350	-	300	ps	
Data hold skew factor	tQHS	-	450	-	400	ps	
Data output hold time from DQS	tQH	tHP- tQHS	-	tHP- tQHS	-	ps	
Write command to 1 <sup>st</sup> DQS latching transition	tDQSS	WL-0.25	WL+ 0.25	WL-0.25	WL+ 0.25	tCK	
DQS input low/high pulse width	tDQSL/H	0.35	-	0.35	-	tCK	
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK	
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK	
Mode register set command cycle time	tMRD	2	-	2	-	tCK	
Write preamble setup time	tWPRES	0	-	0	-	ps	
Write preamble	tWPRE	0.25	-	0.25	-	tCK	
Write postamble	tWPST	0.40	0.60	0.40	0.60	tCK	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Active to Precharge command	tRAS	45	70,000	45	70,000	ns	
Active to Active command period	tRC	60	-	60	-	ns	
Refresh to Refresh command interval	tRFC	105	-	105	-	ns	
Active to Read/Write delay	tRCD	15	-	15	-	ns	
Precharge command period	tRP	15	-	15	-	ns	

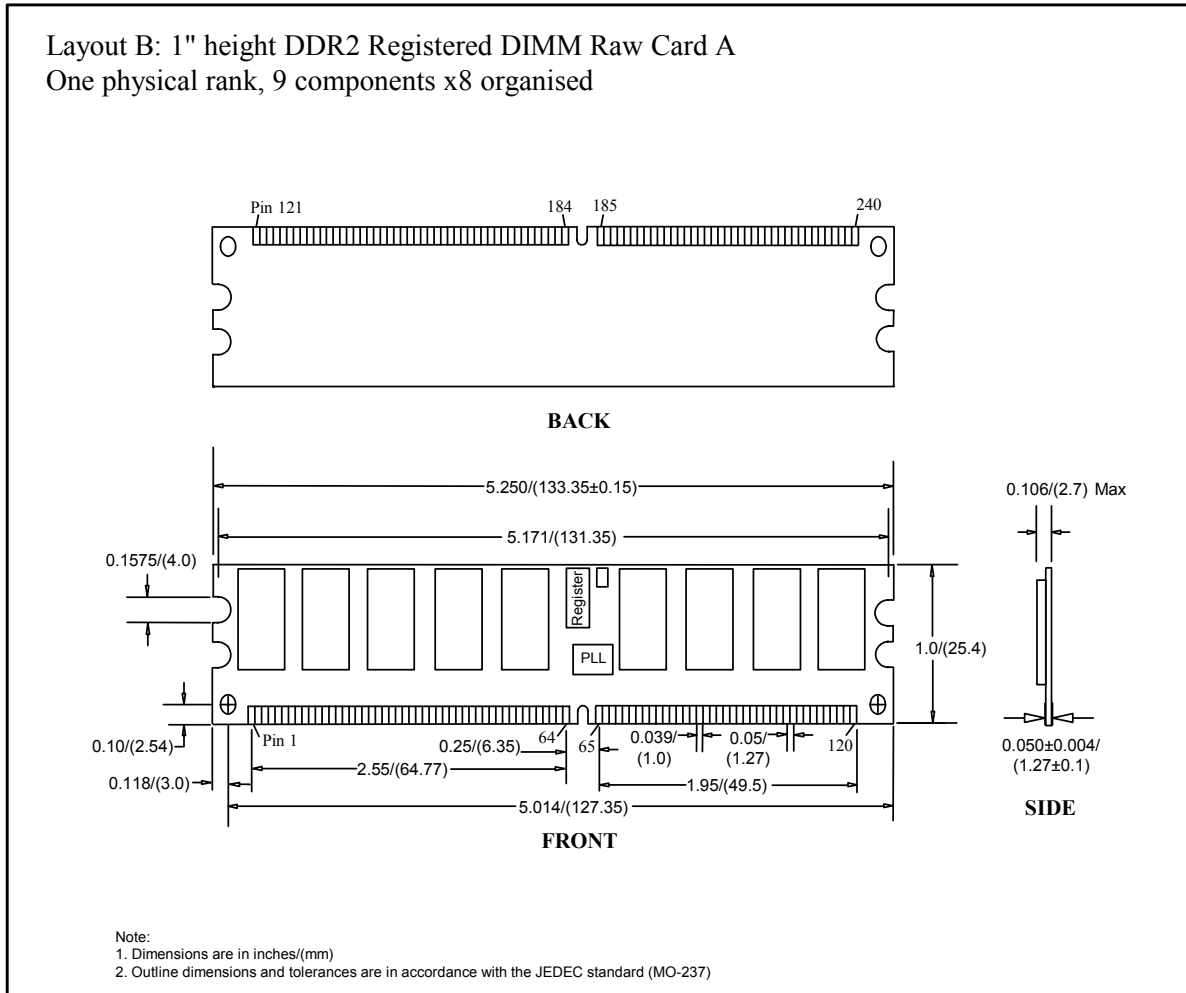
$V_{DD} = +1.8V \pm 0.1V, V_{DDQ} = +1.8V \pm 0.1V, V_{REF} = V_{SS}, f = 100MHz, 0^{\circ}C < T_{OPR} < +55^{\circ}C, V_{OUT}(DC) = V_{DDQ}/2$ 

Parameter	Symbol	-5		-3.75		Units
		DDR2-400		DDR2-533		
		MIN	MAX	MIN	MAX	
Active bank A to Active bank B command	tRRD	7.5	-	7.5	-	ns
$\overline{CAS}$ A to $\overline{CAS}$ B command period	tCCD	2		2		tCK
Write recovery time	tWR	15	-	15	-	ns
Auto Precharge write recovery + Precharge time	tDAL	WR+tRP	-	WR+tRP	-	tCK
Internal Write to Read command delay	tWTR	10	-	7.5	-	ns
Internal Read to Precharge command delay	tRTP	7.5	-	7.5	-	ns
Exit precharge power down to any non-Read command	tXP	2	-	2	-	tCK
Exit Self-Refresh to Read command	tXSRD	200	-	200	-	tCK
Exit Self-Refresh to non-Read command	tXSNR	tRFC+10	-	tRFC+10	-	ns
CKE minimum high and low pulse width	tCKE	3	-	3	-	tCK
Average periodic refresh interval	tREFI	-	7.8	-	7.8	$\mu$ s
OCD drive mode output delay	tOIT	0	12	0	12	ns
CKE low to $\overline{CK}$ , $\overline{CK}$ uncertainty	tDELAY	tIS+tCK+tIH	-	tIS+tCK+tIH	-	ns

Note: These parameters are applicable for all 3 chip manufacturers, Micron, Infineon, and Samsung.

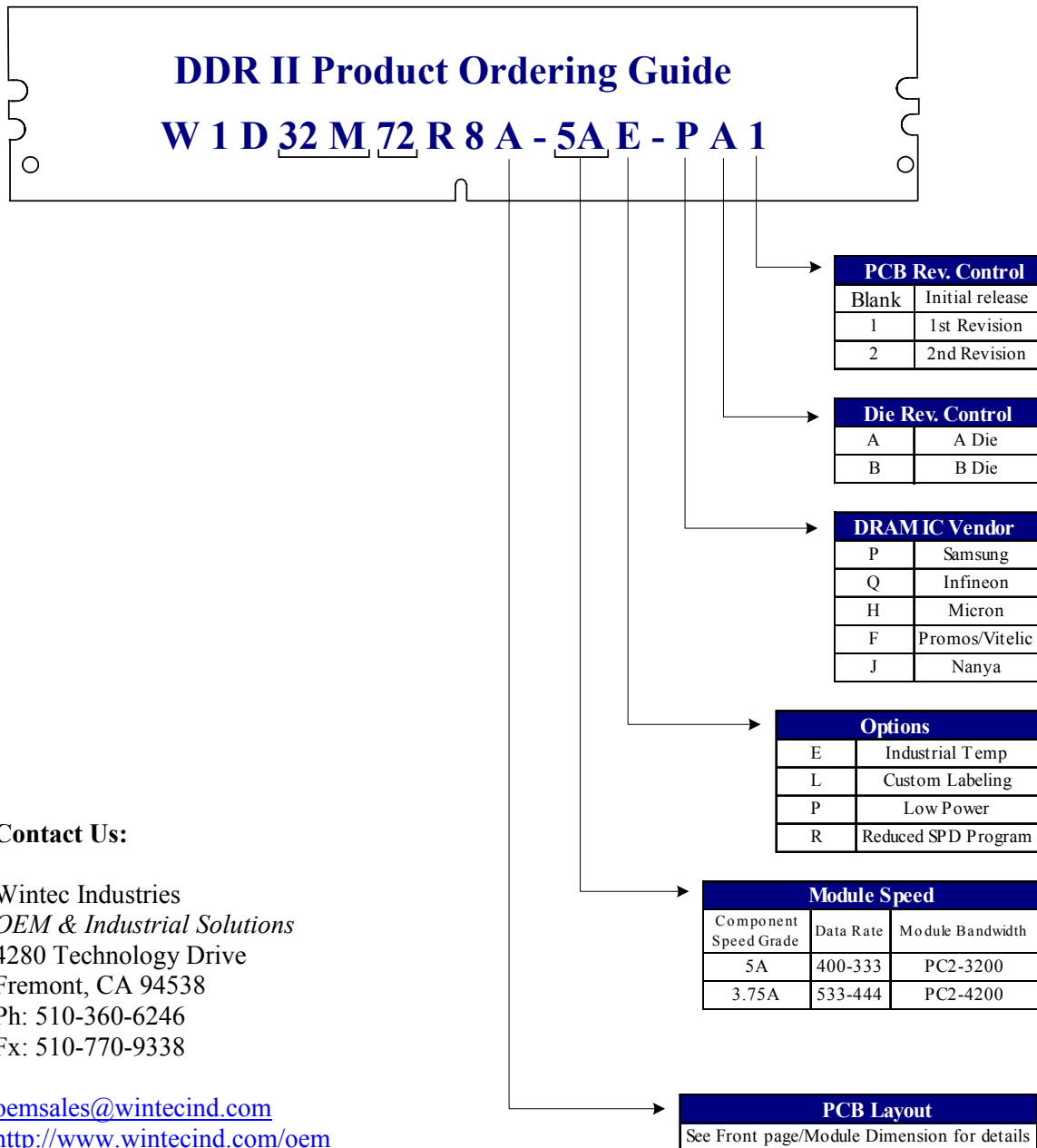


**Physical Dimensions – Layout A:**


**Physical Dimensions – Layout B:**


**Product Ordering Guide:**

- 256MB - W1D32M72R8  
 512MB - W1D64M72R8  
 1GB - W1D128M72R8  
 2GB - W1D256M72R8 (Preliminary\*)


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