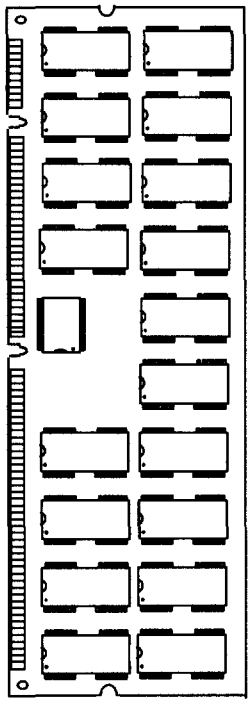
Description

The GMM773322(3)80CNTG is an 32Mx72 bits Dynamic RAM MODULE which is assembled 36 pieces of 16M x 4bit DRAMs in 32 pin TSOP-• ±package , two 16bit driver ICs in 48pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM773322(3)80CNTG is optimized for application to the systems which are required high densityand large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM773322(3)80CNTG provides common data inputs and Extended Data Outputs.

GMM773322(3)80CNTG(Double Side)



Features

* 168 pins Dual In-Line Package
  - GMM773322(3)80CNTG : Gold plating
* Extended DataOuput(EDO) Mode Capability
* Single 3.3V+/-0.3V Power Supply
* Fast Access Time & Cycle Time

(Unit: ns)

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
GMM773322(3)80CNTG-5	50	18	84	20
GMM773322(3)80CNTG-6	60	20	104	25

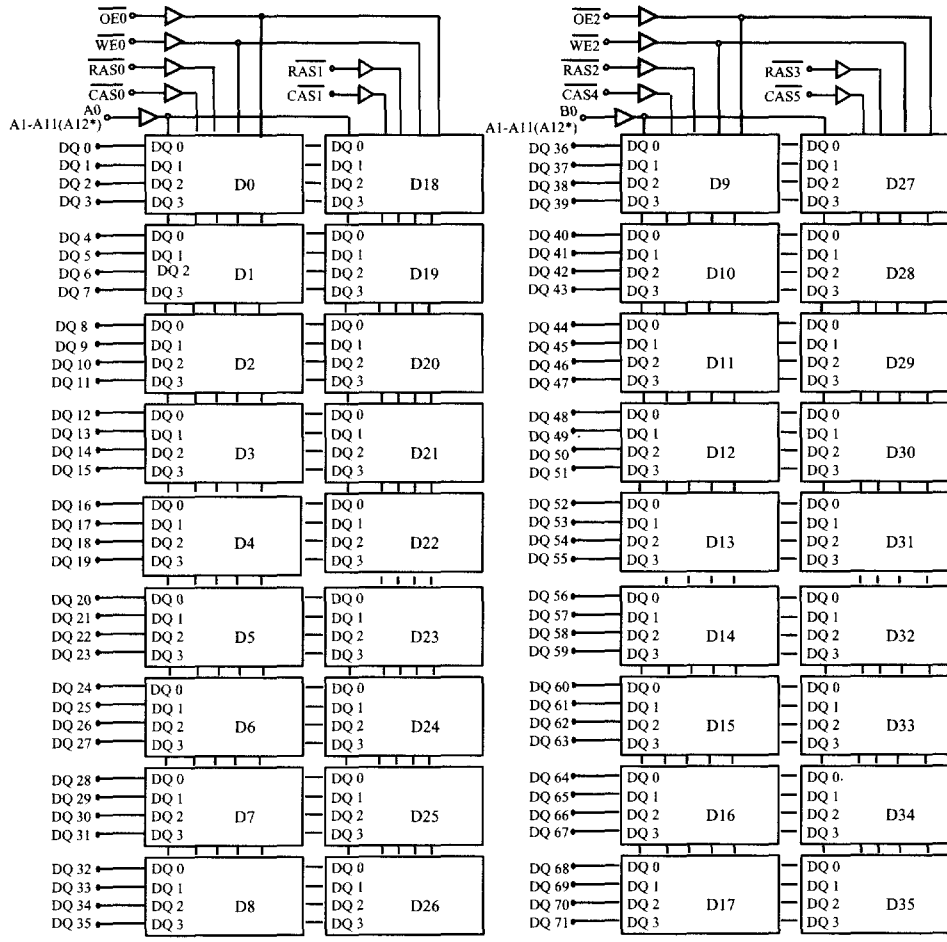
* Low Power
  Active : 9310/8662mW (MAX)
  Standby : 173mW (CMOS level : MAX)
* RAS Only Refresh, CAS before RAS Refresh, Hidden Refresh Capability
* All inputs and outputs TTL Compatible
* GMM77332280CNTG :4K Refresh / 64ms
  GMM77332380CNTG: 8K Refresh / 64ms

Pin Configuration (Top View)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	29	RSVD	57	DQ_{22}	85	V_{SS}	113	RSVD	141	DQ_{58}
2	DQ_0	30	/RAS_0	58	DQ_{23}	86	DQ_{36}	114	/RAS_1	142	DQ_{59}
3	DQ_1	31	/OE_0	59	V_{CC}	87	DQ_{37}	115	RFU	143	V_{CC}
4	DQ_2	32	V_{SS}	60	DQ_{24}	88	DQ_{38}	116	V_{SS}	144	DQ_{60}
5	DQ_3	33	A_0	61	RFU	89	DQ_{39}	117	A_1	145	RFU
6	V_{CC}	34	A_2	62	RFU	90	V_{CC}	118	A_3	146	RFU
7	DQ_4	35	A_4	63	RFU	91	DQ_{40}	119	A_5	147	RFU
8	DQ_5	36	A_6	64	RFU	92	DQ_{41}	120	A_7	148	RFU
9	DQ_6	37	A_8	65	DQ_{25}	93	DQ_{42}	121	A_9	149	DQ_{61}
10	DQ_7	38	A_{10}	66	DQ_{26}	94	DQ_{43}	122	A_{11}	150	DQ_{62}
11	DQ_8	39	A_{12}	67	DQ_{27}	95	DQ_{44}	123	A_{13}*	151	DQ_{63}
12	V_{SS}	40	V_{CC}	68	V_{SS}	96	V_{SS}	124	V_{CC}	152	V_{SS}
13	DQ_9	41	RFU	69	DQ_{28}	97	DQ_{45}	125	RFU	153	DQ_{64}
14	DQ_{10}	42	RFU	70	DQ_{29}	98	DQ_{46}	126	B_0	154	DQ_{65}
15	DQ_{11}	43	V_{SS}	71	DQ_{30}	99	DQ_{47}	127	V_{SS}	155	DQ_{66}
16	DQ_{12}	44	/OE_2	72	DQ_{31}	100	DQ_{48}	128	RFU	156	DQ_{67}
17	DQ_{13}	45	/RAS_2	73	V_{CC}	101	DQ_{49}	129	/RAS_3	157	V_{CC}
18	V_{CC}	46	/CAS_4	74	DQ_{32}	102	V_{CC}	130	/CAS_5	158	DQ_{68}
19	DQ_{14}	47	RSVD	75	DQ_{33}	103	DQ_{50}	131	RSVD	159	DQ_{69}
20	DQ_{15}	48	/WE_2	76	DQ_{34}	104	DQ_{51}	132	/PDE	160	DQ_{70}
21	DQ_{16}	49	V_{CC}	77	DQ_{35}	105	DQ_{52}	133	V_{CC}	161	DQ_{71}
22	DQ_{17}	50	RSVD	78	V_{SS}	106	DQ_{53}	134	RSVD	162	V_{SS}
23	V_{SS}	51	RSVD	79	PD_1	107	V_{SS}	135	RSVD	163	PD_2
24	RSVD	52	DQ_{18}	80	PD_3	108	RSVD	136	DQ_{54}	164	PD_4
25	RSVD	53	DQ_{19}	81	PD_5	109	RSVD	137	DQ_{55}	165	PD_6
26	V_{CC}	54	V_{SS}	82	PD_7	110	V_{CC}	138	V_{SS}	166	PD_8
27	/WE_0	55	DQ_{20}	83	ID_0	111	RFU	139	DQ_{56}	167	ID_1
28	/CAS_0	56	DQ_{21}	84	V_{CC}	112	/CAS_1	140	DQ_{57}	168	V_{CC}

Note : Pins Marked * are not used in this module.
A12(pin 39) is used for only GMM77332380CNTG(8K Ref.)

Block Diagram



* Note : A12 is used for only GMM77332380CNTG(8K Ref.)

Pin Description

Pin	Function	Pin	Function
A0,B0 A1-A11/ A0,B0, A1-A12	Address Inputs(4K Ref)/ Address Inputs(8K Ref)	$\overline{PDE}$	Presence Detect Enable
DQ0-DQ71	Data Input/Output	V_{CC}	Power (+3.3V)
$\overline{RAS0}$~ $\overline{RAS3}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$ 0,1,4,5	Column Address Strobe	NC	No Connection
$\overline{WE0}$, $\overline{WE2}$	Read/Write Enable	$\overline{OE0}$, $\overline{OE2}$	Output Enable
PD 1-8	Presence Detect	RSVD	Reserved Use
ID 0-1	ID bit	RFU	Reserved for Future Use

Presence Detect Pins (Optional)

Pin	50ns	60ns
PD1	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Driver IC & 1 for N.C
ID : 0 for Vss & 1 for N.C

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	C
T_{STG}	Storage Temperature (Plastic)	-55 ~ 125	C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-0.5 ~ 7.0	V
V_{CC}	Power Supply Voltage	-0.5 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	23	W

*Note: 1. Stress greater than above Absolute Maximum Ratings may cause permanent damage to the device.

Recommended DC Operating Conditions (T_A= 0 ~ 70C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.4	-	Vcc+0.3	V	1
V_{IL}	Input Low Voltage	0	-	0.8	V	1

DC Electrical Characteristics: (V_{CC} = 3.3V+/-0.3V, T_A = 0 ~ 70C)

Symbol	Parameter		GMM77332280CNTG		GMM77332380CNTG		Unit	Note
			Min	Max	Min	Max		
V_{OH}	Output Level Output ``H`` Level Voltage (I_{OUT} = -2mA)		2.4	Vcc	2.4	Vcc	V	
V_{OL}	Output Level Output ``L`` Level Voltage (I_{OUT} = 2mA)		0	0.4	0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} min)	50ns	-	2586	-	2226	mA	1,2
		60ns	-	2406	-	2046		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z)		-	102	-	102	mA	
I_{CC3}	$\overline{RAS}$-Only Refresh Current Average Power Supply Current $\overline{RAS}$-Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	50ns	-	2586	-	2226	mA	2
		60ns	-	2406	-	2046		
I_{CC4}	Extended Data Out Mode Current Average Power Supply Current Extended Data Out Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	50ns	-	2046	-	2046	mA	1,3
		60ns	-	1866	-	1866		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$>=V_{CC}-0.2V, D_{OUT} = High-Z)		-	48	-	48	mA	
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	50ns	-	2586	-	2586	mA	
		60ns	-	2406	-	2406		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		-	210	-	210	mA	1
$I_{I(L)}$	Input Leakage Current, Any Input (0V ≤ V_{IN} ≤ Vcc)		-5	5	-5	5	uA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ Vcc)		-5	5	-5	5	uA	

Note: 1. I_{CC} depends on output load condition when the device is selected. $I_{CC(max)}$ is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 3.3V+/-0.3V, T_A = 25C, f = 1MHz)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (A1~A12, A0, B0)	-	20	pF	1
C_{I2}	Input Capacitance ($\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$)	-	20	pF	1, 2
C_{I3}	Input Capacitance ($\overline{RAS0}$~$\overline{RAS3}$)	-	65	pF	1, 2
C_{I4}	Input Capacitance ($\overline{CAS0}$,1/$\overline{CAS4}$,5)	-	20	pF	1, 2
$C_{I/O}$	I/O Capacitance (DQ0~DQ71)	-	20	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 3.3V+/-0.3V, T_A = 0 ~ 70C, Notes 1, 2,19)

Test Conditions

Input rise and fall times : 2ns
Input level : V_{IL} /V_{IH} = 0.0/3.0V
Input timing reference levels : V_{IL} /V_{IH} = 0.8/2.0V
Output timing reference levels : V_{OL} /V_{OH} = 0.8/2.0V
Output load : 1 TTL gate+C (100pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GMM773322(3)80CNTG-5		GMM773322(3)80CNTG-6		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	84	-	104	-		
t_{RP}	$\overline{RAS}$ Precharge Time	30	-	40	-		
t_{CP}	$\overline{CAS}$ Precharge Time	8	-	10	-		
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10000	60	10000		
t_{CAS}	$\overline{CAS}$ Pulse Width	8	10000	10	10000		
t_{ASR}	Row Address Set-up Time	5	-	5	-		
t_{RAH}	Row Address Hold Time	8	-	10	-		
t_{ASC}	Column Address Set-up Time	0	-	0	-		
t_{CAH}	Column Address Hold Time	8	-	10	-		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	12	32	14	40		3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	20	12	25		4
t_{RSH}	$\overline{RAS}$ Hold Time	18	-	20	-		
t_{CSH}	$\overline{CAS}$ Hold Time	35	-	40	-		
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$Precharge Time	10	-	10	-		
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	18	-	20	-		5
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	-	0	-		6
t_{DZC}	$\overline{CAS}$ Set-up Time from D_{IN}	0	-	0	-		6
t_T	Transition Time (Rise and Fall)	2	50	2	50		7
t_{REF}	Refresh Period (4096 Cycles)	-	64	-	64	ms	

Read Cycles

Symbol	Parameter	GMM773322(3)80CNTG-5		GMM773322(3)80CNTG-6		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	50	-	60		8,9
t_{CAC}	Access Time from $\overline{CAS}$	-	18	-	20		9,10,17
t_{AA}	Access Time from Column Address	-	30	-	35		9,11,17
t_{OAC}	Access Time from $\overline{OE}$	-	18	-	20		9
t_{RCS}	Read Command Set-up Time	0	-	0	-		
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-		12
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	-	0	-		12
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-		
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	15	-	18	-		
t_{OFF}	Output Buffer Turn-off Delay Time from $\overline{CAS}$	-	18	-	20		13,21
t_{OEZ}	Output Buffer Turn-off Delay Time from $\overline{OE}$	-	18	-	20		13
t_{CDD}	$\overline{CAS}$ to D_N Delay Time	18	-	20	-		5
t_{RDD}	$\overline{RAS}$ to D_N Delay Time	13	-	15	-		
t_{WDD}	$\overline{WE}$ to D_N Delay Time	13	-	15	-		
t_{OFR}	Output Buffer Turn-off Delay Time from $\overline{RAS}$	-	13	-	15		13,21
t_{WEZ}	Output Buffer Turn-off Delay Time from $\overline{WE}$	-	13	-	15		13
t_{OH}	Output Data Hold Time	3	-	3	-		21
t_{OHR}	Output Data Hold Time from $\overline{RAS}$	3	-	3	-		21
t_{RCHR}	Read Command Hold Time from $\overline{RAS}$	50	-	60	-		
t_{OHO}	Output Data Hold Time from $\overline{OE}$	3	-	3	-		
t_{CLZ}	$\overline{CAS}$ to Output in Low - Z	2	-	2	-		

Wrtie Cycles

Symbol	Parameter	GMM773322(3)80CNTG-5		GMM773322(3)80CNTG-6		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	-	0	-		14
t_{WCH}	Write Command Hold Time	8	-	10	-		21
t_{WP}	Write Command Pulse Width	8	-	10	-		
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	18	-	20	-		
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	8	-	10	-		
t_{DS}	Data-in Set-up Time	0	-	0	-		15
t_{DH}	Data-in Hold Time	13	-	15	-		15

Read-Modify-Write Cycles

Symbol	Parameter	GMM77332(3)280CNTG-5		GMM773322(3)80CNTG-6		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	116	-	140	-		
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	72	-	84	-		14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	30	-	34	-		14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	42	-	49	-		14
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	13	-	15	-		

Refresh Cycles

Symbol	Parameter	GMM773322(3)80CNTG-5		GMM773322(3)80CNTG-6		Unit	Notes
		Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	5	-	5	-		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	8	-	10	-		
t_{WRP}	$\overline{WE}$ setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	5		5			
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	8	-	10	-		
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	-	5	-		

Extended Data Out Mode Cycles

Symbol	Parameter	GMM773322(3)80CNTG-5		GMM773322(3)80CNTG-6		Unit	Notes
		Min	Max	Min	Max		
t_{HPC}	EDO Page Mode Cycle Time	20	-	25	-		20
t_{WPE}	Write pulse width during $\overline{CAS}$ Precharge	8	-	10	-		
t_{RASP}	EDO Mode $\overline{RAS}$ Pulse Width	-	100000	-	100000		16
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	28	-	35		9,17
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	33	-	40	-		
t_{COL}	$\overline{CAS}$ Hold Time Referred $\overline{OE}$	8	-	10	-		
t_{COP}	$\overline{CAS}$ to $\overline{OE}$ set-up Time	5	-	5	-		
t_{RCHP}	Read Command Hold Time from $\overline{CAS}$ Precharge	28	-	35	-		
t_{DOH}	Output Data Hold Time from $\overline{CAS}$ Low	5	-	5	-		9,22
t_{OEP}	$\overline{OE}$ Precharge Time	8	-	10	-		

EDO Page Mode Read-Modify-Write cycle

Symbol	Parameter	GMM773322(3)80CNTG-5		GMM773322(3)80CNTG-6		Unit	Notes
		Min	Max	Min	Max		
t_{HPRWC}	EDO Page Mode Read-Modify-Write Cycle Time	57	-	68	-		
t_{CPW}	$\overline{WE}$ *delay time from* $\overline{CAS}$ *precharge*	45	-	54	-		14

Present Detect Read cycle

Symbol	Parameter	GMM773322(3)80CNTG-5		GMM773322(3)80CNTG-6		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid PD bit		10		10	ns	
t_{PDOFF}	$\overline{PDE}$ to PD bit in active	2	7	2	7		

Notes:

1. AC measurements assume t_T = 2 ns
2. AC initial pause of 200 us is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-RAS refresh)
3. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min) and V_{IL} (max).
8. Assumes that $t_{RCD} <= t_{RCD}$(max) and $t_{RAD} <= t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} >= t_{RCD}$(max) and $t_{RCD} + t_{CAC}$(max) >= $t_{RAD} + t_{AA}$(max).
11. Assumes that $t_{RAD} >= t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$(max) <= $t_{RAD} + t_{AA}$(max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF}(max), t_{OEZ}(max), t_{OFR}(max) and t_{WEZ}(max) define the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} >= t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle: if $t_{RWD} >= t_{RWD}$(min), $t_{CWD} >= t_{CWD}$(min), $t_{AWD} >= t_{AWD}$(min) and $t_{CPW} >= t_{CPW}$(min), the cycle is a read-modify-write and the data output will contain data read from the selected cell: if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. t_{DS} and t_{DH} are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in extended data out mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.

20. t_{HPC}(min) can be achieved during a series of EDO mode early write cycles or EDO mode read cycles. If both write and read operation are mixed in a EDO mode, $\overline{RAS}$ cycle { EDO mode mix cycle (1),(2) } minimum value of $\overline{CAS}$ cycle $t_{HPC}(t_{CAS} + t_{CP} + 2t_T)$ becomes greater than the specified t_{HPC}(min) value.The value of CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH}, and between t_{OFR} and t_{OFF} .
22. t_{DOH} defines the time at which the output level go cross. V_{OL} =0.8V, V_{OH}=2.0V of output timing reference level.
23. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64 us period on the condition a and b below.

    a. Enter self refresh mode within 15.6us after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.

    b. Start burst refresh or distributed refresh at equal interval to all refresh addressed within 15.6 us after exiting from self refresh mode.
24. In case of entering from $\overline{RAS}$-only-refresh, it is necessary to execute CBR refresh before and after self refresh mode according as note 23.
25. For L_version, it is available to apply each 128ms and 31.2 us instead of 64 ms and 15.6 us at note 23.
26. At t_{RASS} +/-100 us , self refresh mode is activated, and not activated at t_{RASS}10us . It is undefined within the range of 10us t_{RASS}. 100 us. for t_{RASS} +/- 10 us , it is necessary to satisfy t_{RPS} .
27. XXX: H or L (H : V_{IH}(min)<=V_{IN}<=V_{IH}(max), L: V_{IH}(min)<=V_{IN}<=V_{IH}(max))

    ///////: Invalid Dout

    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms

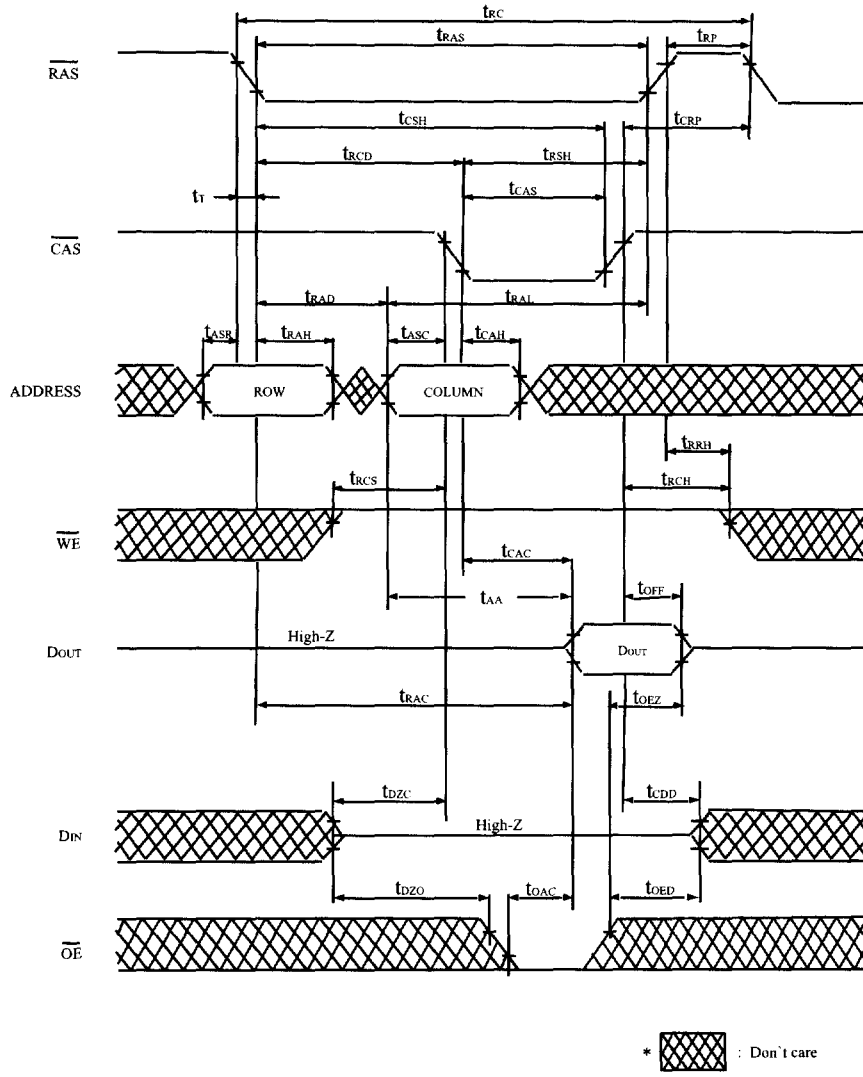


FIGURE 1. READ CYCLE

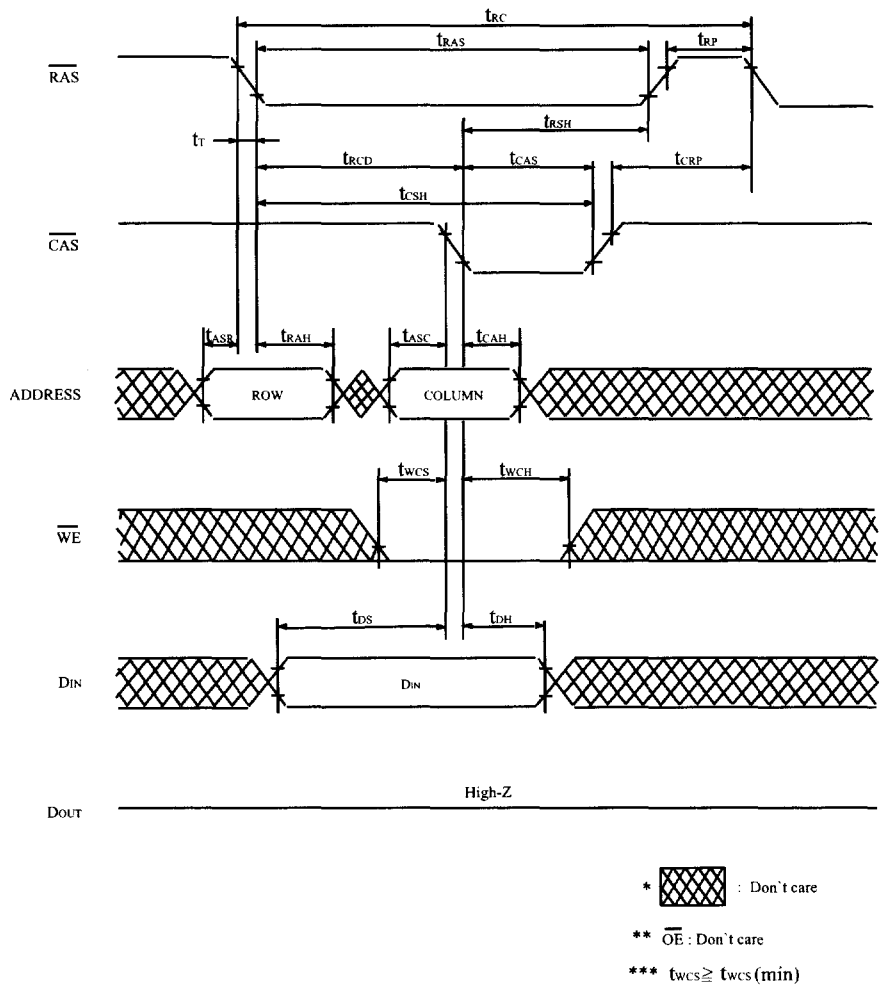


FIGURE 2. EARLY WRITE CYCLE

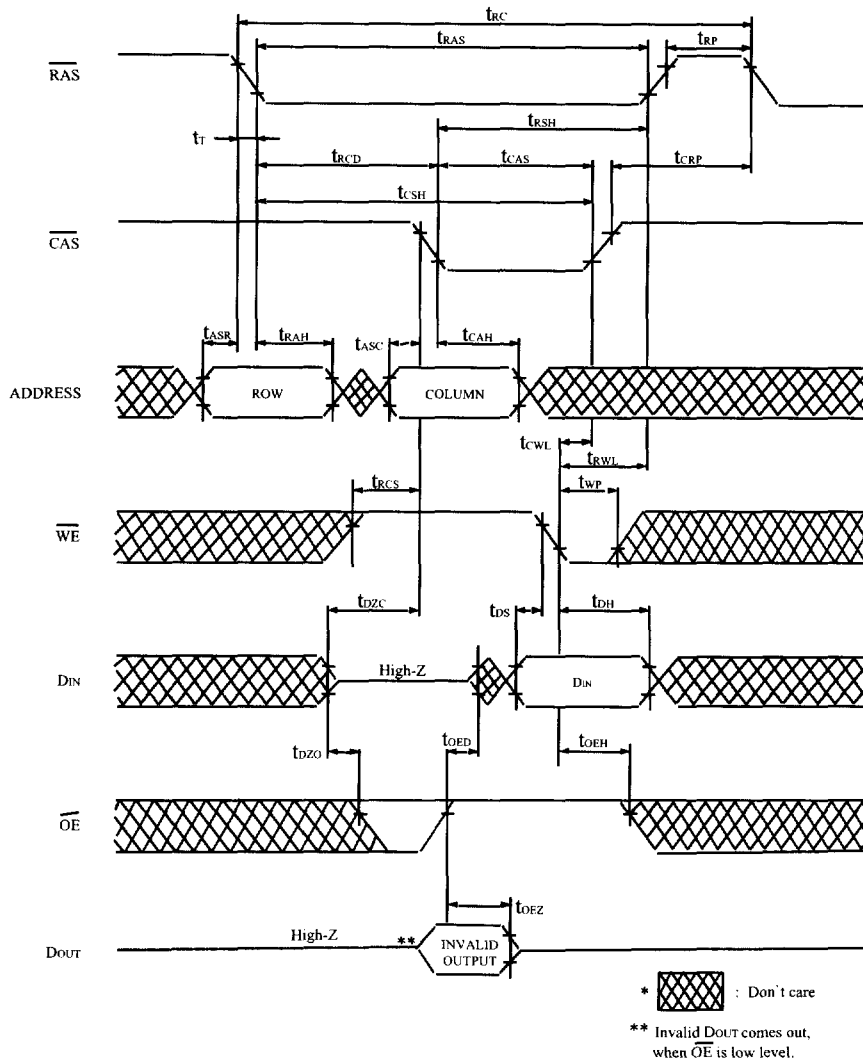


FIGURE 3. DELAYED WRITE CYCLE

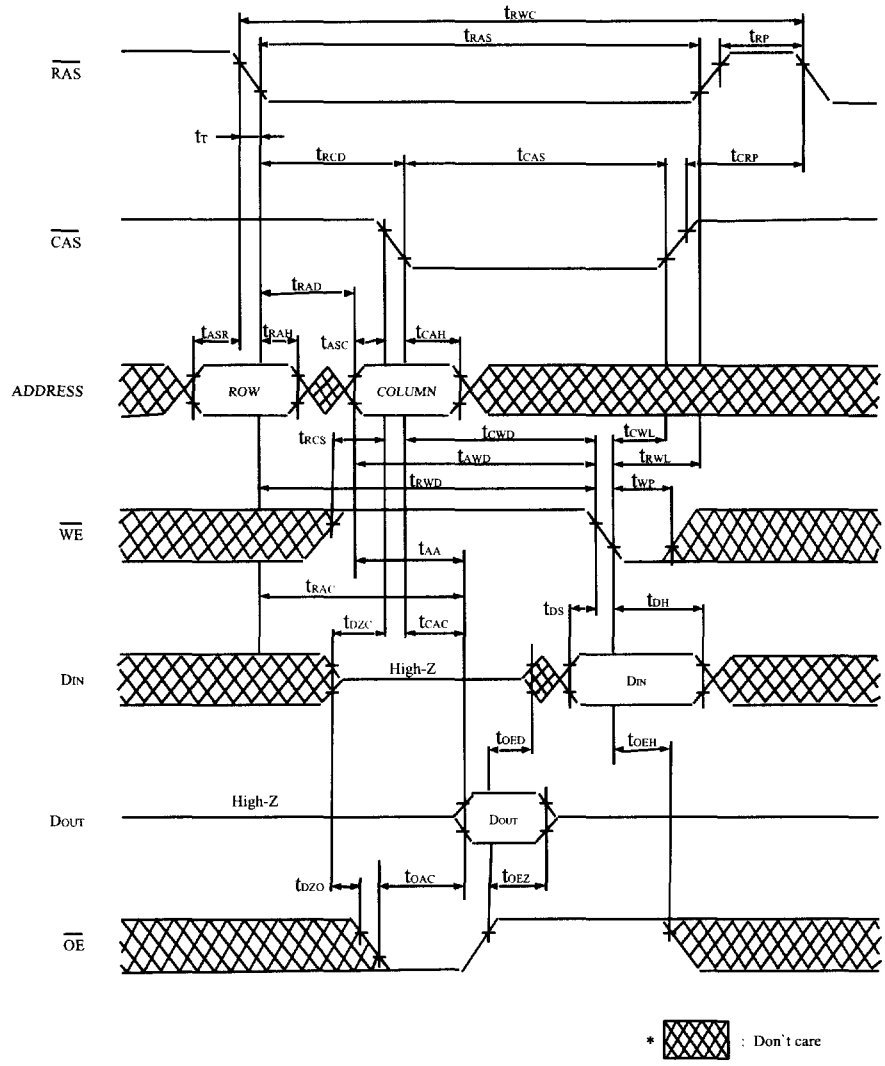


FIGURE 4. READ MODIFY WRITE CYCLE

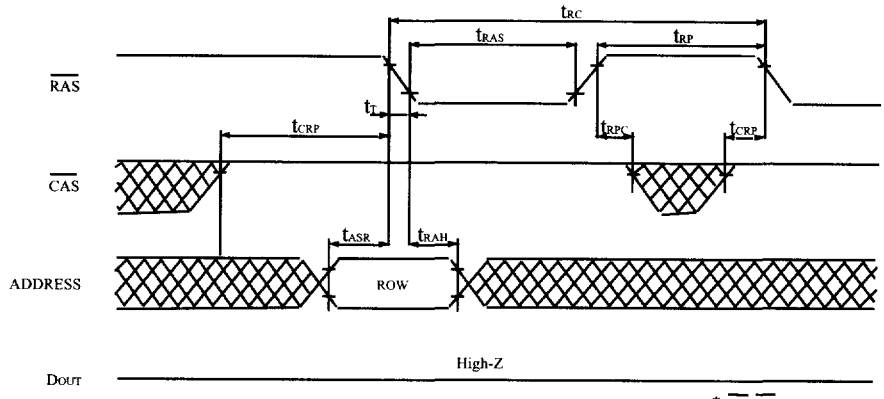


FIGURE 5. RAS ONLY REFRESH CYCLE

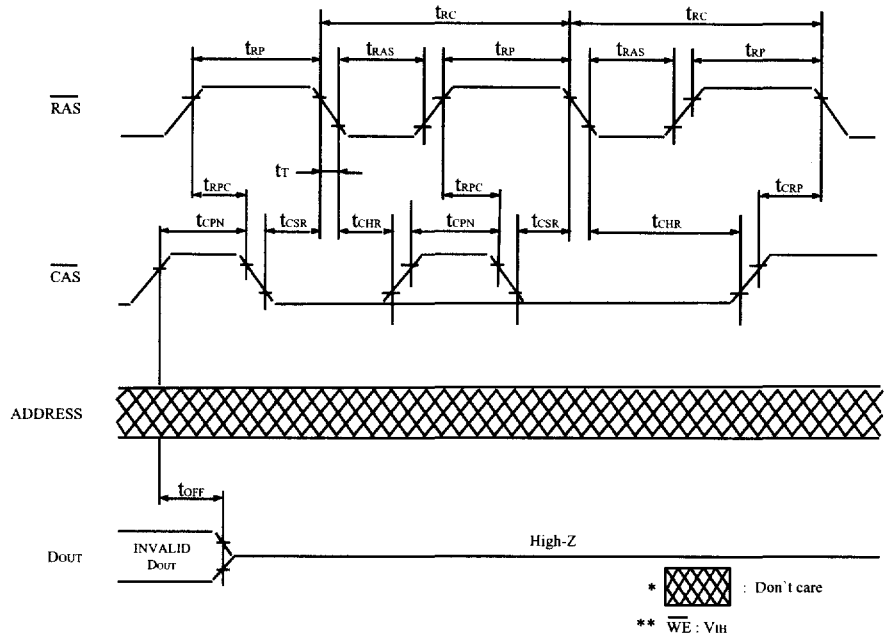


FIGURE 6. CAS BEFORE RAS REFRESH CYCLE

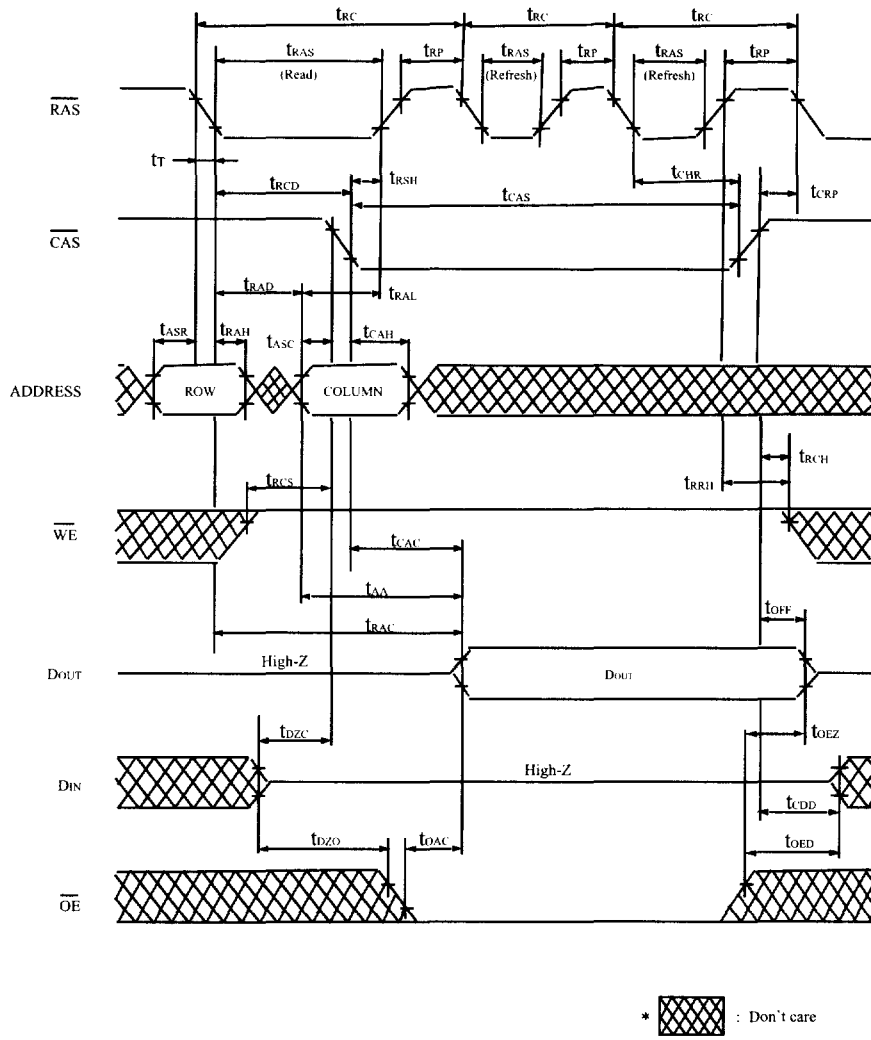


FIGURE 7. HIDDEN REFRESH CYCLE

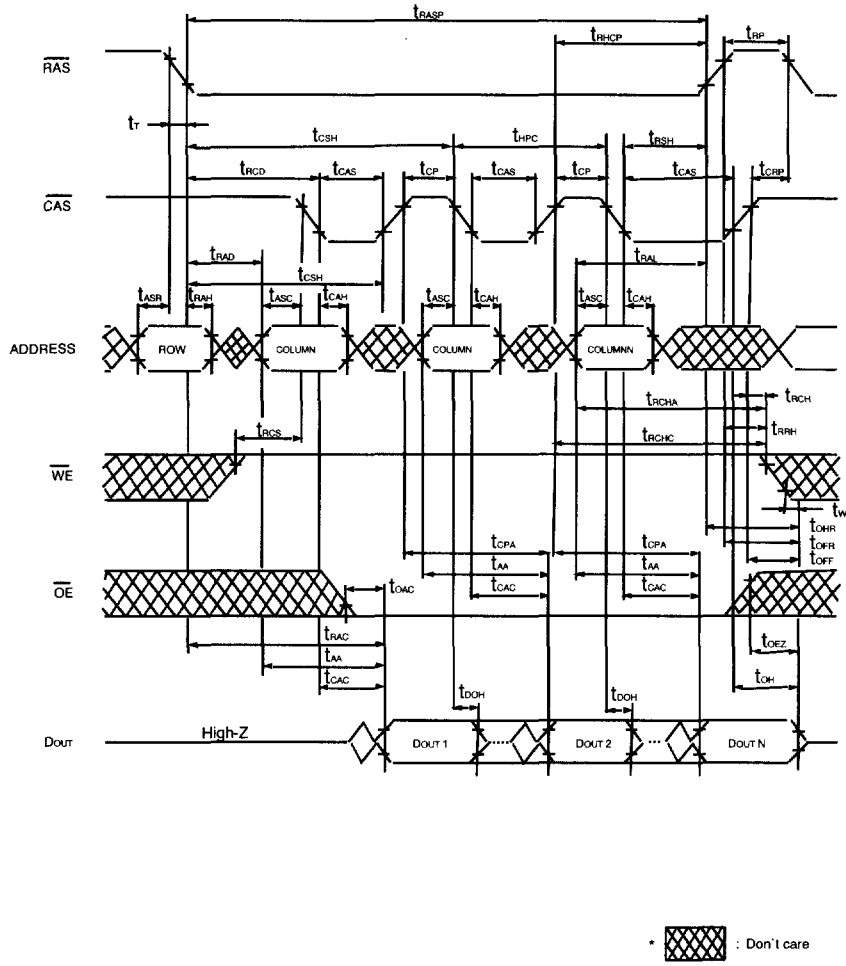


FIGURE 8. EXTENDED DATA OUT MODE READ CYCLE

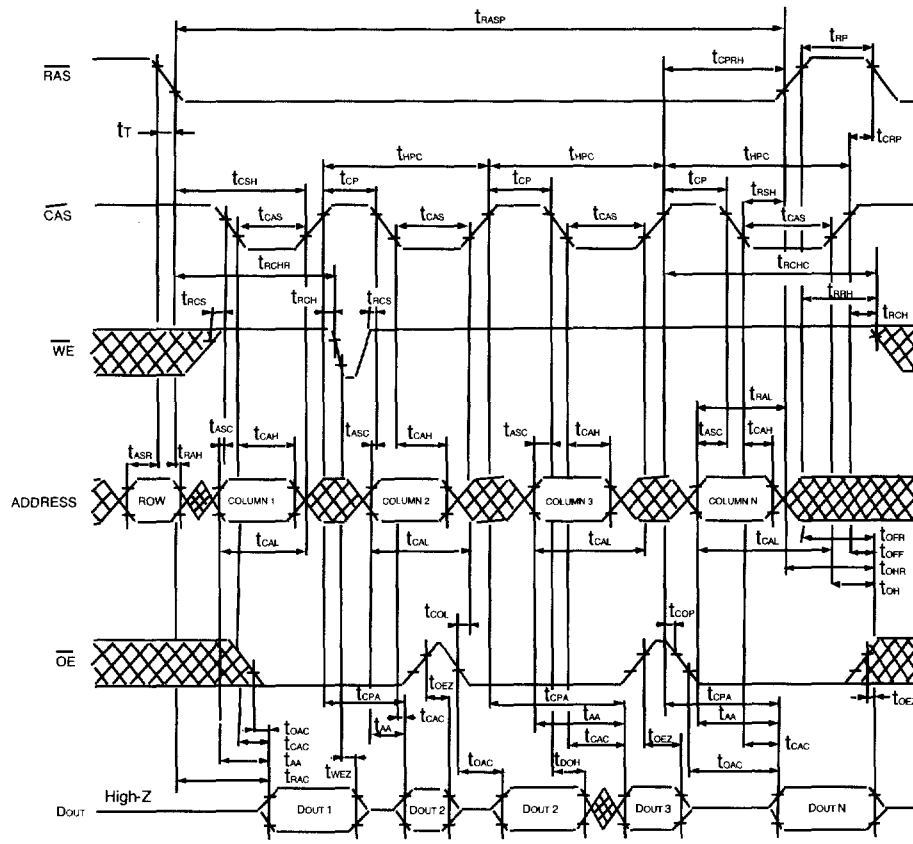


FIGURE 9. EXTENDED DATA OUT MODE READ CYCLE ($\overline{OE}$ CONTROL) *

*NOTE : EDO Hi-Z control by $\overline{OE}$ or $\overline{WE}$. $\overline{OE}$ rising edge disables data outputs. When $\overline{OE}$ goes high during $\overline{CAS}$ high, the data will not come out until next $\overline{CAS}$ access. When $\overline{WE}$ goes low during $\overline{CAS}$ high, the data will not come out until next $\overline{CAS}$ access.

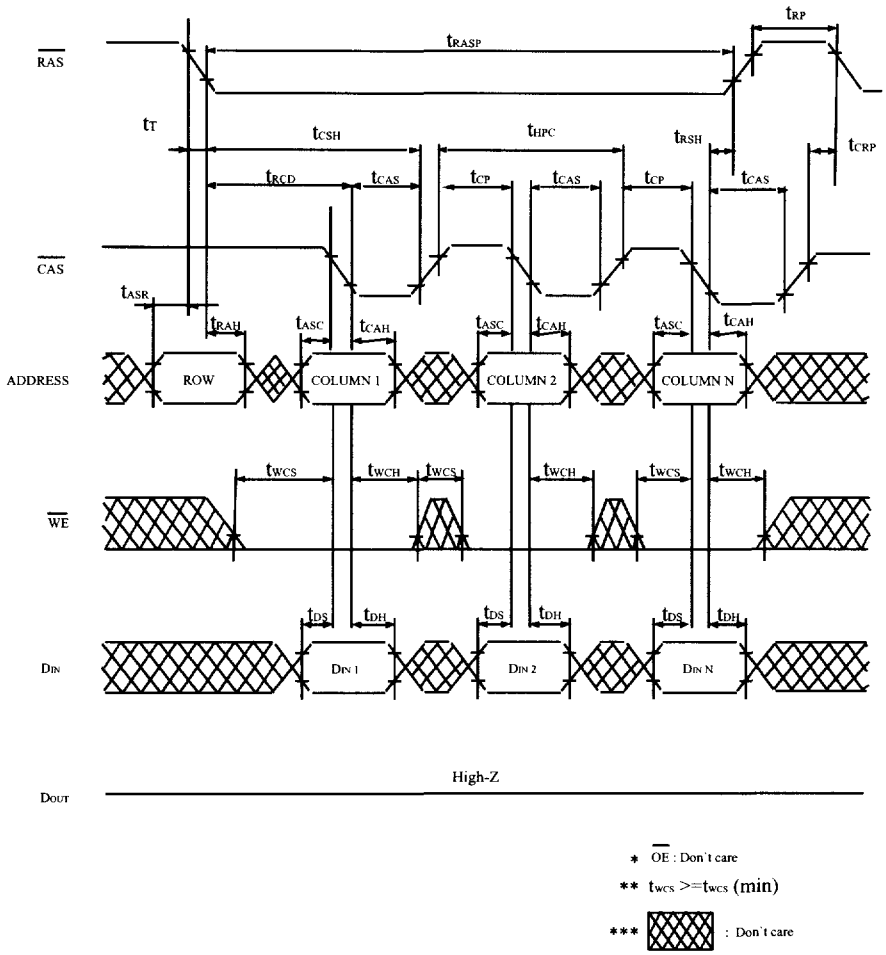


FIGURE 10. EXTENDED DATA OUT MODE EARLY WRITE CYCLE

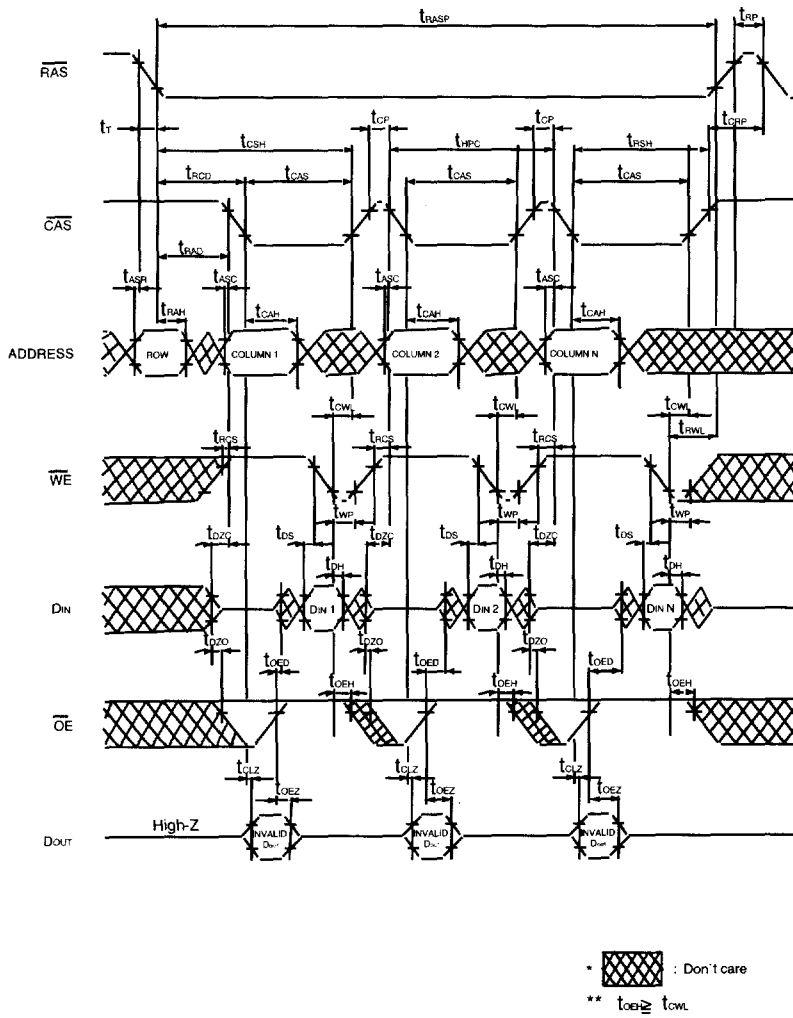


FIGURE 11. EXTENDED DATA OUT MODE DELAYED WRITE CYCLE

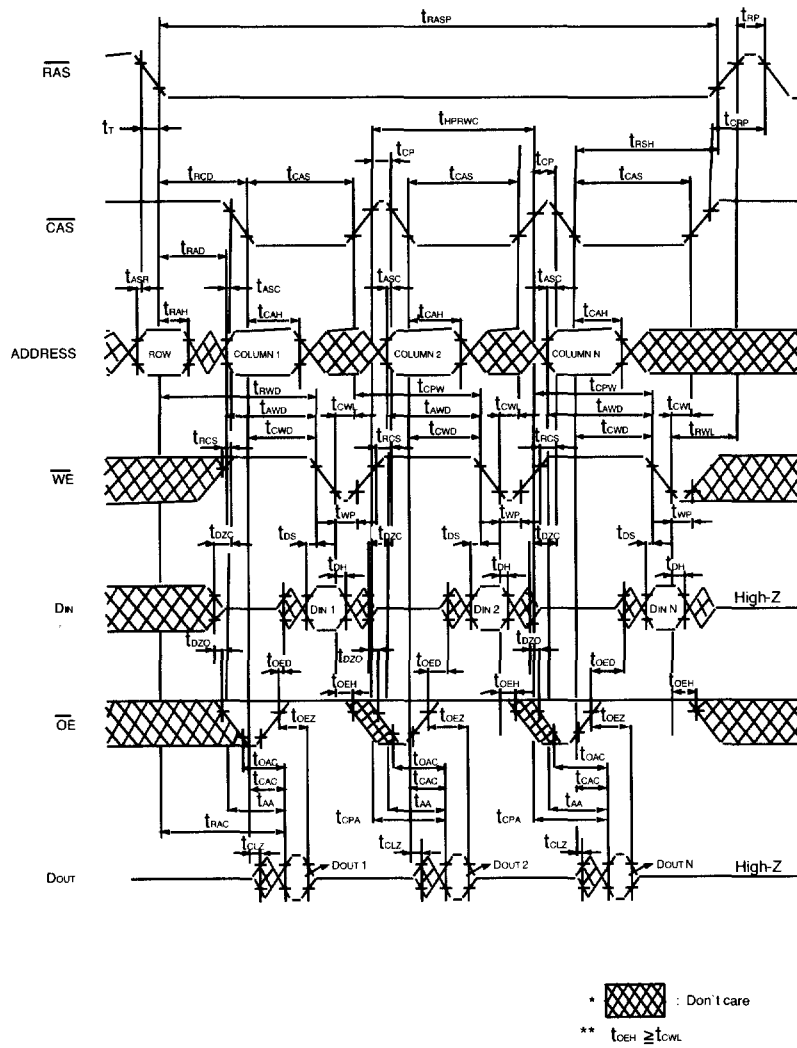


FIGURE 12. EXTENDED DATA OUT MODE READ MODIFY WRITE CYC LE

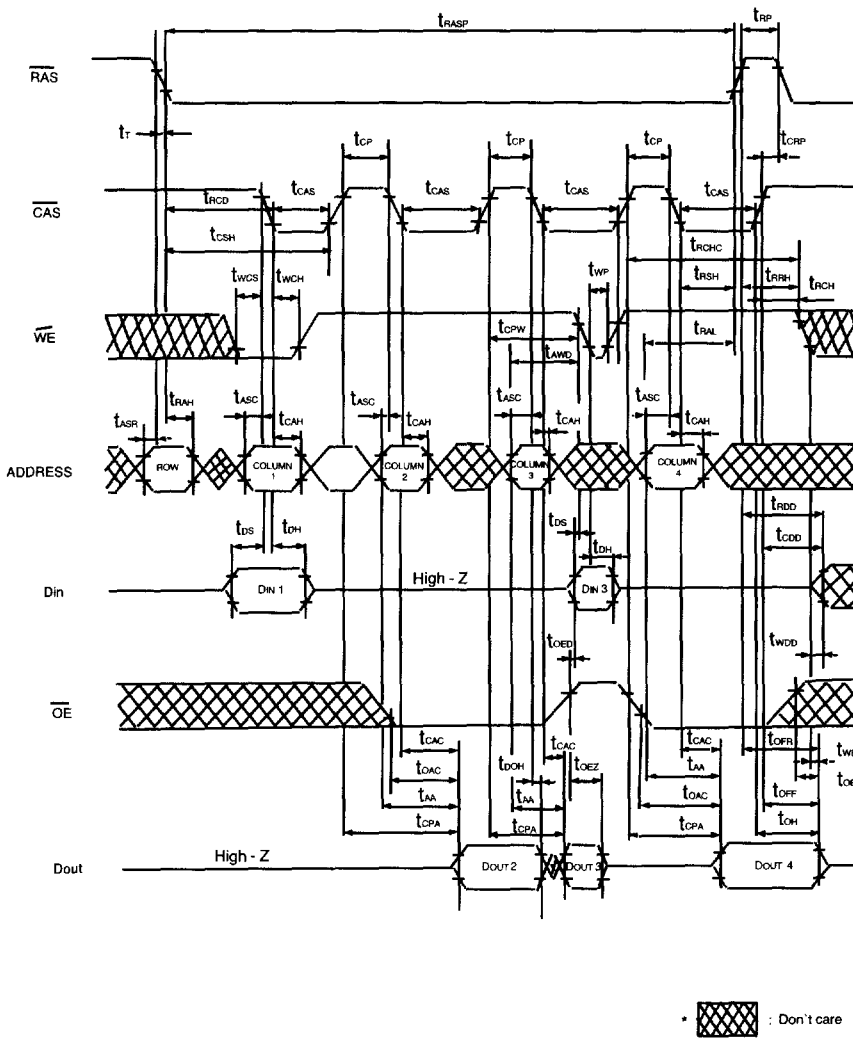


FIGURE 13. EXTENDED DATA OUT MODE MIX CYCLE (1) [23]

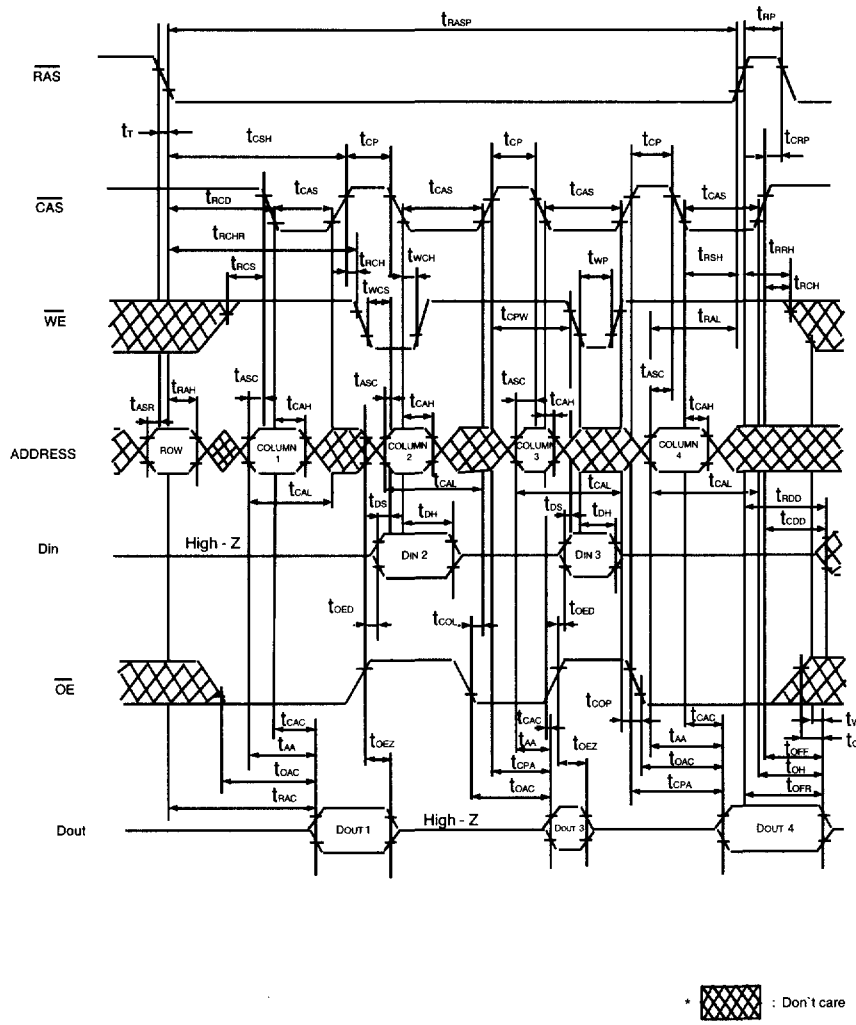


FIGURE 14. EXTENDED DATA OUT MODE MIX CYCLE (2) *23

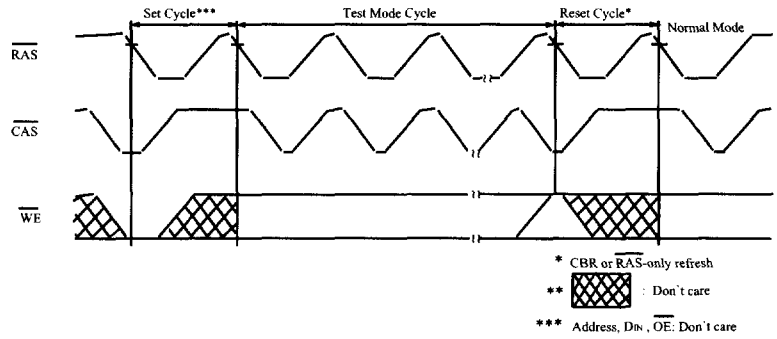


FIGURE 15. TEST MODE CYCLE

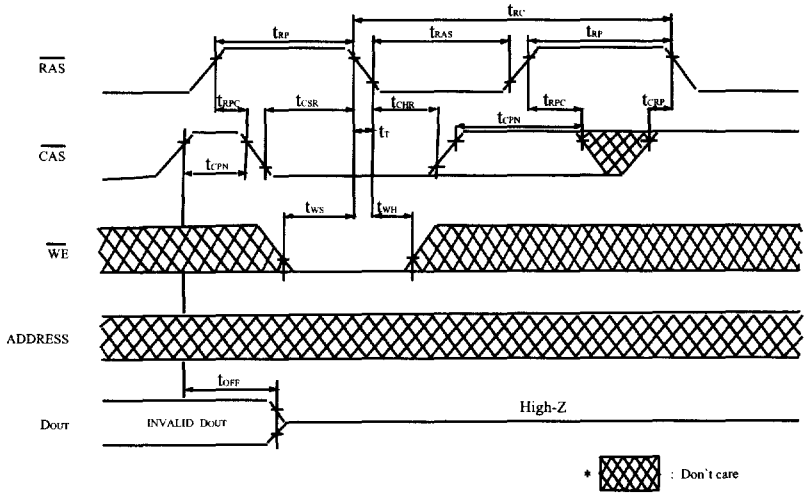


FIGURE 16. TEST MODE SET CYCLE

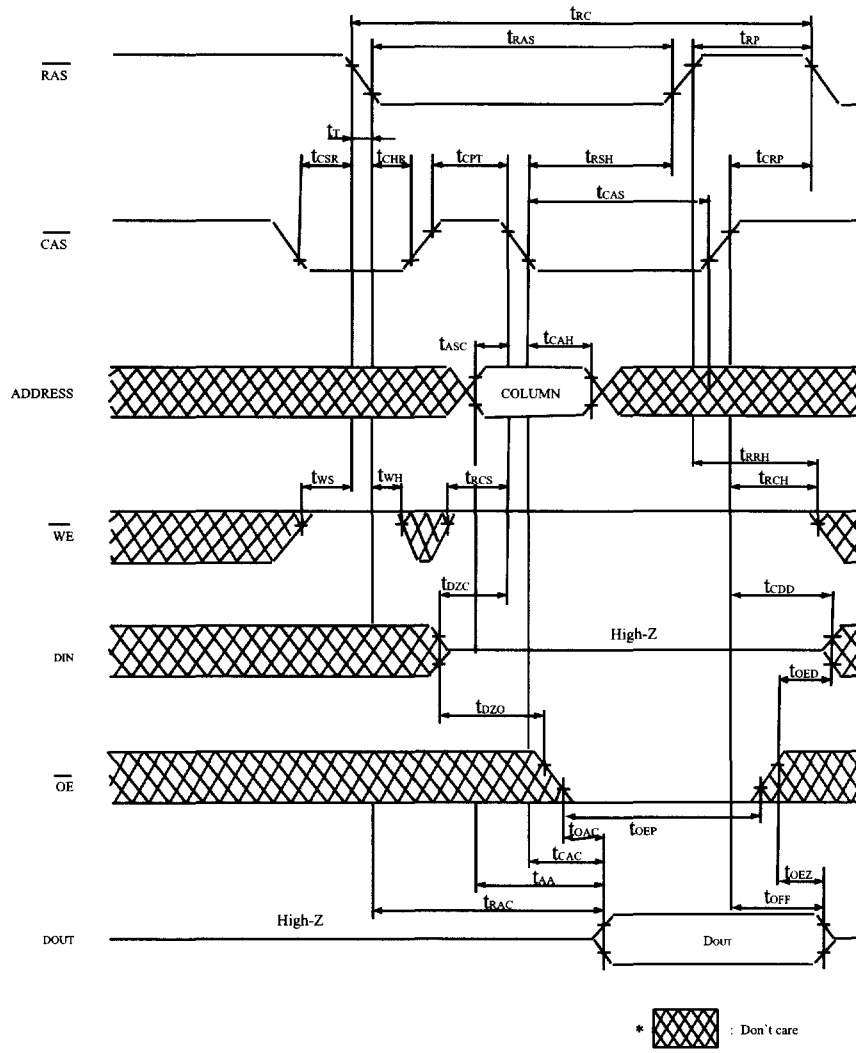


FIGURE 16. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER CHECK CYCLE (READ)

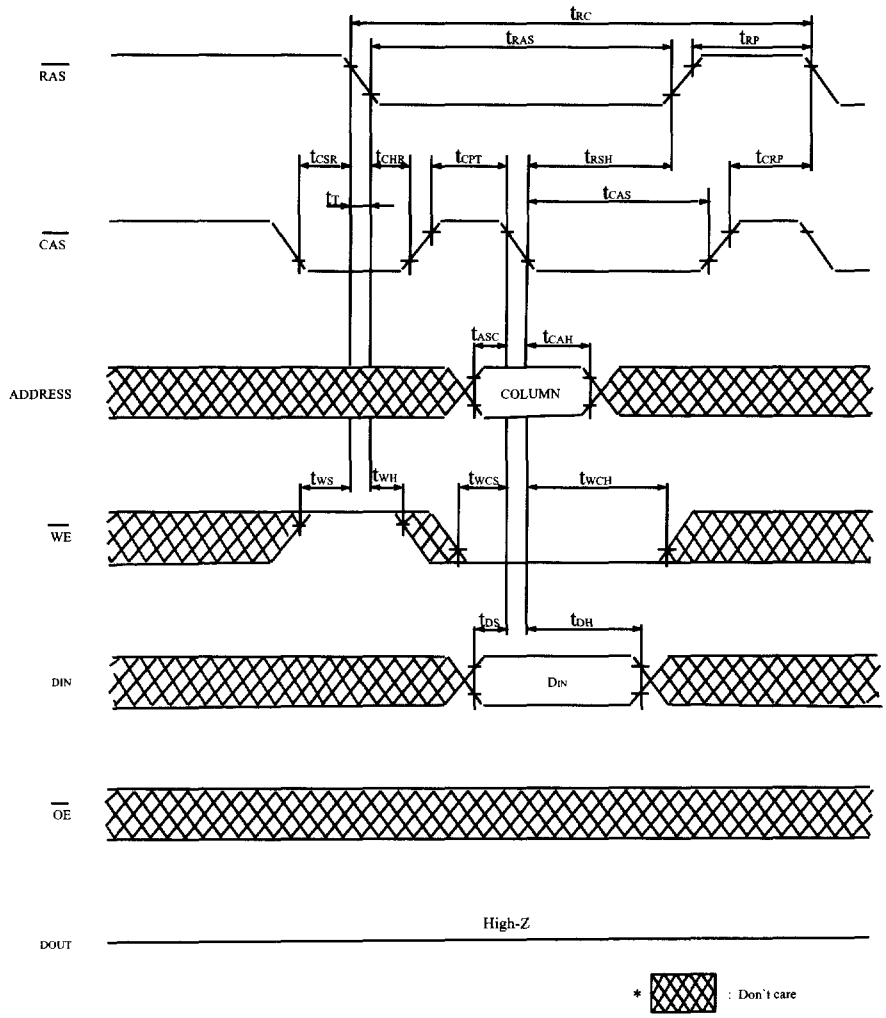
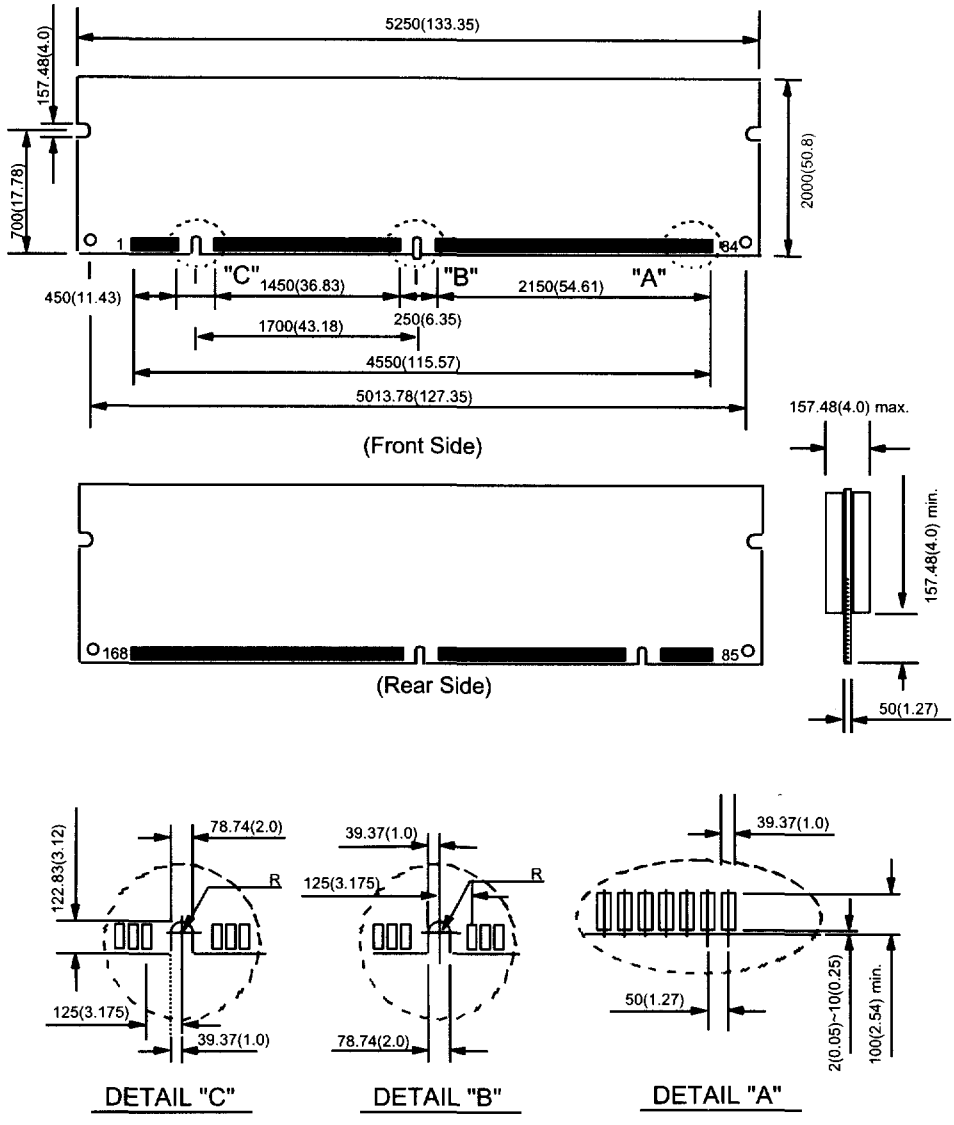


FIGURE 17. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER CHECK CYCLE (WRITE)

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions +/-5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.