

Hot-Swap SiP With Active EMI Filter

Description

The QPI-7 is the low-voltage version of the QPI-8 SiP product that includes the total hot swap function with an EMI filter for DC/DC converter applications. The EMI filter provides active conducted common-mode (CM) and differential-mode (DM) noise attenuation over the CISPR22 frequency range of 150 kHz to 30 MHz. The QPI-7 is designed for use on a 24 volt DC bus. The in-rush current limit and circuit breaker are designed to deliver over 100 W of power over the typical 24 V converter operating range of 18 to 36 V.

The QPI-7's internal fault timer allows it to operate safely in the event of a short across its output. The QPI-7 enters a retry mode where it will attempt to restart until the short condition is removed. The under and over voltage thresholds can be trimmed separately via the UVEN and OV inputs using external series resistors. The Power Good active high output provides opto-coupler drive for a converter's active low enable (See Fig. 9a) or active high by connecting the diode in series with the PWRGD output (See Figure 9b).

The QPI-7 is available in a 25 mm x 25 mm x 4.5 mm SiP (System in Package) with LGA mounting. QPI-EVAL1 kits are available with a mounted QPI-7 with screw terminals for easy insertion and testing. Check www.picorpower.com for the data sheet.

Features

- >60 dB CM attenuation at 500 kHz
- >80 dB DM attenuation at 500 kHz
- 40 Vdc (max input)
- 100 Vdc surge 100 ms
- 707 V Hi-pot hold off to Shield
- Provides safe powered backplane board insertion
- 6 A Breaker with delay, plus 12 A limiter
- 25 mm x 25 mm x 4.5 mm SiP (System-in-a-Package)
- Low profile LGA package
- -40° to +100°C PCB temperature (See Figure 5)
- Hot-Swap & filter combination saves space
- Efficiency >98%
- Connects between input supply and power converter's input hold-up capacitors
- Patents pending

Applications

- Industrial and Military COTS

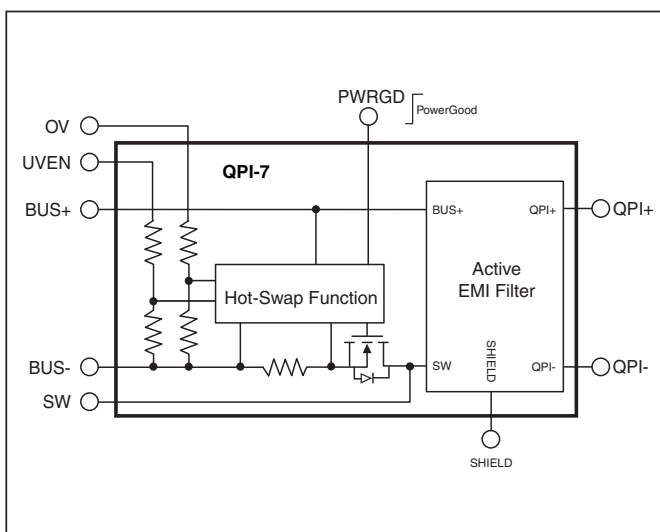


Figure 1 - Block diagram, EMI filter and Hot-Swap

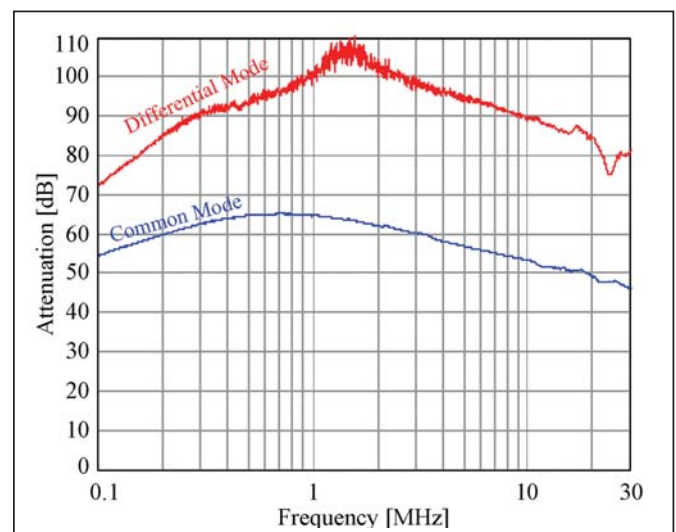


Figure 2 - QPI-7 network analyzer attenuation curves

Absolute Maximum Ratings – Exceeding these parameters may result in permanent damage to the product.

Pins	Parameter	Notes	Min	Typ	Max	Units
BUS+, SW, PWG to BUS-	Input voltage	Continuous	-0.5		40	Vdc
BUS+, SW, PWG to BUS-	Input voltage	100mSec Transient			100	Vdc
BUS+/BUS- to Shield	BUS Inputs to Shield Hi-pot				+/-707	Vdc
QPI+ to QPI-	Input to output current	Pulsed Limit @ 25°C		12		Adc
Package	Power Dissipation	VBUS=24V, 6Adc, 25°C			3.0	W
Package	Operating Temperature	PCB to QPI Interface	-40		100	°C
Package	Thermal Resistance	Free Air			50	°C/W
Package	Junction Temperature	Tb=100°C Pd=4W @15°C/W			160	°C
Package	Thermal Resistance	PCB Layout Dependent ⁽¹⁾			15	°C/W
Package	Storage Temperature		-40		125	°C
Package	Re-flow Temperature	20s exposure @ ⁽²⁾			212	°C
All Pins	ESD	HBM			+/-2	kV

Note 1: Refer to Figure 15 and QPI application note QPI-AN1 for critical PCB layout guidelines to achieve this thermal resistance when re-flowed onto the PCB.

Note 2: RoHS compliant product maximum peak temperature is 245°C for 20 seconds.

Electrical Characteristics – (Parameter limits apply over the operating PCB temperature range unless otherwise noted)

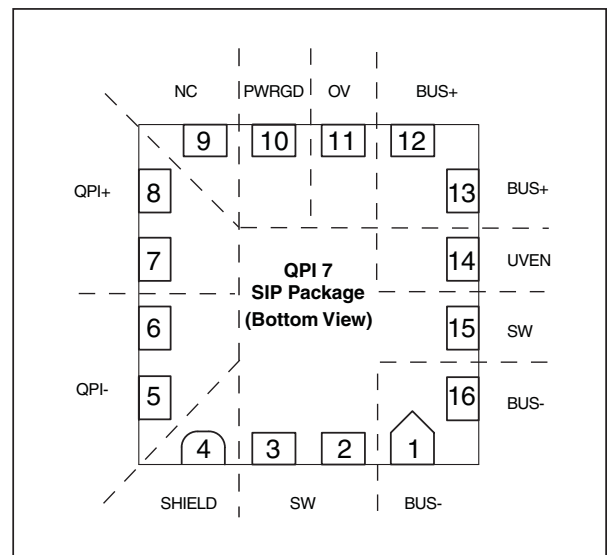
Symbol	Parameter	Notes	Min	Typ	Max	Units
Vb+b-	BUS+ to BUS- Input Range	Measured at 5 A ⁽³⁾	UV		40	Vdc
V+oi	BUS+ to QPI+ Voltage Drop	Measured at 5 A ⁽³⁾		100		mVdc
V-oi	BUS- to QPI- Voltage Drop	Measured at 5 A ⁽³⁾		250		mVdc
CMIL	Common Mode Insertion Loss	VBUS=24 V Frequency=500 kHz		63		dB
DMIL	Differential Mode Insertion Loss	VBUS=24 V Frequency=500 kHz		80		dB
I BUS+ to BUS-	Input Bias Current at 40 volts	Input current from BUS+ to BUS-		15		mA
IPG QPI+ to QPI-	Load Current Prior to PWRGD	Critical Maximum DC Load			25	mA
UV	Under Voltage Threshold - Rising	Controller Disabled to Enabled		18		V
UVHYS	Under Voltage Hysteresis - Falling	Controller Enabled to Disabled		UV – 2V		V
OV	Over Voltage Threshold - Rising	Controller Enabled to Disabled		38		V
OVHYS	Over Voltage Hysteresis - Falling	Controller Disabled to Enabled		OV - 2V		V
PWGSAT	Power Good Low Voltage	IPWG = 1 mA	0.2		0.6	mV
PWGLK	Power Good High Leakage	VPWG=40 V			1	uA

Note 3: Refer to Figure 5 for current derating curve.

Pin Descriptions

Pin Number	Name	Description
1, 16	BUS-	Negative bus potential
2, 3, 15	SW	Negative rail controlled by hot insertion function.
4	SHIELD	Shield connects to the converter shield and Y-capacitor common point via RY. See Figures 9a and 9b.
5, 6	QPI-	Negative input to the converter
7, 8	QPI+	Positive input to the converter
10	PWRGD	Open collector output that asserts low when power is NOT good.
12, 13	BUS+	Positive bus potential
14	UVEN	High side of UV resistor divider
11	OV	High side of OV resistor divider
9	Not used	No connection

SiP Package Outline (bottom view)



Applications – EMI

The QPI-7 is an active EMI filter providing conducted common-mode and differential-mode attenuation from 150 kHz to 30 MHz. Designed for the industrial and military bus range, the QPI supports the filtering of system boards to the EN 55022 class B limit.

The QPI-7 minimizes the empirical design work of passive approaches and the uncertainty that a solution will actually bring the system into compliance.

The plots in Figures 3 and 4 were taken using the standard 50_/50uH LISN and measurement conditions with the peak detection mode of the spectrum analyzer for a conducted EMI test. The converter is a VICOR V24B12C200BN, 24V

to12V dc-dc converter with a 100W load. The results show the total noise spectrum compared to the CISPR22 EN 55022 Class B Quasi-peak detection limit.

The plot in figure 4 shows the effect of inserting a QPI-7 filter between the DC bus and the converter's inputs with a 100W load on the converter's output. The resulting plot shows the QPI-7 is effective in reducing the measured pre-filtered total noise spectrum to well below the EN 55022 Quasi-peak detection limit. Using the Quasi-peak detection measurement mode would result in lower amplitudes by the error factor this method introduces.

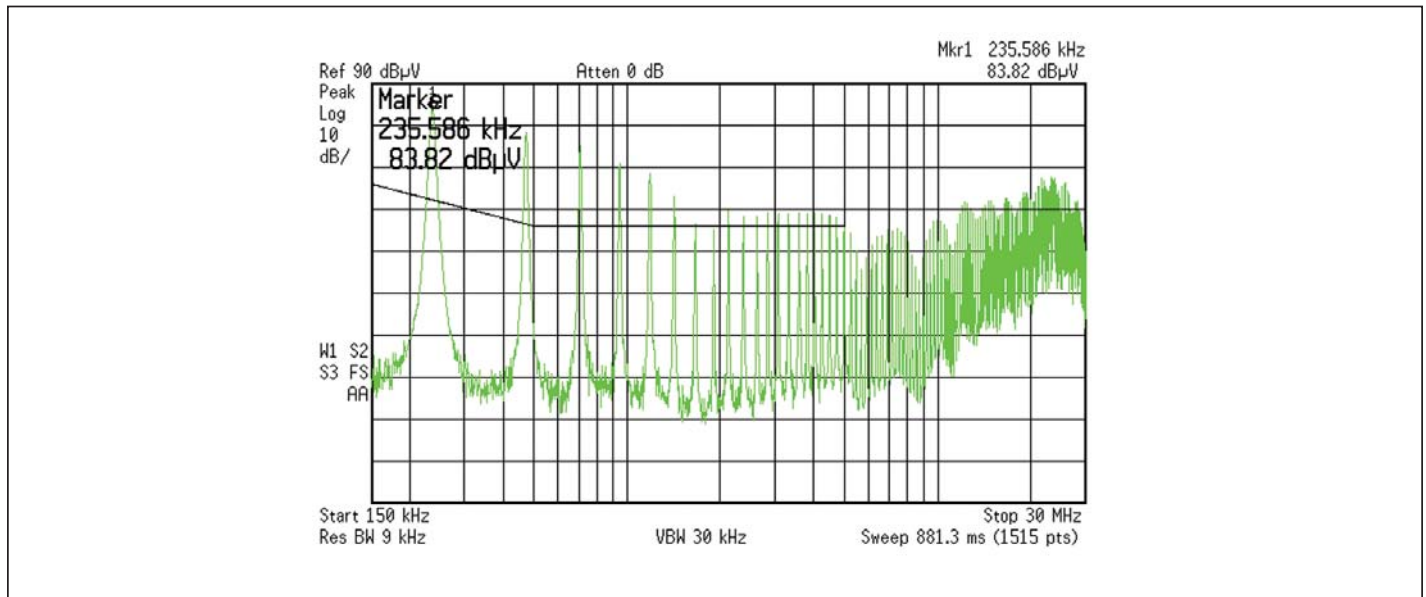


Figure 3 – Conducted EMI profile of a DC-DC converter.

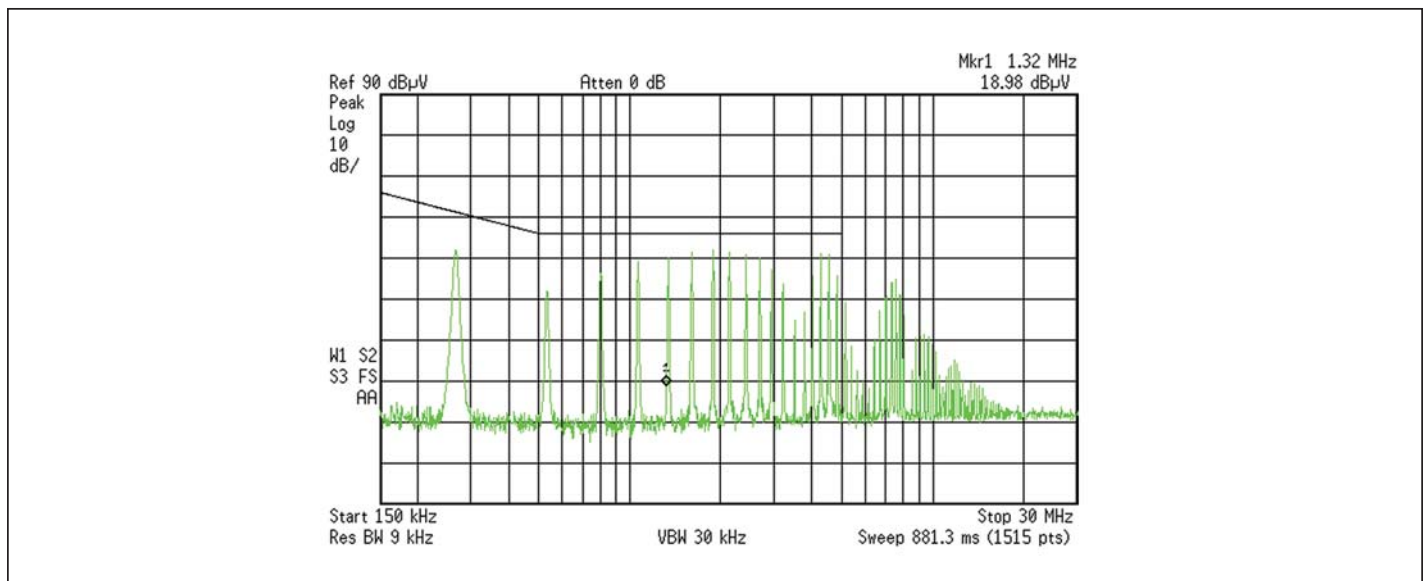


Figure 4 – Conducted EMI profile of a DC-DC converter with QPI-7.

Applications – Hot-Swap

The QPI-7's high-temperature 6 amp rating provides filtering for up to 144 watts of power from a 24 V bus with a 70°C PCB temperature. The 1.0" x1.0" x 0.2" surface mount LGA package provides ease of manufacturing by eliminating through-hole assembly. The current de-rating curve shown in figure 5 should be used when the PCB temperature that the QPI-7 is mounted to exceeds 70°C.

The QPI-7 is designed to have an under-voltage range of 16 V to 18 V set point when the UVEN pin is tied directly to the BUS+ pin. The QPI-7 becomes enabled when the input voltage exceeds 18 V and continues to work down to 16V before being disabled.

The QPI-7 over-voltage range is designed to be 36V to 38V when the OV pin is tied directly to the BUS+ pin. The QPI-7 remains functioning until the input voltage surpasses 38 V, where the QPI-7 will shutdown until the input voltage falls below 36 V.

External resistors can be added to trim the UV and OV trip points higher (See Figures 9a and 9b). The graph in Figure 6 shows the trimming effect for a range of external series resistors.

It is critical to keep the load current on the converter's input capacitor to less than 25mA during the initial power-up phase. This limit is set by the current limit level and the duty cycle of the circuit breaker timer. Once Powergood has been asserted the full load can be enabled.

An external capacitor CE, shown in Figures 9a and 9b, will provide the required hold-up filtering during a zero-volt BUS transient event. This filtering will enable the Powergood state of the QPI-7 to remain unchanged during this transient, provided there is enough hold-up capacitance and input energy to maintain the power converter's operation.

If the CE capacitor is used, a minimum value of 1K should be used for RUVEN to prevent damaging the enable diodes.

To prevent the QPI-7 from going into a fault mode and de-asserting the PWRGD signal after the transient, the converter's input capacitors must be sized so that they can be completely restored in the time of one 12A current pulse, about 750 μs, and still maintain the required input current of the converter. If greater bulk capacitance is required for higher loads, then the circuit in Figure 9c could be used to slowly charge the capacitors. To reduce bulk capacitance and take advantage of the V² energy relationship, a boost circuit with a switch-over function can be used to charge fewer bulk storage capacitors to a higher voltage.

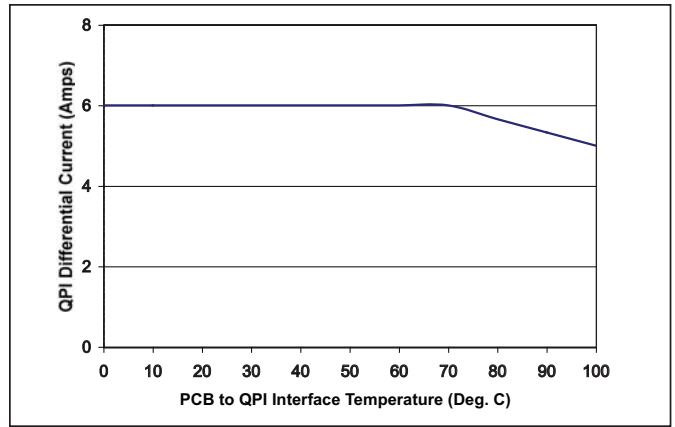


Figure 5 – QPI-7 current derating curve over temperature.

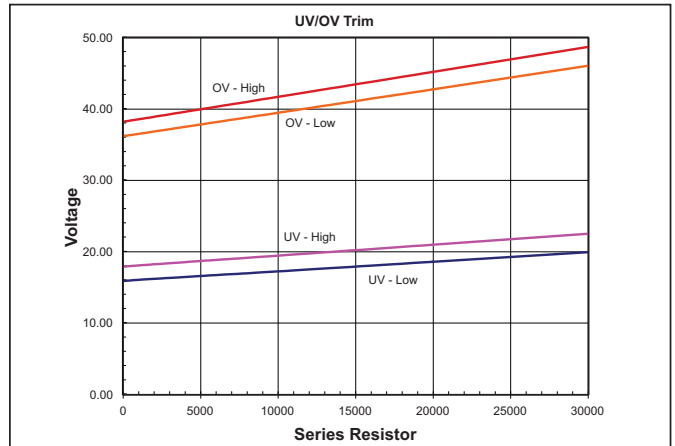


Figure 6 – Trimming UV/OV with external series resistor.

$$UVEN_{LO} = \frac{2.5 V(RUVEN + 118,700)}{18,700}$$

$$UVEN_{HI} = 2.5 V + (RUVEN + 100,000)(154 \mu A)$$

$$OV_{LO} = 2.5 V + (ROV + 102,000)(350 \mu A)$$

$$OV_{HI} = \frac{2.5 V(ROV + 109,150)}{7,150}$$

Figure 7 – UVEN and OV resistor equations.

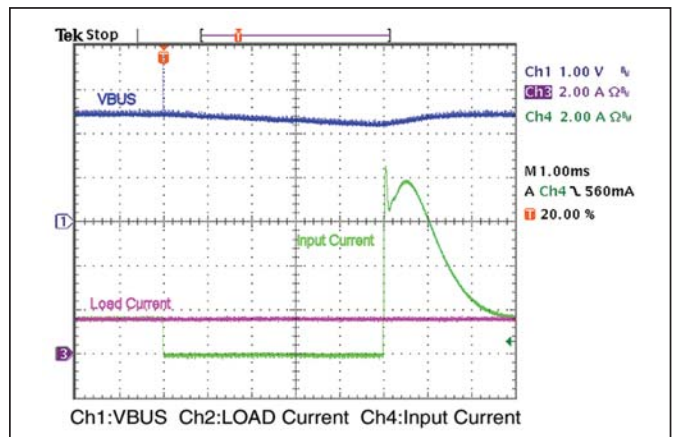


Figure 8 – 5ms BUS transient, 40W load

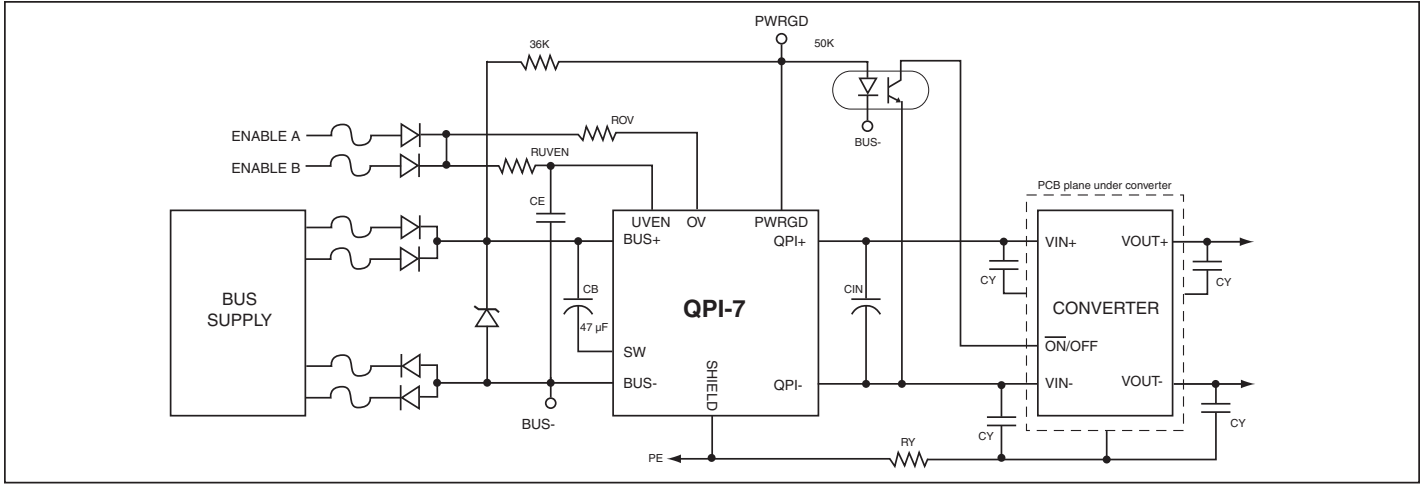


Figure 9a – Typical ATCA System with QPI-7 and Low Enable Converter
 (Refer to Figure 15 and QPI-AN1 application note for critical PCB layout guidelines)

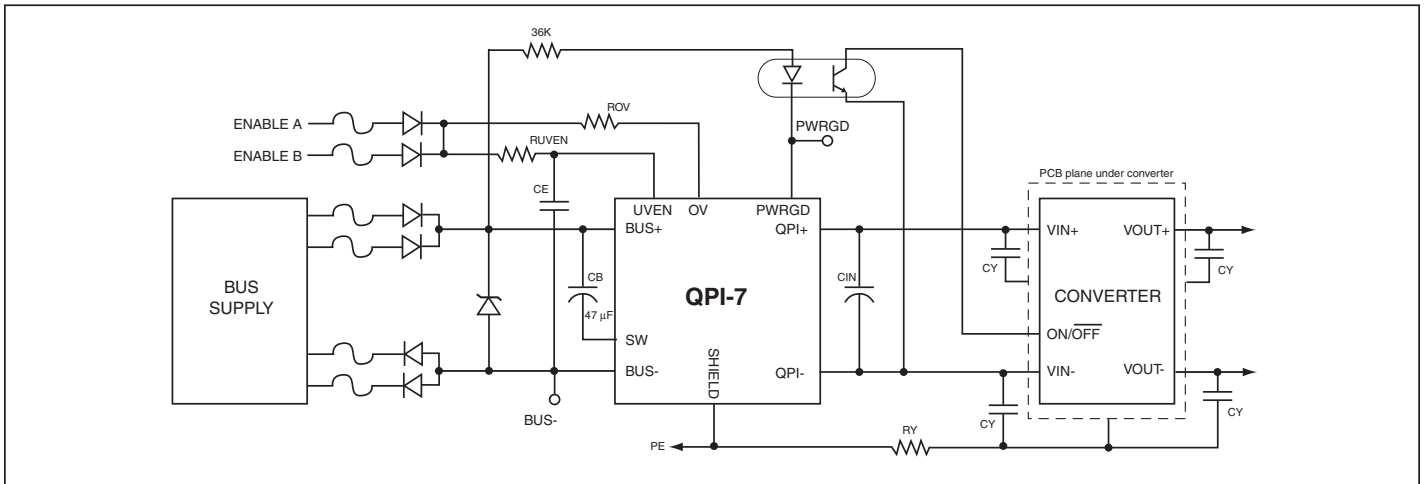


Figure 9b – Typical ATCA System with QPI-7 and High Enable Converter
 (Refer to Figure 15 and QPI-AN1 application note for critical PCB layout guidelines)

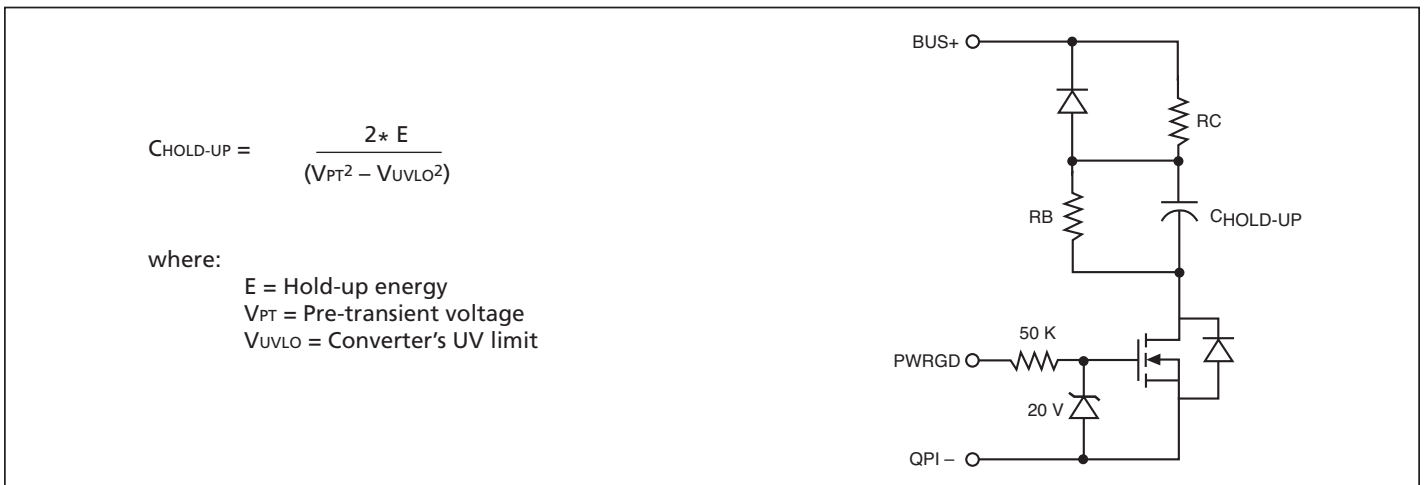


Figure 9c – Powergood controlled, auxiliary bulk storage capacitor charging circuit.

Start-up

The following oscilloscope pictures show the hot swap BUS- current, QPI- to Bus- voltage and PWRGD to BUS- output voltage of the QPI-7 during operation. Figures 10 and 11 are the QPI-7's in-rush characteristics under two load capacitance conditions.

In Figure 10 a 470 mF capacitor required roughly 330 ms to completely charge from a 24 V bus voltage. The QPI-7 can charge large amounts of bulk capacitance to maintain converter operation during 0V Bus transients. Figure 11 shows the QPI-7 charging 4700 uF of load capacitance to 24 V. Under this condition the PWRGD takes about 2.9s to go high after the UVEN input is pulled high. Figure 11's time-scale is too long to show the current pulses that charge the bulk capacitance.

After insertion, when the UVEN voltage exceeds 18 V the UV detection fault is cleared, the QPI-7 goes through a delay cycle (~45ms) to allow for system stabilization and de-bounce. After this time, the QPI- to BUS- path is turned on and current is allowed to pass, monitored by the current sense function. Initially the current level exceeds the 6 A circuit breaker limit, the event timer starts and the power good state is not valid. The sense function and linear control loop will allow twice the circuit breaker current to pass. If the current does not drop below the circuit breaker level prior to reaching the timer limit, typically 800 mS, the QPI- to BUS- path will open. The effective duty cycle under the current limit condition is approximately 1%. Once the load capacitors are fully charged to the input bus potential, the load condition falls below 6 A and the PWRGD pin is asserted high, providing that the bus supply is still within the UV and OV range.

Transient Protection and Recovery

Figures 12 and 13 show the QPI-7's ability to handle low resistance shorts (< 2 W) at the load terminals to emulate fast and slow blown fuse events. In Figure 12, the transient short is 2s long and the QPI- to BUS- path is opened within 1 ms of this occurrence.

Figure 13 demonstrates the QPI-7's performance with a short circuit on its output. The QPI-7 remains in a low duty cycle mode until the short is removed, then restarts normally.

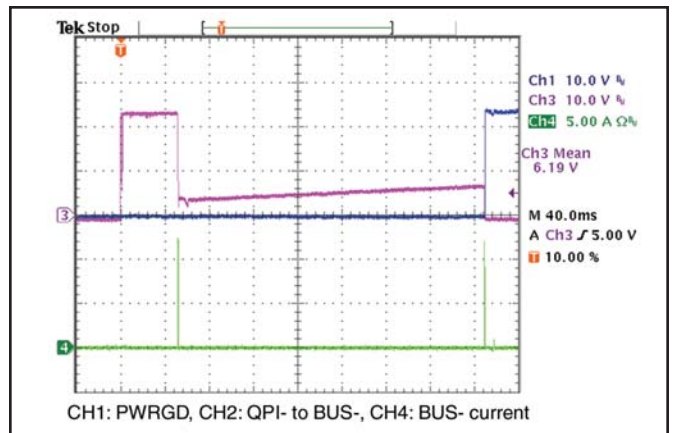


Figure 10 – 470 μ F capacitor @ 24 V

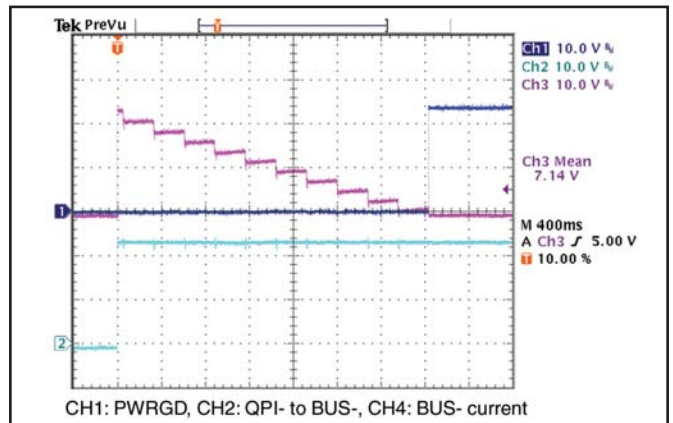


Figure 11 – 4700 mF load capacitor @ 24 V

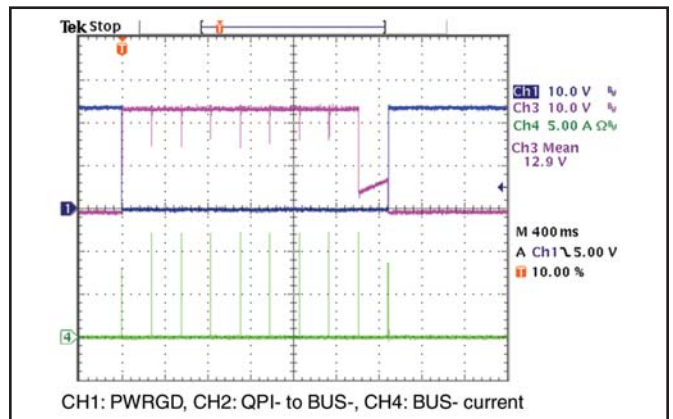


Figure 12 – 2 second short circuit

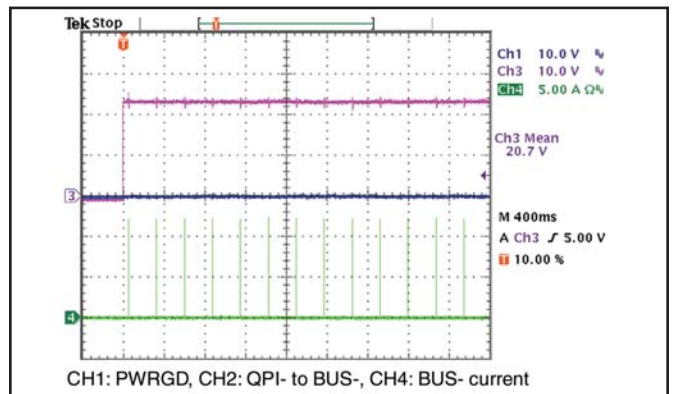


Figure 13 – Start-up into short circuit

QPI-7 PCB Layout Considerations

For optimal QPI-7 filtering performance, care must be taken when routing the signal paths of RY and the shield connections on the pc board. The RY resistor must connect between the converter's shield plane and the shield pin of the QPI-7. The connection to the chassis or protective earth, if required, should be taken directly from the QPI-7 shield pin as shown if Figures 9a and 9b.

Figure 15 shows how this can be accomplished by using the QPI-7's shield pin to bridge the connection between RY and earth without allowing any parasitic paths that might circumvent the QPI-7 and degrade filtering performance. Reference can be made to the QPI-AN1 application note for critical PCB layout recommendations regarding filter performance, but use the QPI-7 pin/pad locations. Some systems may require the converter's positive or negative input or output "terminal" to be connected to PE (Protective Earth) ground for safety or other considerations.

When using the QPI in this situation this "terminal" must be connected to the converter shield plane created in the PCB layout under the converter. Because the PE earth path may pass excessive current under a fault condition the resistance of this path may be limited to a low resistance value. To meet the resistance requirement without degrading filter performance RY can be replaced by a 4.7uH inductor rated for the fault current condition maintaining low power dissipation during a fault until the protection device clears. The shield return pcb traces must be sized to handle this current as well.

Post Solder Cleaning

Picor lidded QP SIPs are not hermetically sealed and must not be exposed to liquid, including but not limited to cleaning solvents, aqueous washing solutions or pressurized sprays.

When soldering, it is recommended that no-clean flux solder be used, as this will insure that potentially corrosive mobile ions will not remain on, around, or under the module following the soldering process.

For applications requiring water wash compatibility the "-01" open frame version should be used.

Ordering Information

Part Number	Description
QPI-7LZ	QPI-7 LGA Package, RoHS Compliant
QPI-7LZ-01	QPI-7 LGA, RoHS Compliant Open Frame Package

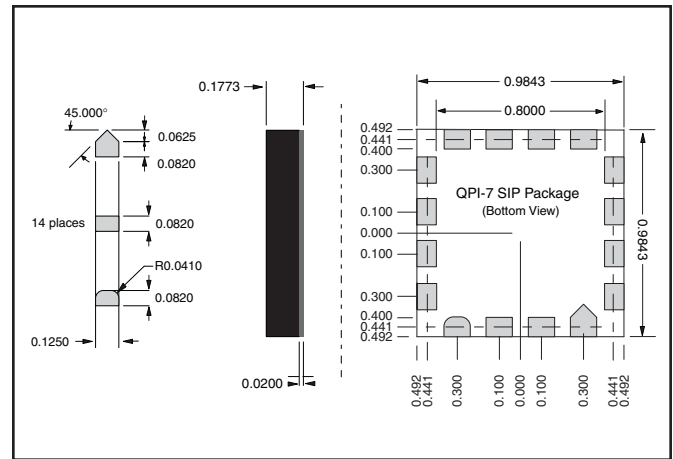


Figure 14 – LGA Pad, package height and pad location dimensions in inches.

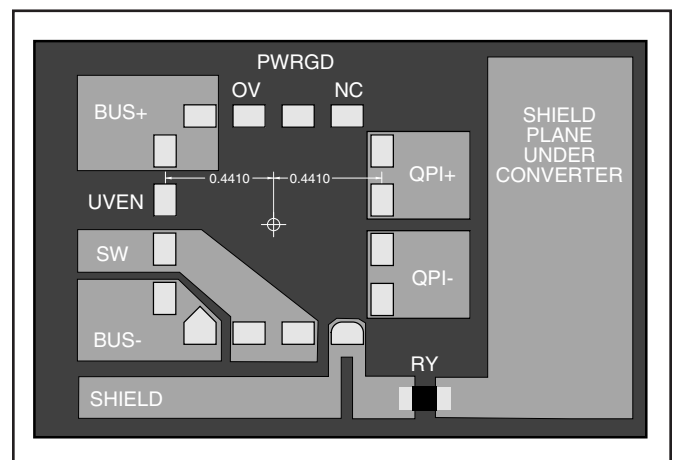


Figure 15 – Recommended PCB layout pattern.

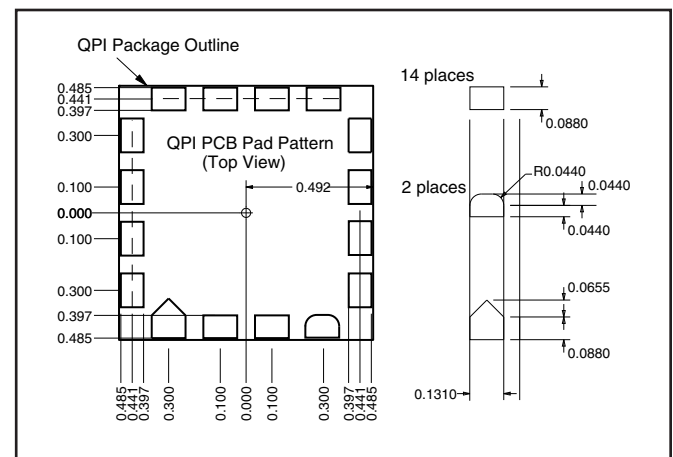


Figure 16 – Recommended PCB receiving footprint.

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Vicor Corporation
25 Frontage Road, Andover, MA, USA 01810
Tel: 800-735-6200 Fax: 978-475-6715

Email
Sales Support: vicorexp@vicorpower.com
Technical Support: apps@vicorpower.com