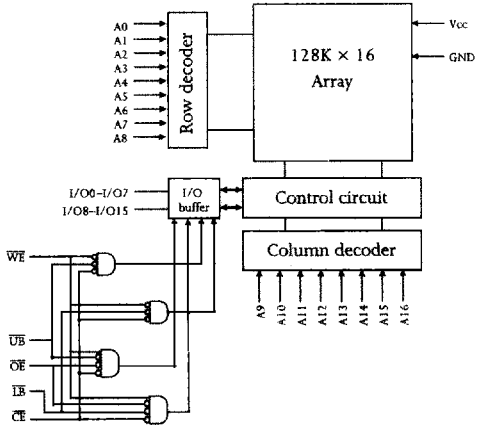
Advance information

Features

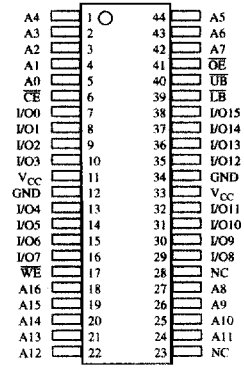
- Organization: 131,072 words × 16 bits
- 3.3V±0.3 operation
- High speed
  - 10/12/15 ns address access time
  - 5/6/8 ns output enable access time
- Low power consumption
  - Active: 504 mW max (15 ns cycle)
  - Standby: 18 mW max, CMOS I/O
  - Very low DC component in active power
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- 44-pin JEDEC standard package
  - 400 mil SOJ
  - 400 mil TSOP II
- Upward and downward compatible
  - 32K×16 (AS7C513)
  - 64K×16 (AS7C1026)
  - 256K×16 (AS7C4098)
- Center power and ground pins for low noise
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- Industrial temperature range available (-40 to +85 °C)
- Optimized for DSP applications

Logic block diagram



Pin arrangement

SOJ, TSOP II



Selection guide

	7C3128K16-10	7C3128K16-12	7C3128K16-15	Unit
Maximum address access time	10	12	15	ns
Maximum output enable access time	5	6	8	ns
Maximum operating current	160	150	140	mA
Maximum CMOS standby current	5	5	5	mA

DID 11-20026-A.

Functional description

The AS7C3128K16 is a high performance CMOS 2 Mbit Static Random Access Memory (SRAM) organized as 131,072 words × 16 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

The AS7C3128K16 is optimized for use in Texas Instruments TMS320C5X DSP applications. Alliance offers 32K,64K,128K, and 256K dep memory devices all in the same pin configuration for interchangeablility.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15 ns with output enable access times (t_{OE}) of 5/6/8 ns are ideal for high performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is High the device enters standby mode. The AS7C3128K16 is guaranteed not to exceed 28 mW power consumption in CMOS standby mode. This device also offers 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0-I/O15 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) High. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

The devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ enables the lower bits, I/O0–I/O7, and $\overline{UB}$ enables the higher bits, I/O8–I/O15.

All chip inputs and outputs are LVTTL-compatible, and operation is from dual 3.3V supplies.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any input pin relative to GND	V_t	−1	+7.0	V
Voltage on any I/O pin relative to GND	V_t	-1	V_{CC}+0.5	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	−55	+150	°C
Temperature under bias	T_{bias}	−10	+85	°C
DC output current	I_{out}	–	50	mA

NOTE: Stresses greater than those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0–I/O7	I/O8–I/O15	Mode
H	X	X	X	X	High Z	High Z	Standby
L	H	L	L	H	D_{OUT}	High Z	Read I/O0–I/O7
L	H	L	H	L	High Z	D_{OUT}	Read I/O8–I/O15
L	H	L	L	L	D_{OUT}	D_{OUT}	Read I/O0–I/O15
L	L	X	L	L	D_{IN}	D_{IN}	Write I/O0–I/O15
L	L	X	L	H	D_{IN}	High Z	Write I/O0–I/O7
L	L	X	H	L	High Z	D_{IN}	Write I/O8–I/O15
L	H	H	X	X	High Z	High Z	Output disable
L	X	X	H	H			

Key: X = don't care, L = Low, H = High

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Recommended operating conditions

Parameter		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	3.0	3.3	3.6	V
		GND	0.0	0.0	0.0	V
Input voltage		V_{IH}	2.0	–	V_{CC} + 0.5	V
		V_{IL}	–0.5†	–	0.8	V
Ambient operating temperature	Commercial	T_A	0	–	70	°C
	Industrial	T_A	-40	–	85	°C

† V_{IL} min = –3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics

Parameter	Symbol	Test conditions	-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	$0V \le V_{in} \le V_{CC}$	–	5	–	5	–	5	µA
Output leakage current	$\lvert I_{LO} \rvert$	Outputs disabled $0V \le V_{out} \le V_{CC}$	–	5	–	5	–	5	µA
Operating power supply current	I_{CC}	$\overline{CE} \le V_{IL}$, V_{CC} = Max, outputs open, $f = f_{Max} = 1/t_{RC}$	–	160	–	150	–	140	mA
Standby power supply current	I_{SB}	$\overline{CE} \le V_{IL}$, V_{CC} = Max, outputs open, $f = f_{Max} = 1/t_{RC}$	–	40	–	40	–	30	mA
	I_{SB1}	$\overline{CE} \ge V_{CC}$–0.2V, V_{CC} = Max, $V_{in} \le$ GND + 0.2V or $V_{in} \ge V_{CC}$ - 0.2V, f = 0	–	5	–	5	–	5	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min	2.4	–	2.4	–	2.4	–	V

Shaded areas indicate preliminary information.

Capacitance

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{in} = V_{out}$ = 0V	7	pF

Read cycle [3,9]

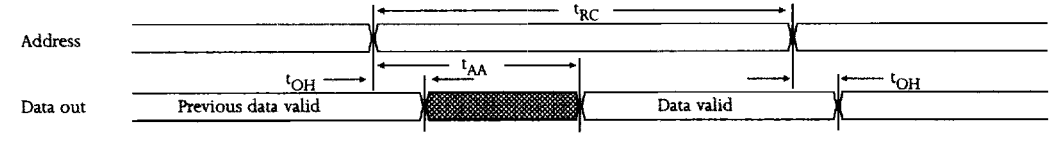
Parameter	Symbol	-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	Unit	Notes
Read cycle time	t_{RC}	10	–	12	–	15	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	10	–	12	–	15	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	5	–	6	–	8	ns	
Output hold from address change	t_{OH}	4	–	4	–	4	–	ns	5
$\overline{CE}$ Low to output in low Z	t_{CLZ}	0	–	0	–	0	–	ns	4, 5
$\overline{CE}$ High to output in high Z	t_{CHZ}	–	6	–	6	–	6	ns	4, 5
$\overline{OE}$ Low to output in low Z	t_{OLZ}	0	–	0	–	0	–	ns	4, 5
Byte select access time	t_{BA}	–	5	–	6	–	8	ns	
Byte select Low to low Z	t_{BLZ}	0	–	0	–	0	–	ns	4,5
Byte select High to high Z	t_{BHZ}	–	5	–	6	–	6	ns	4,5
$\overline{OE}$ High to output in high Z	t_{OHZ}	–	5	–	6	–	6	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	ns	4, 5
Power down time	t_{PD}	–	10	–	12	–	15	ns	4, 5

Shaded areas indicate preliminary information.

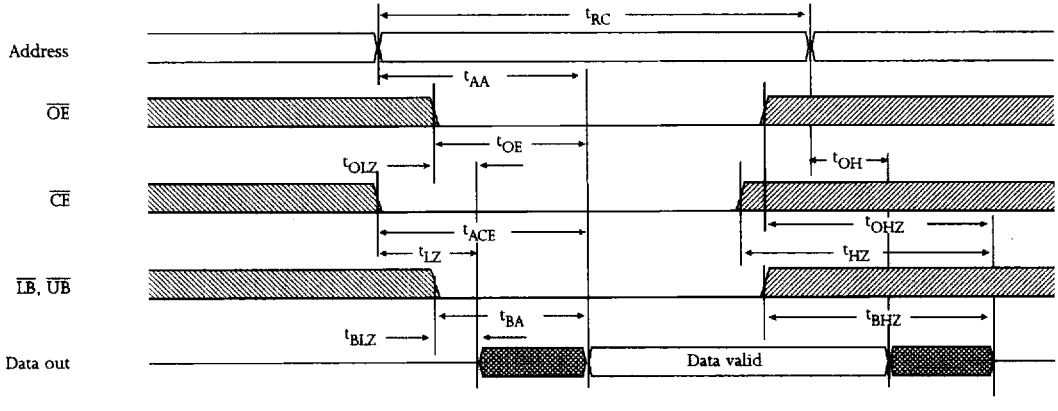
Key to switching waveforms

Rising input Falling input Undefined output/don't care

Read waveform 1 [3,6,7,9]



Read waveform 2 [3,6,8,9]



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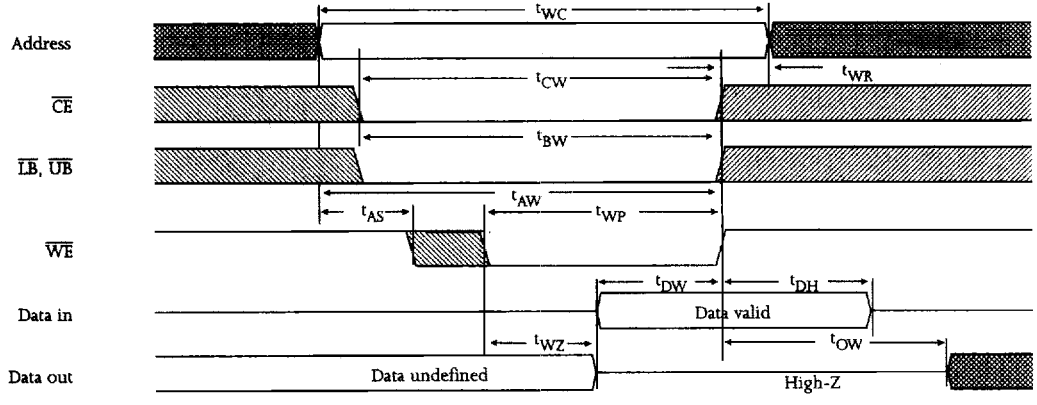
Write cycle[11]

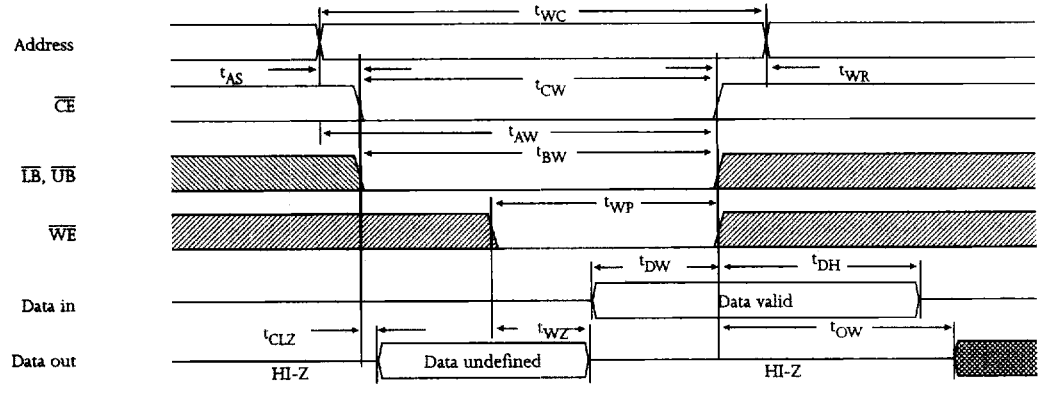
Parameter	Symbol	-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	Unit	Notes
Write cycle time	t_{WC}	10	–	12	–	15	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	9	–	10	–	12	–	ns	
Address setup to write end	t_{AW}	8	–	9	–	10	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	ns	
Write pulse width	t_{WP}	8	–	9	–	10	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5	–	6	–	8	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	ns	5
Write enable to output in high Z	t_{WZ}	–	6	–	6	–	6	ns	4, 5
Output active from write end	t_{OW}	1	–	1	–	1	–	ns	4, 5
Byte select low to end of write	t_{BW}	8	–	9	–	9	–	ns	

Shaded areas indicate preliminary information.

Write waveform 1[10,11]



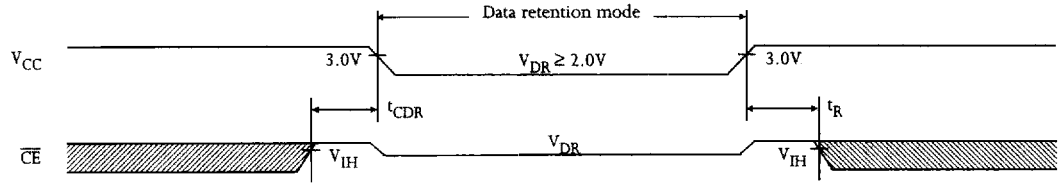
Write waveform 2[10,11]



Data retention characteristics [13]

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0V	2.0	–	V
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CC}-0.2V$	–	500	µA
Chip deselect to data retention time	t_{CDR}	$V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns
Input leakage current	$\lvert I_{LI} \rvert$		–	1	µA

Data retention waveform



AC test conditions

- Output load: see Figure B, except as noted.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

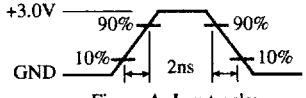


Figure A: Input pulse

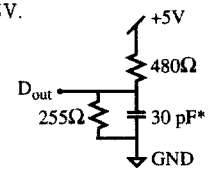


Figure B: Output load

Thevenin Equivalent:

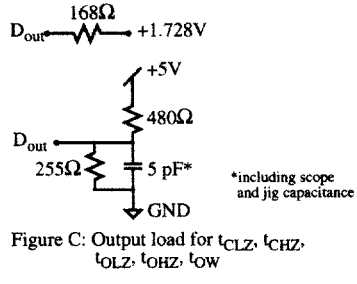
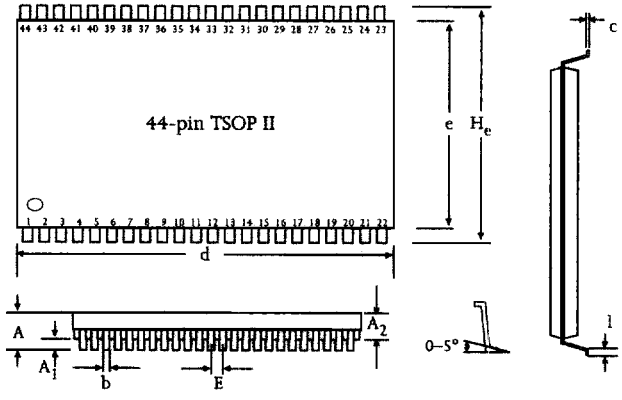


Figure C: Output load for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{OW}

Notes

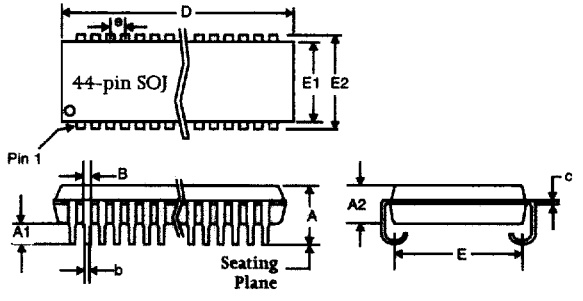
1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, C.
4 These parameters are specified with C_L = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is High for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE}$ or $\overline{WE}$ must be High during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 This data applicable to AS7C3128K16 only. The AS7C31026 functions similarly.
13 2V data retention applies to commercial temperature range operation only.

Package dimensions



44-pin TSOP II

	Min (mm)	Max (mm)
A		1.2
A_1	0.05	
A_2	0.95	1.05
b	0.25	0.45
c	0.15 (typical)	
d	20.85	21.05
e	10.06	10.26
H_e	11.56	11.96
E	0.80 (typical)	
l	0.40	0.60



44-pin SOJ
400 mil

	Min	Max
A	0.128	0.148
A1	0.025	-
A2	1.105	1.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 NOM	
E1	0.395	0.405
E2	0.435	0.445
e	0.050 NOM	

AS7C3128K16 ordering codes

Package \ Access time		10 ns	12 ns	15 ns
Plastic SOJ, 400 mil	3.3V commercial	AS7C3128K16-10JC	AS7C3128K16-12JC	AS7C3128K16-15JC
TSOP II, 18.4×10.2 mm	3.3V commercial	AS7C3128K16-10TC	AS7C3128K16-12TC	AS7C3128K16-15TC

Note: Contact Alliance for industrial temperature availability.

AS7C3128K16 part numbering system

AS7C	3	128K16	-XX	X	C
SRAM prefix	3 = 3.3V CMOS	Device number	Access time	Package: J = SOJ 400 mil T = TSOP type 2, 18.4×10.2 mm	Temperature range, C = Commercial: 0°C to 70°C I = Industrial: -40°C to 85°C