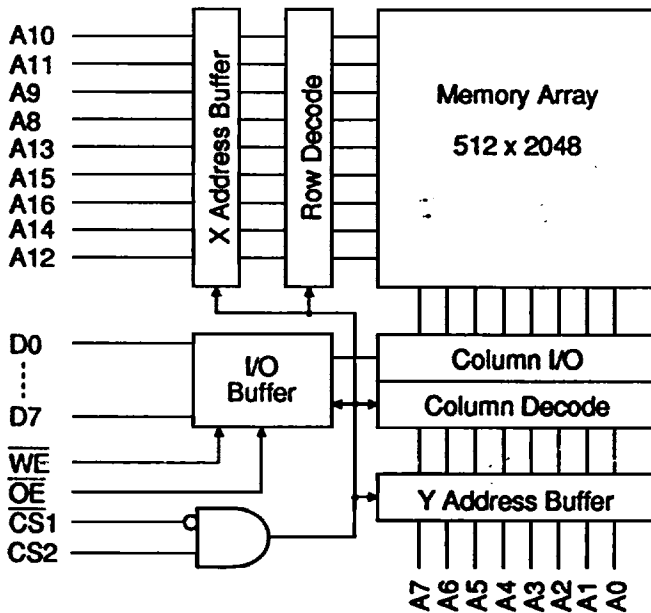# mo∫aic

Mosaic
Semiconductor
Inc.

131,072 x 8 CMOS High Speed Static RAM

Features

Very Fast Access Times of 45/55/70 ns
JEDEC Standard 32 pin DIL footprint
VIL™ High Density Package Available
Low Power Standby   50µW (typ.)
Low Power Operation 150mW(typ.)
Completely Static Operation
3.0V Battery Back-up Capability.
Directly TTL compatible
Common data inputs & outputs
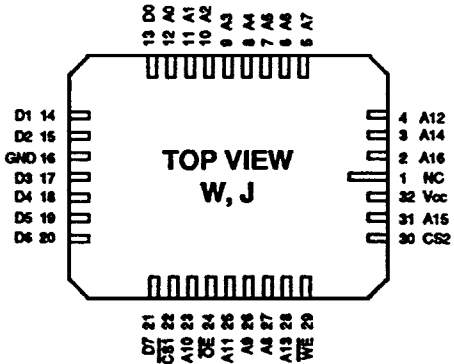May be processed in accordance with MIL-STD-883

Block Diagram

Pin Definition

Pin assignments (DIP TOP VIEW S, K, V, G):

Pin	Name		Pin	Name
1	NC		32	VCC
2	A16		31	A15
3	A14		30	CS2
4	A12		29	WE
5	A7		28	A13
6	A6		27	A8
7	A5		26	A9
8	A4		25	A11
9	A3		24	OE
10	A2		23	A10
11	A1		22	CS1
12	A0		21	D7
13	D0		20	D6
14	D1		19	D5
15	D2		18	D4
16	GND		17	D3

TOP VIEW W, J (chip carrier)

Pin Functions

Pin	Function
A0-A16	Address Inputs
D0-7	Data Input/Output
CS1	Chip Select 1
CS2	Chip Select 2
OE	Output Enable
WE	Write Enable
NC	No Connect
V$_{cc}$	Power (+5V)
GND	Ground

Package Details

Pin Count	Description	Package Type	Material	Pin Out
32	0.6" Dual-in-Line (DIP)	S	Ceramic	JEDEC
32	0.4" Dual-in-Line (DIP)	K	Ceramic	JEDEC
32	0.1" Vertical-in-Line (VIL™)	V	Ceramic	JEDEC
32	Bottom Brazed Flat Pack	G	Ceramic	JEDEC
32	Extended Leadless Chip Carrier (LCC)	W	Ceramic	JEDEC PENDING
32	J-Leaded Chip Carrier (JLCC)	J	Ceramic	JEDEC PENDING

Package dimensions and outlines are displayed on pages 6&7.
VIL is a trademark of Mosaic Semiconductor, US patent No. D316251

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	V_T	-0.5V to +7	V	
Power Dissipation	P_T	1	W	
Storage Temperature	T_{STG}	-65 to +150	°C	

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -3.0V pulse of less than 30ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	5.8	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (8128I)
	T_{AM}	-55	-	125	°C (8128M, MB)

Notes : (1) V_{IL} can be -3.0V pulse of less than 30ns.

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IH}=Gnd to V_{cc}	-2	-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH}, $\overline{CS2}$ =V_{IL},V_{OUT}=GND to V_{CC}				
		$\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}	-2	-	2	μA
Operating Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, $\overline{CS2}$ = V_{IH},I_{OUT}=0mA	-	30	80	mA
Average Supply Current	I_{CC1}	Min. Cycle, duty=100%, I_{OUT}=0mA,$\overline{WE}$=V_{IH}	-	60	120	mA
StandbySupply Current	I_{SB}	$\overline{CS1}$=V_{IH},$\overline{CS2}$ = V_{IL},V_{IN}=V_{IH} or V_{IL}	-	-	15	mA
	I_{SB1}	$\overline{CS1}$≥V_{CC}-0.2V, $\overline{CS2}$ ≤ 0.2V				
		0.2V≥V_{IN}≥V_{CC}-0.2V	-	0.01	2	mA
Output Voltage	V_{OL}	I_{OL}=6.0mA for -45 and -55 speed device	-	-	0.4	V
		I_{OL}=2.1 mA for -70 speed device				
	V_{OH}	I_{OH}=-4.0mA for -45 and -55 speed device	2.4	-	-	V
		I_{OH}=-1 mA for -70 speed device				

Note 1: Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%,T_A=25°C)

Parameter	Symbol	Test Condition	typ	max	Unit
I/P Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF

Note: This parameter is sampled and not 100% tested.

AC Test Conditions   Output Load

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: See Load Diagram
* V_{CC}=5V±10%
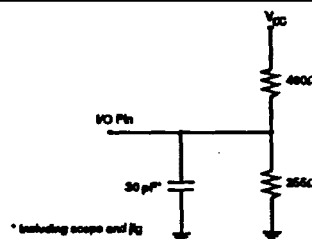
Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

Parameter	Symbol	-45 min	-45 max	-55 min	-55 max	-70 min	-70 max	Units
Read Cycle Time	t_{RC}	45	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	45	-	55	-	70	ns
Chip Selection ($\overline{CS1}$) Access Time	t_{CO1}	-	45	-	55	-	70	ns
Chip Selection ($\overline{CS2}$) Access Time	t_{CO2}	-	45	-	55	-	70	ns
Output Enable to Output Valid	t_{OE}	-	25	-	30	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns
Chip Selection ($\overline{CS1}$) to O/P in Low Z[2]	t_{LZ1}	5	-	5	-	5	-	ns
Chip Selection ($\overline{CS2}$) to O/P in Low Z[2]	t_{LZ2}	5	-	5	-	5	-	ns
Output Enable to Output in Low Z[2]	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselect ($\overline{CS1}$) to O/P in high Z[2]	t_{HZ1}	0	20	0	25	0	30	ns
Chip Deselect ($\overline{CS2}$) to O/P in high Z[2]	t_{HZ2}	0	20	0	25	0	30	ns
Output Disable to Output in High Z[2]	t_{OHZ}	0	20	-	25	-	30	ns

## Read Cycle Timing Waveform [1]
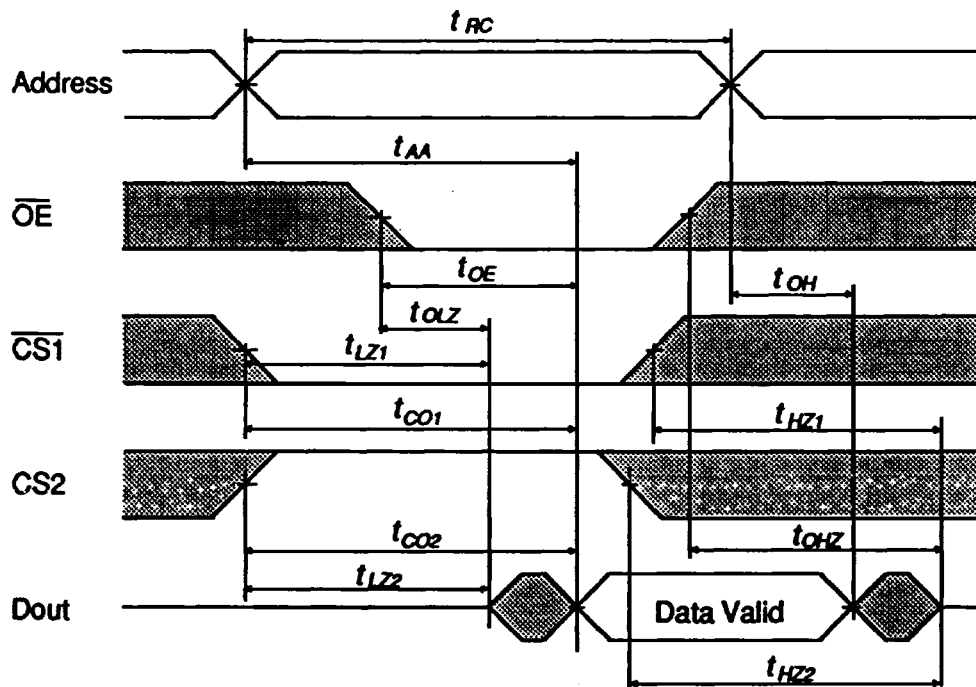
Notes:
(1) $\overline{WE}$ is High for Read Cycle.
(2) t_{LZ} and t_{OLZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. At any given temperature and voltage condition, t_{LZ} max is less than t_{LZ} min both for a given device and from device to device. This parameter is sampled and not 100% tested.

Write Cycle

Parameter	Symbol	-45 min	-45 max	-55 min	-55 max	-70 min	-70 max	Unit	Notes
Write Cycle Time	t_{WC}	45	-	55	-	70	-	ns	
Chip Selection to End of Write	t_{CW}	40	-	45	-	50	-	ns	
Address Valid to End of Write	t_{AW}	40	-	45	-	50	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	·ns	
Write Pulse Width	t_{WP}	35	-	40	-	45	-	ns	
Write Recovery Time	t_{WR}	3	-	3	-	3	-	ns	
		5	-	5	-	5	-	ns	(11)
Write to Output in High Z	t_{WHZ}	0	25	0	30	0	35	ns	(10)
Data to Write Time Overlap	t_{DW}	20	-	25	-	30	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns	(10)

Write Cycle No.1 Timing Waveform

Write Cycle No.2 Timing Waveform (12)
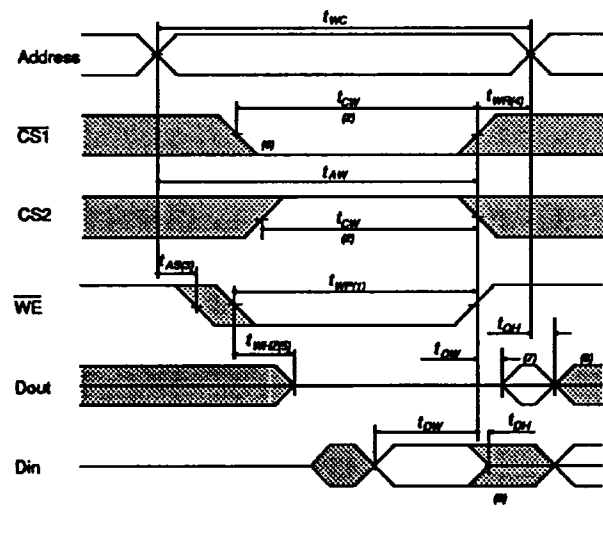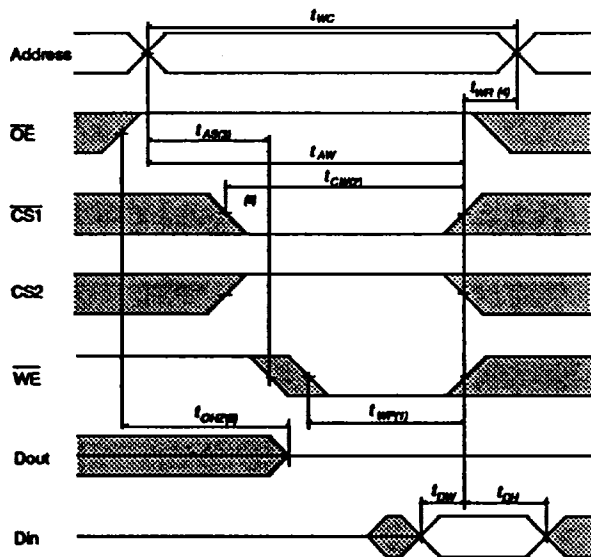
AC Characteristics Notes

(1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ goig high. t_{WC} is measured from the beginning of write to the end of write.

(2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

(3) t_{AS} is measured from the address valid to the beginning of write.

(4) t_{WR} is measured from the earlier of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going high to the end of write cycle.

(5) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, outputs remain in high impedance state.

(7) Dout is in the same phase as written data of this write cycle.

(8) Dout is the read data of next address.

(9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.

(10) t_{WHZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. These parameters are sampled and not 100% tested.

(11) This value is mesured from CS2 going low to the end of the write cycle.

(12) $\overline{OE}$ is continuously low. ($\overline{OE}=V_{IL}$)

Low V_{cc} Data Retention Characteristics - L Version Only (T_A=-55°C to +125°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{cc} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{cc}$-0.2V, CS2 $\geq V_{cc}$-0.2V or 0V $\leq$ CS2 $\leq$ 0.2V. $V_{IN} \geq$ 0V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{cc}=3.0V,$V_{IN} \geq$ 0V, $\overline{CS1} \geq V_{cc}$-0.2V, CS2 $\geq V_{cc}$-0.2V or 0V $\leq$ CS2 $\leq$ 0.2V.	-	-	700	µA
Chip Deselect to Data Retention	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Notes (1) CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer and $\overline{OE}$ buffer. If CS2 controls data retention mode, Vin levels ($\overline{WE},\overline{OE},\overline{CS1}$,I/O) can be in the high impedance state. If $\overline{CS1}$ controls Data Retention mode, CS2 must be $\geq V_{cc}$ - 0.2V or 0V $\leq$ CS2 $\leq$ 0.2V. The other input levels (address, $\overline{WE},\overline{OE}$,I/O) can be in the high impedance state.

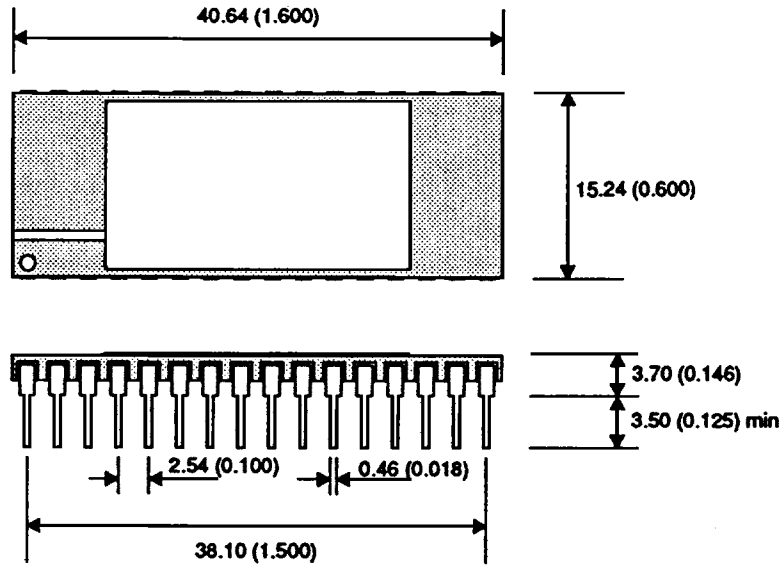## Low V_{cc} Data Retention Timing Waveform 1 ($\overline{CS1}$ controlled)
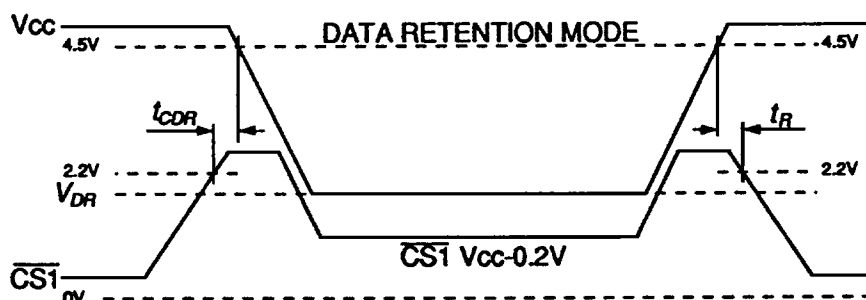
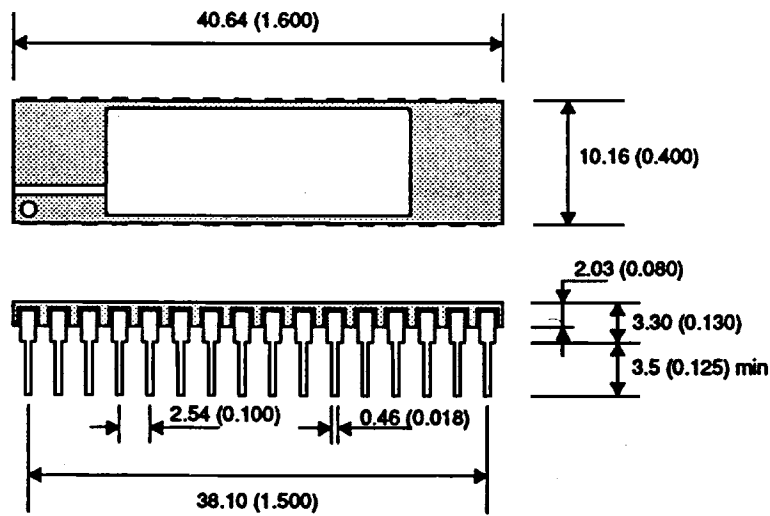
Low V_{cc} Data Retention Timing Waveform 2 (CS2 controlled)

5
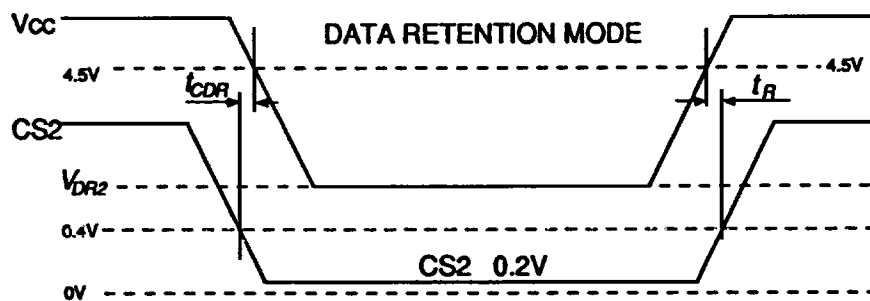
Package Details Dimensions in mm (inches). Tolerance on all dimensions ±0.254 (0.01)
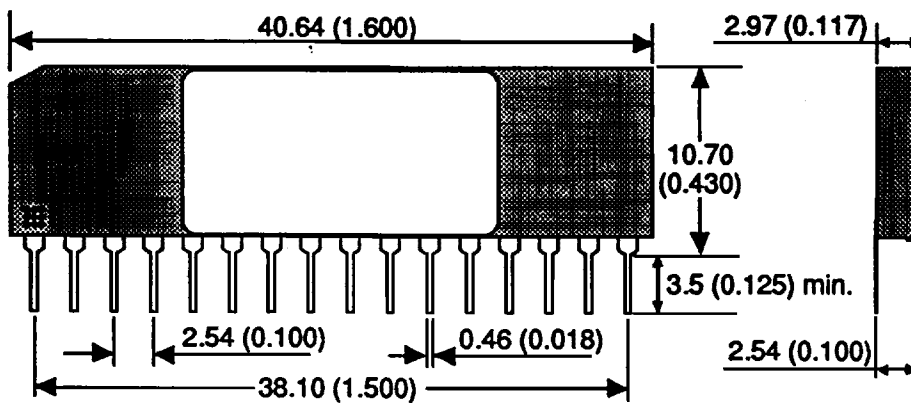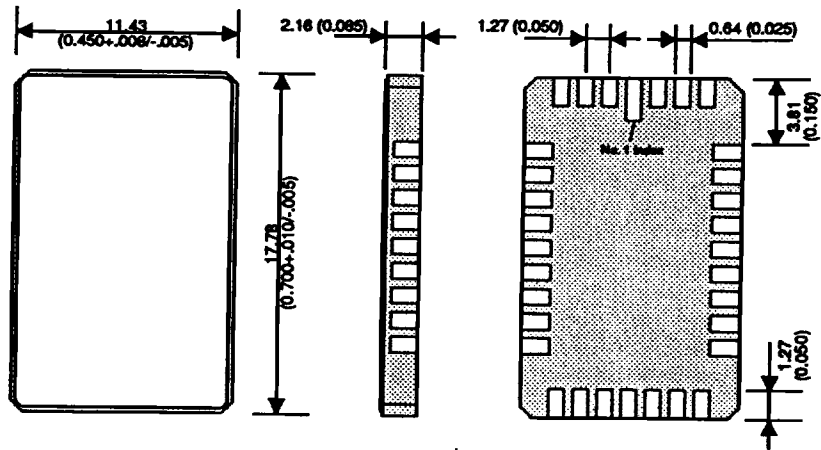
32 pin 0.6" Dual-In-Line (DIP) - 'S' Package

40.64 (1.600)

15.24 (0.600)

3.70 (0.146)

3.50 (0.125) min

2.54 (0.100)   0.46 (0.018)

38.10 (1.500)

32 pin 0.4" Dual-In-Line (DIP) - 'K' Package

40.64 (1.600)

10.16 (0.400)

2.03 (0.080)

3.30 (0.130)

3.5 (0.125) min

2.54 (0.100)   0.46 (0.018)

38.10 (1.500)

32 pin 0.1" Vertical-In-Line (VIL™) - 'V' Package

40.64 (1.600)   2.97 (0.117)

10.70
(0.430)

3.5 (0.125) min.

2.54 (0.100)   0.46 (0.018)

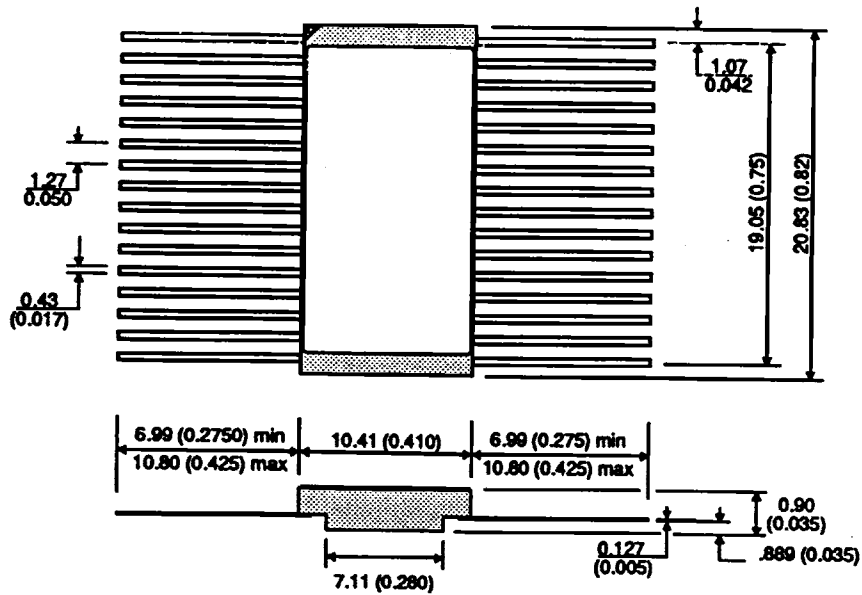38.10 (1.500)   2.54 (0.100)

32 pin Extended Leadless Chip Carrier (LCC) - 'W' Package

32 pin Extended 'J' Leaded Chip Carrier (JLCC) - 'J' Package
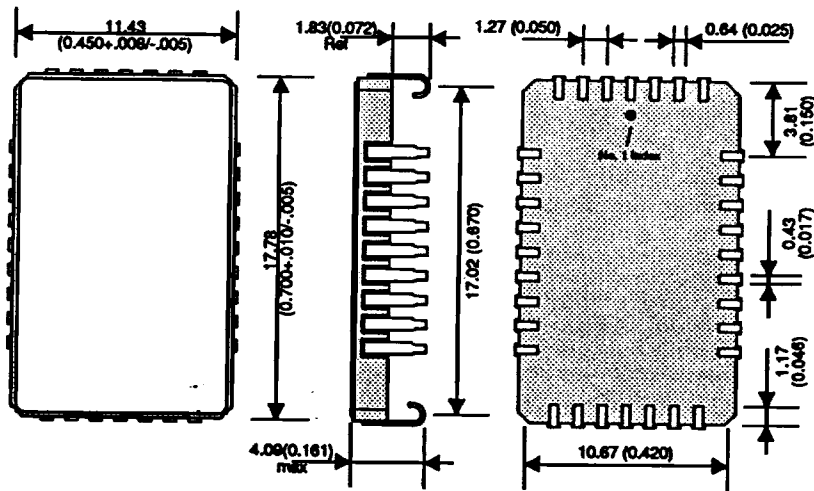
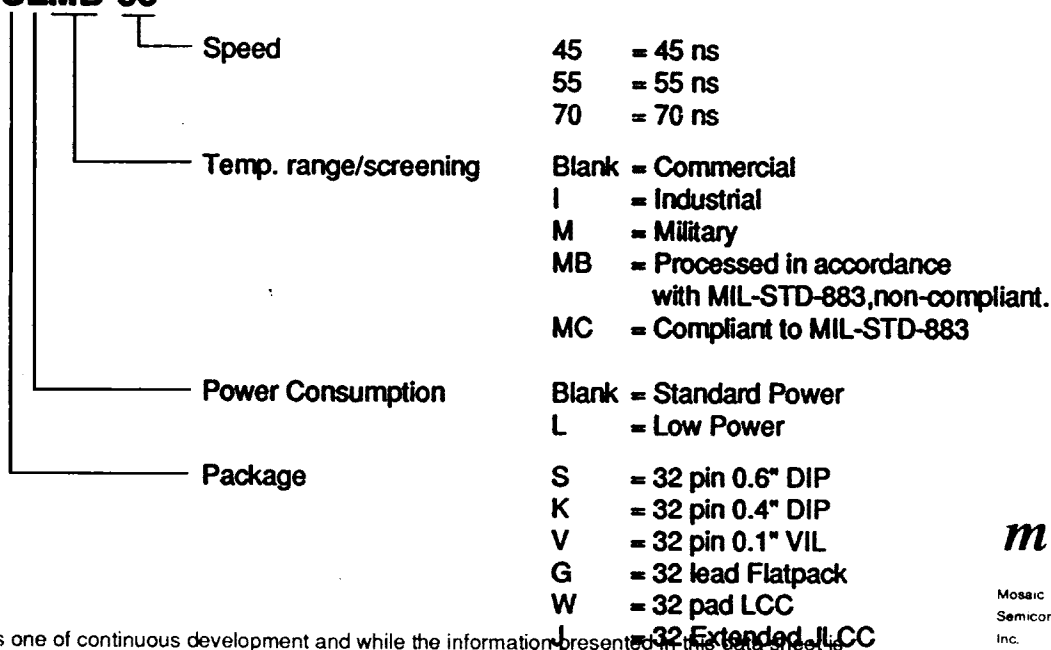## 32 pin Ceramic Flatpack - 'G' Package

Military Screening Procedure

Component Screening Flow for high reliability non-compliant product is detailed below:

MB COMPONENT SCREENING FLOW

SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles, -65°C to +150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	Method 1015, Condition D, T_A=+125°C, 160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

MSM8128SLMB-55

- Speed
  - 45 = 45 ns
  - 55 = 55 ns
  - 70 = 70 ns
- Temp. range/screening
  - Blank = Commercial
  - I = Industrial
  - M = Military
  - MB = Processed in accordance with MIL-STD-883, non-compliant.
  - MC = Compliant to MIL-STD-883
- Power Consumption
  - Blank = Standard Power
  - L = Low Power
- Package
  - S = 32 pin 0.6" DIP
  - K = 32 pin 0.4" DIP
  - V = 32 pin 0.1" VIL
  - G = 32 lead Flatpack
  - W = 32 pad LCC
  - J = 32 Extended LCC

mo∫aic

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