

Quad buffer/line driver (3-state)

74AC126
74ACT126

FEATURES

- 74ACT126 has TTL-compatible inputs
- 74AC126 has CMOS-compatible inputs
- 3-State outputs source/sink 24mA
- 3-State outputs drive bus lines or buffer memory address registers
- Meets or exceeds JEDEC standard standard for 74AC(T)XX family

DESCRIPTION

The 74AC126/ 74ACT126 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74AC126 consists of four independent non-inverting buffers/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL			UNIT
			AC		ACT	
			V _{CC} = 3.3V	V _{CC} = 5.0V	V _{CC} = 5.0V	
t _{PHL} /t _{PLH}	Propagation delay nA to nY	C _L = 50pF V _{CC} = 3.3V	3.5	2.6	4.2	ns
C _I	Input capacitance		4.5			pF
C _{PD}	Power dissipation capacitance per buffer	V _I = GND to V _{CC} ¹ outputs enabled outputs disabled	23 6		23 4	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

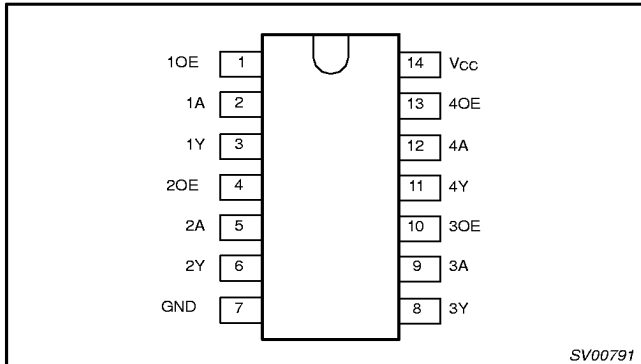
ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
14-Pin Plastic SOL	-40°C to +85°C	74AC126 D 74ACT126 D	74AC126 D 74ACT126 D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to +85°C	74AC126 DB 74ACT126 DB	74AC126 DB 74ACT126 DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to +85°C	74AC126 PW 74ACT126 PW	74AC126PW DH 74ACT126PW DH	SOT402-1

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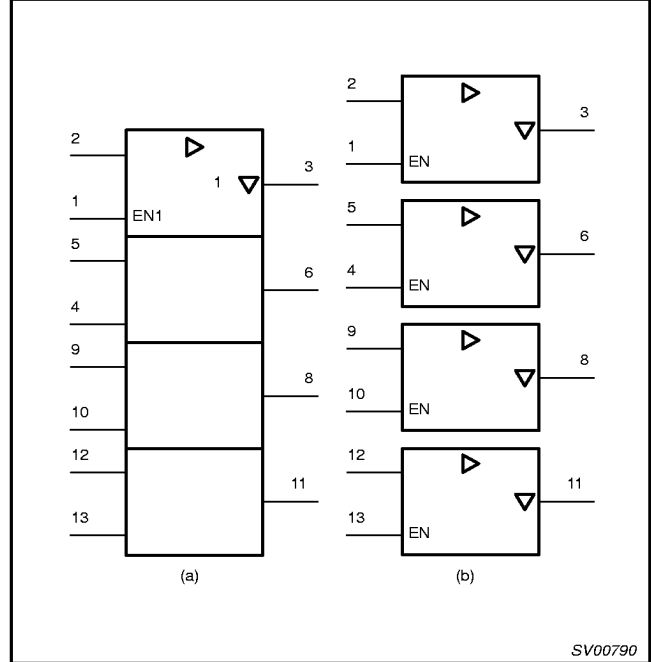
PIN CONFIGURATION



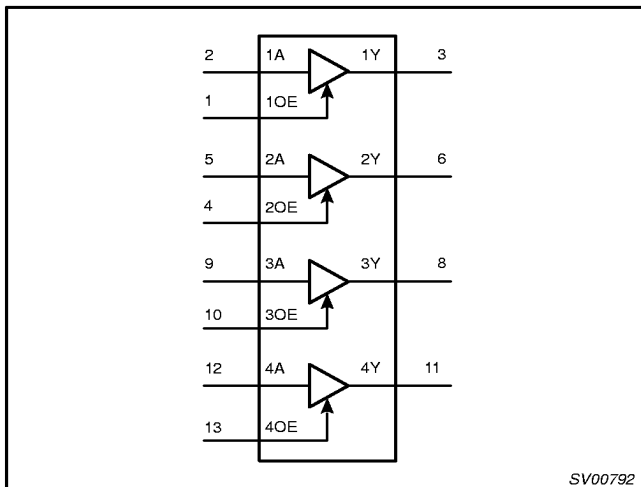
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1OE to 4OE	Data enable inputs (active HIGH)
2, 5, 9, 12	1A to 4A	Data inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0 V)
14	V _{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL

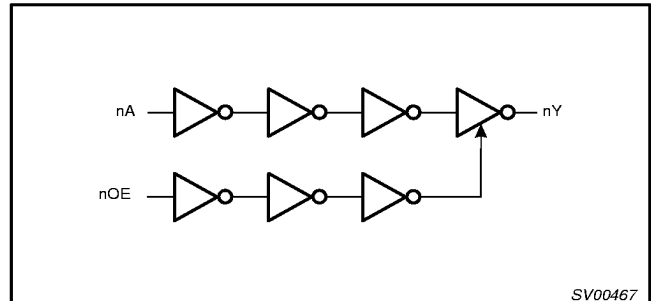


FUNCTION TABLE

INPUTS		OUTPUT
nOE	nA	nY
H	H	H
H	L	L
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC DIAGRAM



Quad buffer/line driver (3-state)

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage for 'AC	2.0	6.0	V
V _{CC}	DC supply voltage for 'ACT	4.5	5.5	V
V _{IN}	DC input voltage range	0	V _{CC}	V
V _O	DC output voltage range	0	V _{CC}	V
T _{amb}	Operating free-air temperature range	-40	+85	°C
ΔV/Δt	Minimum input edge rate — AC devices V _{IN} from 30% to 70% of V _{CC} V _{CC} @ 3.3V, 4.5V, 5.5V	125		mV/ns
	— ACT devices V _{IN} from 0.8V to 2.0V V _{CC} @ 4.5V, 5.5V	125		

ABSOLUTE MAXIMUM RATINGS¹

in accordance with the Absolute Maximum Rating System (IEC134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _{IN} = -0.5V	-20	mA
		V _{IN} = V _{CC} + 0.5V	+20	
V _{IN}	DC input voltage		-0.5 to V _{CC} + 0.5	V
I _{OK}	DC output diode current	V _O = -0.5V	-20	mA
		V _O = V _{CC} + 0.5V	+20	
V _O	DC output voltage		-0.5 to V _{CC} + 0.5	V
I _O	DC output source or sink current		± 50	mA
I _{CC} , I _{GND}	DC V _{CC} or GND current per output		± 50	mA
I _{CC} , I _{GND}	DC V _{CC} or GND current		± 200	mA
T _{stg}	Storage temperature range		-65 to 150	°C
P _{TOT}	Power dissipation per package — plastic mini-pack (SO) — plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K	500	mW
		above +60°C derate linearly with 5.5 mW/K	500	

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Quad buffer/line driver (3-state)

74AC126
74ACT126**DC ELECTRICAL CHARACTERISTICS (74AC126)**

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} (V)	LIMITS			UNIT	
				Temp = -40°C to +85°C				
				MIN	TYP ¹	MAX		
V _{IH}	HIGH level Input voltage	V _{OUT} = 0.1V or (V _{CC} - 0.1V)	3.0	2.1	1.5		V	
			4.5	3.15	2.25			
			5.5	3.85	2.75			
V _{IL}	LOW level Input voltage	V _{OUT} = 0.1V or (V _{CC} - 0.1V)	3.0		1.5	0.9	V	
			4.5		2.25	1.35		
			5.5		2.75	1.65		
V _{OH}	HIGH level output voltage	I _{OUT} = -50 μA	3.0	2.9	2.99		V	
			4.5	4.4	4.49			
			5.5	5.4	5.49			
			V _{IN} = V _{IL} or V _{IH} , I _{OH} = -12mA ¹	3.0	2.46			V
			V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ¹	4.5	3.76			
			V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ¹	5.5	4.76			
V _{OL}	LOW level output voltage	I _{OUT} = 50 μA	3.0		0.01	0.1	V	
			4.5		0.01	0.1		
			5.5		0.01	0.1		
			V _{IN} = V _{IL} or V _{IH} , I _{OL} = 12mA ¹	3.0			0.44	V
			V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ¹	4.5			0.44	
			V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ¹	5.5			0.44	
I _{IN}	Input leakage current	V _{IN} = V _{CC} , GND	5.5			±1.0	μA	
I _{OZ}	3-State output OFF-state current	V _{IN} (OE) = V _{IL} , V _{IH} V _{IN} = V _{CC} , GND V _{OUT} = V _{CC} , GND	5.5			±2.5	μA	
I _{OLD} ²	Dynamic output current ²	V _{OLD} = 1.65V max	5.5	75			mA	
I _{OHD} ²	Dynamic output current ²	V _{OHD} = 3.85V min	5.5			-75	mA	
I _{CC}	Quiescent supply current	V _{IN} = V _{CC} or GND	5.5			40	μA	

NOTES:

1. All outputs loaded
2. Maximum test duration 2.0 ms; one output loaded at a time

Quad buffer/line driver (3-state)

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74ACT126**DC ELECTRICAL CHARACTERISTICS (74ACT126)**

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{OUT} = 0.1V or (V _{CC} - 0.1V)	4.5	2.0	1.5		V
			5.5	2.0	1.5		
V _{IL}	LOW level Input voltage	V _{OUT} = 0.1V or (V _{CC} - 0.1V)	4.5		1.5	0.8	V
			5.5		1.5	0.8	
V _{OH}	HIGH level output voltage	I _{OUT} = -50 μA	4.5	4.4	4.49		V
			5.5	5.4	5.49		
		V _{IN} = V _{IL} or V _{IH} ; I _{OH} = -24mA ¹	4.5	3.76			V
		V _{IN} = V _{IL} or V _{IH} ; I _{OH} = -24mA ¹	5.5	4.76			
V _{OL}	LOW level output voltage	I _{OUT} = 50 μA	4.5		0.01	0.1	V
			5.5		0.01	0.1	
		V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 24mA ¹	4.5			0.44	V
		V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 24mA ¹	5.5			0.44	
I _{IN}	Input leakage current	V _{IN} = V _{CC} , GND	5.5			±1.0	μA
I _{OZ}	3-State output OFF-state current	V _{IN} (OE) = V _{IL} , V _{IH} V _{IN} = V _{CC} , GND V _{OUT} = V _{CC} , GND	5.5			±2.5	μA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{IN} = V _{CC} - 2.1V Other inputs at V _{CC} or GND; I _{OUT} = 0	5.5			1.5	mA
I _{OLD} ²	Dynamic output current	V _{OLD} = 1.65V max	5.5	75			mA
I _{OHD} ²	Dynamic output current	V _{OHD} = 3.85V min	5.5			-75	mA
I _{CC}	Quiescent supply current	V _{IN} = V _{CC} or GND	5.5			40	μA

NOTES:

- All outputs loaded
- Maximum test duration 2.0ms, one output loaded at a time

Quad buffer/line driver (3-state)

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74ACT126**AC CHARACTERISTICS FOR 74AC126**GND = 0V; $t_r = t_f = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; .

SYMBOL	PARAMETER	V_{CC}^1 (V)	LIMITS					UNIT	WAVEFORM
			$T_{amb} = +25^\circ\text{C}$			$T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$			
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	Propagation delay nA to nY	3.3 5.0	2.0 1.5	3.5 2.6	9.0 6.5	1.5 1.0	10.0 7.5	ns	1, 3
t_{PHL}	Propagation delay nA to nY	3.3 5.0	2.0 1.5	3.5 2.6	9.0 6.5	1.5 1.0	10.0 7.5	ns	1, 3
t_{PZH}	3-State output enable time nOE to nY	3.3 5.0	2.0 1.5	4.5 3.1	9.5 7.0	1.5 1.0	11.0 8.0	ns	2, 3
t_{PZL}	3-State output enable time nOE to nY	3.3 5.0	2.0 1.5	4.7 3.2	9.5 8.0	1.5 1.0	11.0 8.0	ns	2, 3
t_{PHZ}	3-State output disable time nOE to nY	3.3 5.0	2.0 1.5	5.0 3.5	9.0 7.5	1.5 1.0	10.0 7.5	ns	2, 3
t_{PLZ}	3-State output disable time nOE to nY	3.3 5.0	2.0 1.5	4.4 3.0	9.0 7.5	1.5 1.0	10.0 7.5	ns	2, 3

NOTE:

1. Voltage range 3.3V is $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$
Voltage range 5.0V is $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$

AC CHARACTERISTICS FOR 74ACT126GND = 0V; $t_r = t_f = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; .

SYMBOL	PARAMETER	V_{CC}^1 (V)	LIMITS					UNIT	WAVEFORM
			$T_{amb} = +25^\circ\text{C}$			$T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$			
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	Propagation delay nA to nY	5.0	2.0	4.7	9.0	1.5	10.0	ns	1, 3
t_{PHL}	Propagation delay nA to nY								
t_{PZH}	3-State output enable time OE to nY	5.0	2.0	4.5	8.5	1.5	9.5	ns	1, 3
t_{PZL}	3-State output enable time OE to nY	5.0	2.0	4.7	8.5	1.5	9.5	ns	2, 3
t_{PHZ}	3-State output disable time OE to nY	5.0	2.0	4.0	8.0	1.5	9.0	ns	2, 3
t_{PLZ}	3-State output disable time OE to nY	5.0	2.0	3.6	8.0	1.5	9.0	ns	2, 3

NOTE:

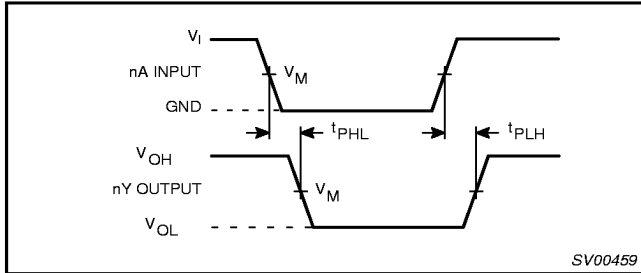
1. These values are at $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$

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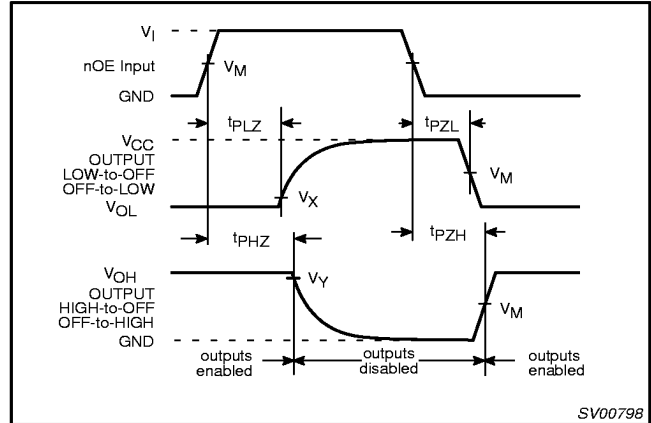
AC WAVEFORMS

$V_M = 50\% V_{CC}$ for 'AC devices; 1.5V for 'ACT devices
 $V_M = 50\% V_{CC}$ for 'AC/'ACT devices
 V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load.



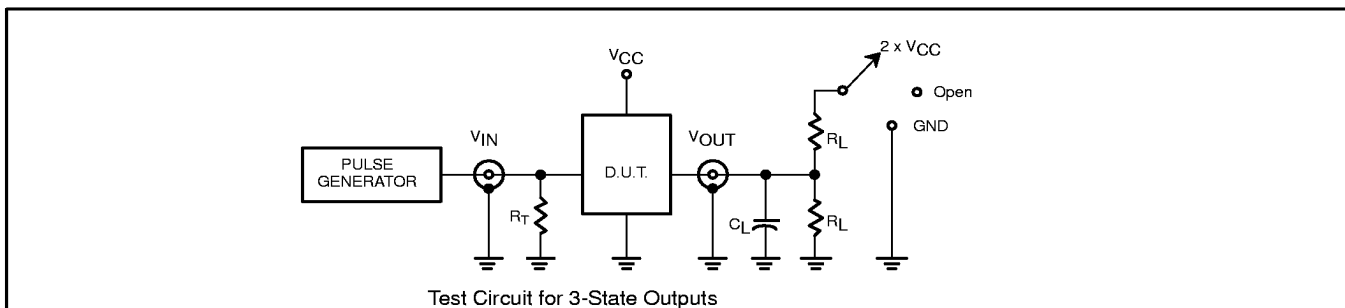
Waveform 1. Input (nA) to output (nY) propagation delays and output transition times.

$V_X = V_{OL} + 0.3V$
 $V_Y = V_{OH} - 0.3V$



Waveform 2. 3-state enable and disable times.

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open

FAMILY	V_{IN} Input Requirements	V_m Input	V_m Output
AC	GND to V_{CC}	$50\% V_{CC}$	$50\% V_{CC}$
ACT	GND to 3.0V	1.5V	$50\% V_{CC}$

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance, see AC characteristics
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SV00451

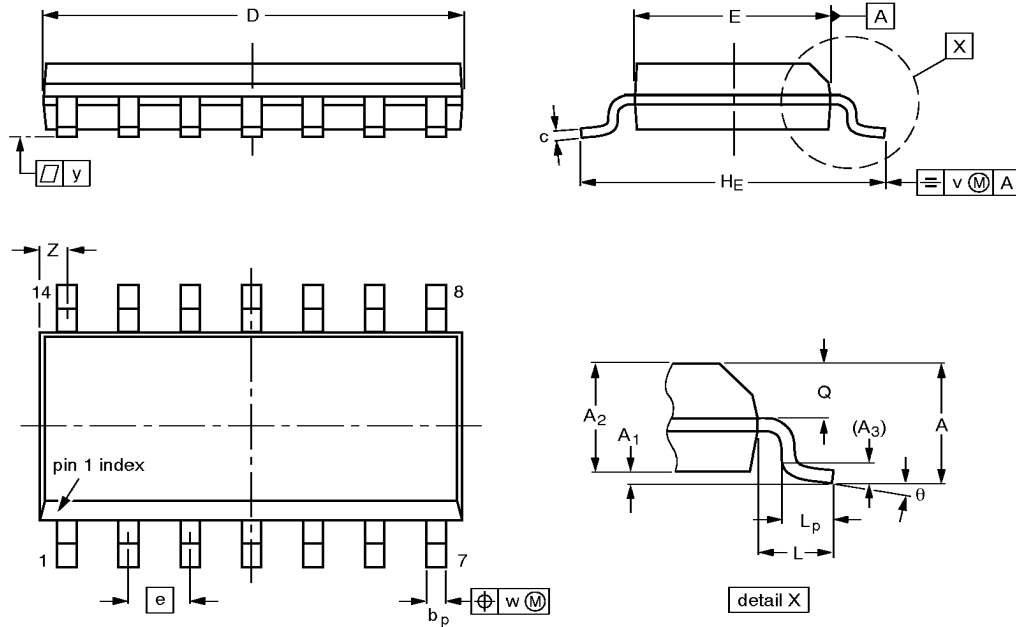
Waveform 3. Load circuitry for switching times.

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

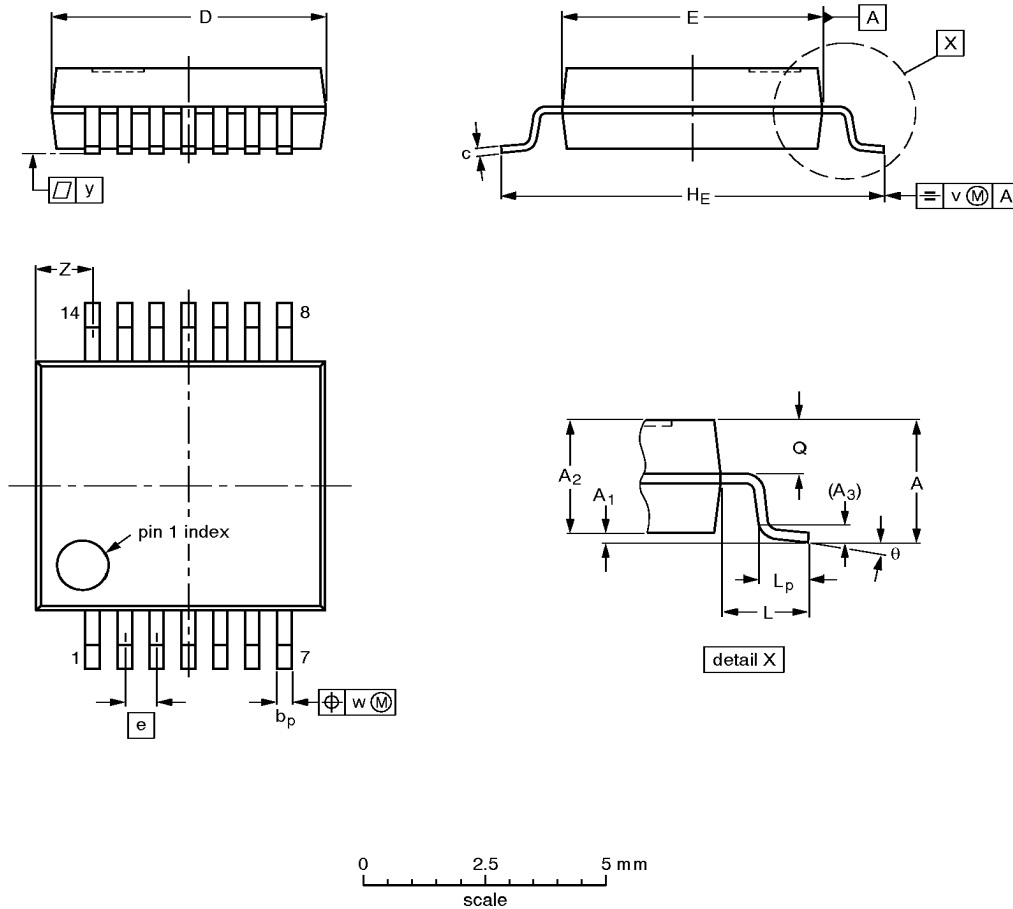
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT108-1	076E06S	MS-012AB			91-08-13 95-01-23

Quad buffer/line driver (3-state)

74AC126
74ACT126

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

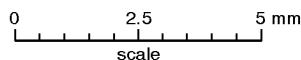
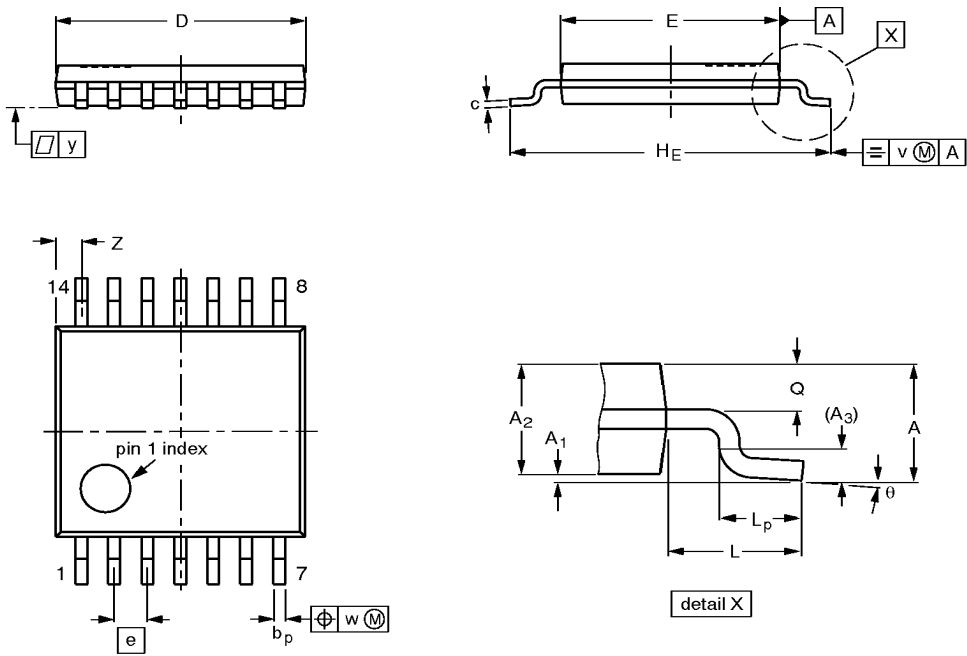
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				95-02-04 96-01-18

Quad buffer/line driver (3-state)

74AC126
74ACT126

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				-94-07-12- 95-04-04