Integrated Mixed-Signal Solutions

C-Major™ Consumer Audio

STEEBAC9460B Evaluation Board User's Guide

(For the evaluation of STAC9460/61/62/63 audio codecs and DACs)

Preliminary Version 1.0
12/6/01

2-9460-EB1-1.0-1201

1. FEATURES

- 6-channel analog output with independent volume control
- Differential stereo analog input
- Dual microphone inputs with independent volume control
- Digital inputs (clock and data signals) can be provided by an external source, using standard I2S interface
- On-board, I2S clock generation
- SPDIF interface to digital audio signal sources (available soon)
- RS-232 serial interface to host computer with user-configurable baud rate

Device	DAC	ADC
STAC9460	6 DACs, 24 Bits	2 ADCs, 24 Bits
STAC9461	6 DACs, 24 Bits	N/A
STAC9462	2 DACs, 24 Bits	2 ADCs, 24 Bits
STAC9463	2 DACs, 24 Bits	N/A

Table 1. Product Comparison Table

2. DESCRIPTION

The STEEBAC9460B evaluation board (for evaluating D-Major consumer audio STAC9460/61/62/63 codecs and DACs) provides a flexible and convenient platform for evaluating the functionality and performance of the STAC9460/61/62/63; 24-bit, 192 kHz consumer audio codecs and DACs. With a full array of 6 channel analog outputs, differential and microphone inputs, and multiple options for standard I2S digital inputs, the STEEBAC9460B evaluation board interfaces easily to the majority of digital audio test equipment, providing convenient options for user application development.

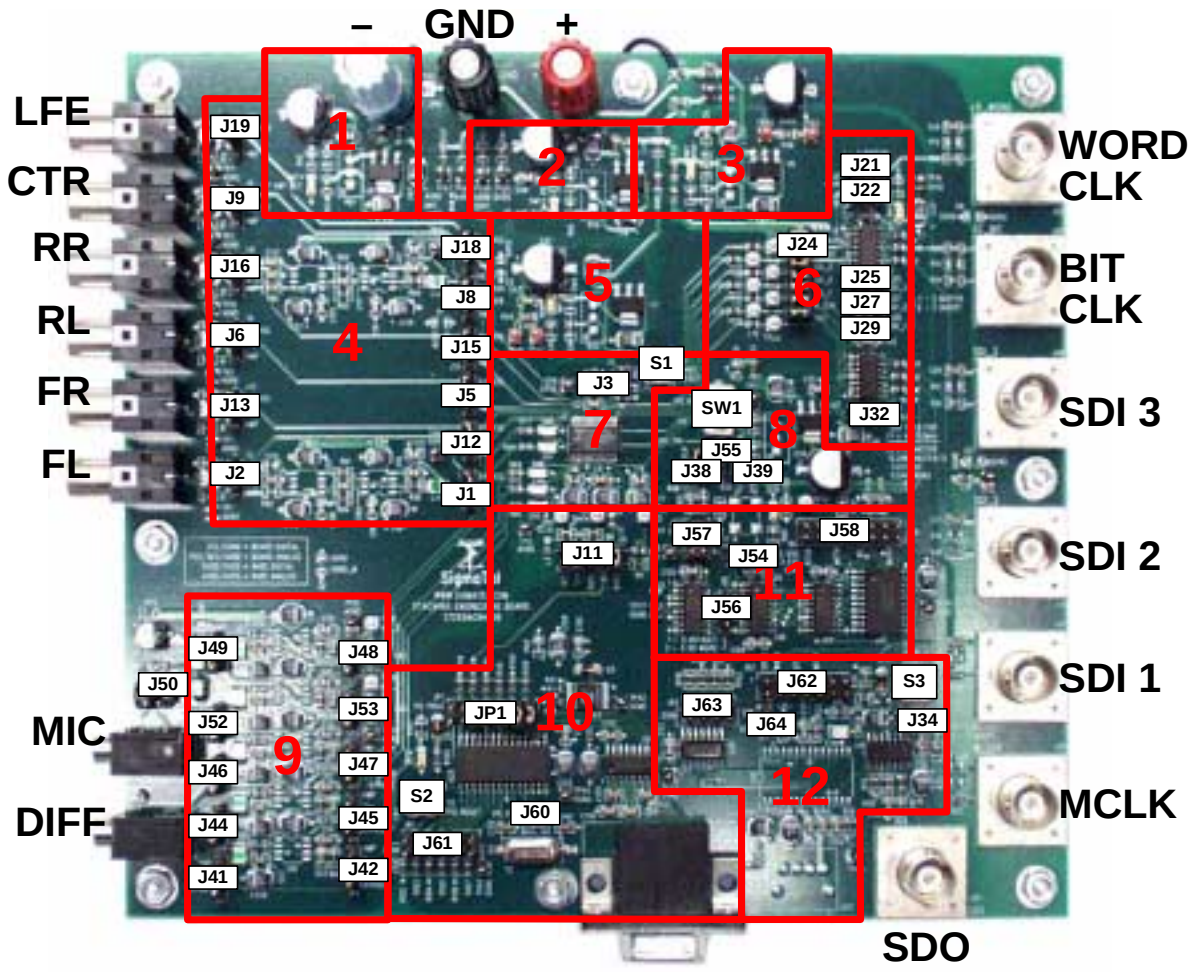
Operation of the STEEBAC9460B Evaluation Board requires a minimal amount of external equipment:

- Analog/digital signal analyzer (Audio Precision Cascade SYS-2522 recommended)
- Digital signal source using standard I2S interface (Audio Precision SIA-2322 adapter recommended)
- PC with available COM port
- Power supply (7V minimum supply needed)
- Operation in Digital Loopback Mode is supported, but will be limited by the ADC dynamic range.

3. SYSTEM OVERVIEW

Note: The STEEBAC9460B evaluation board was designed for engineering evaluation and therefore includes stuffing options for circuits that would not be required in a typical consumer audio application. As a result, this board is not intended to serve as an example reference design, but rather a flexible evaluation vehicle.

Figure 1 illustrates the location of circuits and jumper settings for the STEEBAC9460B evaluation board.



1 : OP AMP NEG. PWR
2 : BOARD ANALOG PWR
3 : CODEC DIGITAL PWR
4 : ANALOG OUTPUT AMPLIFIERS*
5: CODEC ANALOG PWR
6 : DIGITAL INPUT BUFFERS*
7 : STAC9460
8 : BOARD DIGITAL PWR*
9 : ANALOG INPUT AMPLIFIERS*
10 : I2C/RS232 TERMINAL INTERFACE
11 : CLK GENERATION*
12 : SPDIF*

* DENOTES OPTIONAL CIRCUITRY USED FOR EVALUATION/CHARACTERIZATION PURPOSES

Figure 1. STEEBAC9460B Evaluation Board

3.1. Analog I/O

6 analog outputs for front (left and right), surround (left and right), center, and LFE channels are provided through standard RCA connectors. The differential and microphone inputs are provided through standard stereo audio jacks. The microphone input is user-configurable for a biased, mono, or stereo microphone input. (See details on jumper settings for J50 in Table 7, "Description of Jumper/Switch Settings," on page 7 below.)

3.2. Digital I/O and Clocks

3.2.1. External I2S Interface

The STEEBAC9460B evaluation board provides a convenient I2S interface through standard BNC connectors, which allows clock and data signals to be generated by an external source, such as an Audio Precision test system. To use the BNC inputs for I2S inputs, install jumpers as directed in Table 2, "Jumper Settings for BNC I2S Inputs".

JUMPER	CONNECTIONS
J24	Install all jumpers
J58	Remove all jumpers
J62	Remove all jumpers

Table 2. Jumper settings for BNC I2S Inputs

3.2.2. I2S Clock Generation Module

In addition, the board includes a user-configurable clock generation circuit that provides I2S clock and master clock inputs to the STAC9460/61/62/63. To use the clock generation circuit, install jumpers as directed in Table 3, "Jumper Settings for CLK Generataion Circuit".

JUMPER	CONNECTIONS
J24	Install all jumpers
J62	Remove all jumpers
J38	Install jumper
J54	Install jumper 1-2
J56	Install jumper 1-2 for 48 kHz WORD CLK or Install jumper 2-3 for 96 kHZ WORD CLK
J58	Install 1-2 for 48 or 96 kHz WORD CLK Install 5-6 for 3.072 Mhz BIT CLK Install 9-10 for 24.5 Mhz MASTER CLK or Install 11-12 for 12.2 Mhz MASTER CLK Install 13-14 to enable BIT CLK

Table 3. Jumper settings for CLK Generation Circuit

Note: When using the CLK generation circuit, disconnect any BNC connectors providing clock signals.

3.2.3. SPDIF Input Interface

The STEEBAC9460B evaluation board also includes an audio receiver circuit which provides additional flexibility through a standard SPDIF input interface. To use this SPDIF receiver circuit for digital clock and data inputs, install jumpers as described in Table 4.

JUMPER	CONNECTIONS
J55	Install to provide power to receiver circuit
J39	Install to provide power to U4 inverter
J64	Do not install, leave open
J63	Install 1-2, 3-4, 7-8 to set the serial port mode configuration for the CS8414 digital audio receiver. Note: If all jumpers are unpopulated, the CS8414 is held in reset
J52	Install 1-2, 3-4, 5-6, 9-10 to provide SDI_1, WCLK, BIT CLK, and MCLK, respectively, to the STAC9460/61/62/63
J58	Do not install any jumpers This is necessary to prevent any interference from clock signals sourced by the clock generation circuit

Table 4. Jumper settings for SPDIF Receiver Circuit

3.3. Power supply

Power is provided to the STEEBAC9460B evaluation board through three binding posts: GND, +7V, -7V. The +7V supply is separated and regulated down to 5V to provide isolated supply sources to digital and analog circuits on the board. The –7V supply is optional and used only when needed to provide a negative supply to the amplifiers that can be used to boost the analog I/O signals.

4. SERIAL CONTROL PORT (RS-232 INTERFACE)

Configuration and control of the STAC9460/61/62/63 processor on the evaluation board is accomplished through an RS-232 serial connection. A terminal program, such as HyperTerminal or TeraTerm, should be used to communicate over this interface. Jumper settings (JP1) on the board determine the baud rate for the serial connection (see Table 5 for details). Note: The default setting is 1200 baud.

J 1-2	J3-4	J5-6	Baud Rate
ON	ON	ON	1200*
OFF	ON	ON	2400
ON	OFF	ON	4800
OFF	OFF	ON	9600
ON	ON	OFF	19200
OFF	ON	OFF	38400
ON	OFF	OFF	76800
OFF	OFF	OFF	115200

Table 5. RS-232 Serial Interface Baud Rate Jumper Settings (JP1)

The terminal program should be configured with the settings shown in Table 6.

Parameter	Value
Baud rate	1200 (default)
Data	8
Parity	None
Stop Bits	1
Flow Control	Off

Table 6. Terminal Program Configuration

Several functions are available within the serial interface software for configuration and control of the STAC9460/61/62/63:

"**A**": prints the I2C slave device address used by the PIC16F876 to address the STAC9460/61/62/63.

"**D**": dumps the contents of registers 0-A, C, E-14 to the screen. (Registers B and D are not printed because they are reserved.)

"**Rxx**": reads the value of register xx and prints it out to the screen.

"**Wxxyy**": writes value yy into register xx.

STAC9460/61/62/63 register configuration scripts are provided on the CD-ROM included with this evaluation board. These scripts can be used in conjunction with the terminal program to automatically configure the STAC9460/61/62/63 for performance evaluation of the DAC or ADC.

In a typical terminal program, a configuration script can be run automatically by executing a "Send file" or "Transfer file", creating a fast and convenient method for configuring the STAC9460/61/62/63. For example, if using HyperTerminal, execute Transfer, Send Text File, and then choose the desired STAC9460/61/62/63 configuration script. This will execute all register writes contained within the chosen configuration script.

See Section 6, Recommended Test Procedures, for details on the STAC9460/61/62/63 configuration scripts.

5. JUMPER AND SWITCH SETTINGS

(Please refer to the STEEBAC9460B evaluation Board schematics for further details on jumper and switch functionality.)

Jumper	Purpose	Position	Function Selected
JP1	General I2C control	1-2, 3-4, 5-6	Select baud rate for serial interface, see Table 1.0 for details
		7-8	Enable keyboard echo; default is OFF
		9-10	Determines I2C slave address: OFF: addr. = 0x54 ON* addr. = 0x56
		11-12	Not used
		13-14	For PIC16F876 prog. only; *Must remain OFF*
J1, J2	Analog output amp. option	1-2	Amplify front left channel
		2-3*	Bypass amp.
J5, J6	Analog output amp. option	1-2	Amplify front right channel
		2-3*	Bypass amp.
J8, J9	Analog output amp. option	1-2	Amplify center channel
		2-3*	Bypass amp.
J12, J13	Analog output amp. option	1-2	Amplify front right channel
		2-3*	Bypass amp.
J15, J16	Analog output amp. option	1-2	Amplify rear right channel
		2-3*	Bypass amp.
J18, J19	Analog output amp. option	1-2	Amplify LFE channel
		2-3*	Bypass amp.
J3	PIC16F876 reset	OFF*	If On, S2 provides STAC9460/61/62/63 reset simultaneous with PIC reset
J11	I2C control	1-2*	CS high, I2C slave address = 56
		3-4	CS controlled by I2C master
		5-6	CS low, I2C slave address = 54
J21	LR_WORD buffer/invert option	1-2*	Buffer LR_WORD
		3-4	Invert LR_WORD
J22	SC_BIT buffer/invert option	1-2*	Buffer SC_BIT
		3-4	Invert SC_BIT
J24	Signal pass-through for digital I/O	All ON*	*Must remain ON.*
J25	SDI_3 buffer/invert option	1-2*	Buffer SDI_3
		3-4	Invert SDI_3
J27	SDI_2 buffer/invert option	1-2*	Buffer SDI_2
		3-4	Invert SDI_2
J29	SDI_1 buffer/invert option	1-2*	Buffer SDI_1
		3-4	Invert SDI_1
J32	MCLK buffer/invert option	1-2*	Buffer MCLK
		3-4	Invert MCLK
J34	SDO buffer/invert option	1-2*	Buffer SDO
		3-4	Invert SDO
J38	VCC CLK power source	ON*	Provides power to clk gen circuit
J39	SDO Buffer power source	ON*	Provides power to SDO buffer

Table 7. Description of Jumper/Switch Settings

Jumper	Purpose	Position	Function Selected
J41, J42	Differential input amp. option	1-2* 3-4	Bypass amp. Amplify diff. right channel
J44, J45	Differential input amp. option	1-2* 3-4	Bypass amp. Amplify diff. left channel
J46, 47	Differential input amp. option	1-2* 3-4	Bypass amp. Amplify diff. GND
J48, J49	Mic input amp. option	1-2* 3-4	Bypass amp. Amplify mic right channel
J52, J53	Mic input amp. option	1-2* 3-4	Bypass amp. Amplify mic left channel
J50	Mic input config. options	1-3 3-4* 4-6	Provide mic bias Stereo mic Mono mic
J54	Clock input select for CLK gen. circuit	1-2* 3-4	On-board OSC External CLK input
J55	SPDIF power source	OFF*	Provides power to SPDIF circuit
J56	Set value of WORD CLK from CLK. generation circuit	1-2* 3-4	48 kHz WORD CLK 96 kHz WORD CLK
J57	External CLK input for CLK gen. circuit	OFF	Option to provide external clk source to replace on-board 49 Mhz oscillator
J58	Passes thru signals from CLK generation circuit	1-2* 5-6* 9-10* 11-12 13-14*	48 or 96 kHz WORD CLK 3.072 Mhz BIT CLK 24.5 Mhz MASTER CLK 12.2 Mhz MASTER CLK Enable BIT CLK
J60	SigmaTel internal eval. only	N/A	N/A
J61	SigmaTel internal eval. only	OFF*	Must remain OFF
J62, J63, J64	SigmaTel internal eval. only	N/A	
S1	STAC9460/61/62/63 reset	N/A	Toggle provides soft reset
S2	PIC16F876 reset	N/A	Toggle provides soft reset
SW1	PIC16F876 power	ON*	Enables power supply to PIC16F876

Table 7. Description of Jumper/Switch Settings (Continued)

Note: * Denotes default jumper/switch setting

6. RECOMMENDED TEST PROCEDURES

The CD-ROM included with the STEEBAC9460B evaluation board provides standard Audio Precision test procedures and STAC9460/61/62/63 configuration scripts for use in basic ADC and DAC performance measurements.

Figures 2 and 3 illustrate the recommended Audio Precision to STEEBAC9460B evaluation Board connections, and the recommended switch settings for the transmitter module of the SIA-2322, respectively.

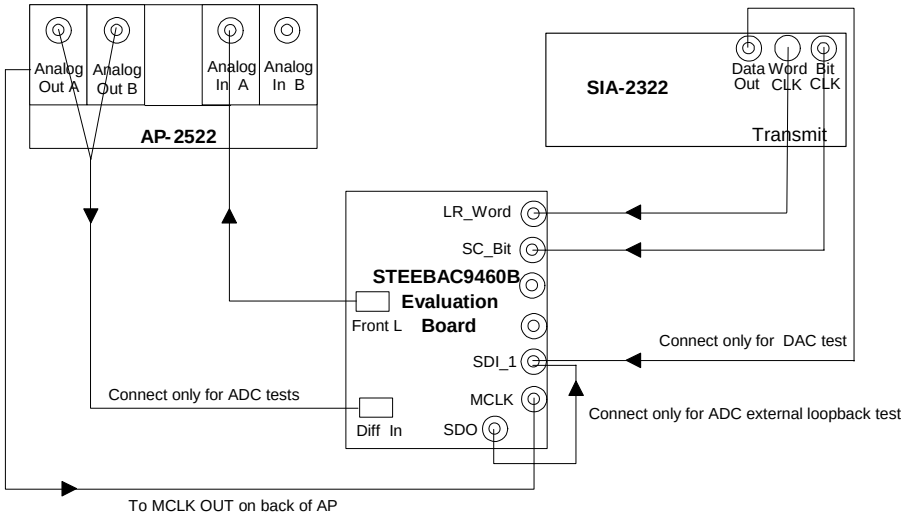


Figure 2. Audio Precision Connections

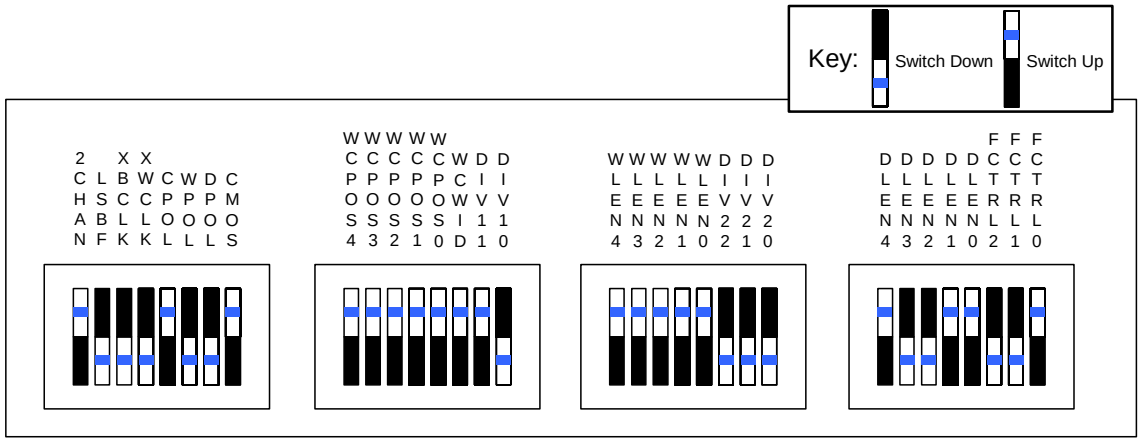


Figure 3. SIA-2322 Transmitter Switch Settings

6.1. DAC performance measurements

I2S digital inputs are provided by the external test system (i.e. the Audio Precision SIA 2322 adapter). Use the 9460_dac.txt script through the serial interface to configure the STAC9460/61/62/63. Use the 9460_DAC_FFT.at2c and 9460_DAC_THDvAMPL_sweep.at2c test procedures on the Audio Precision system to measure DAC performance.

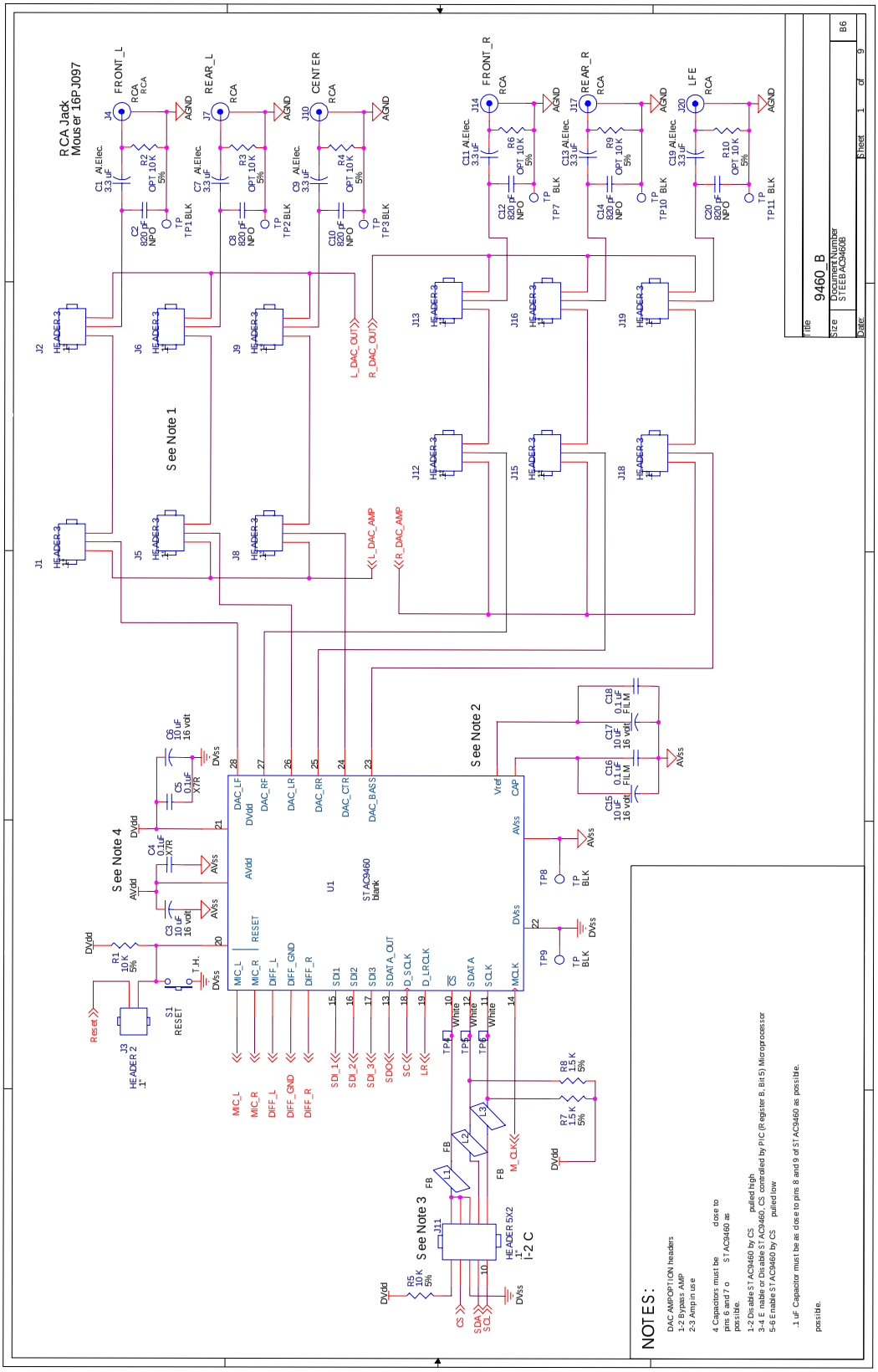
6.2. ADC performance measurements

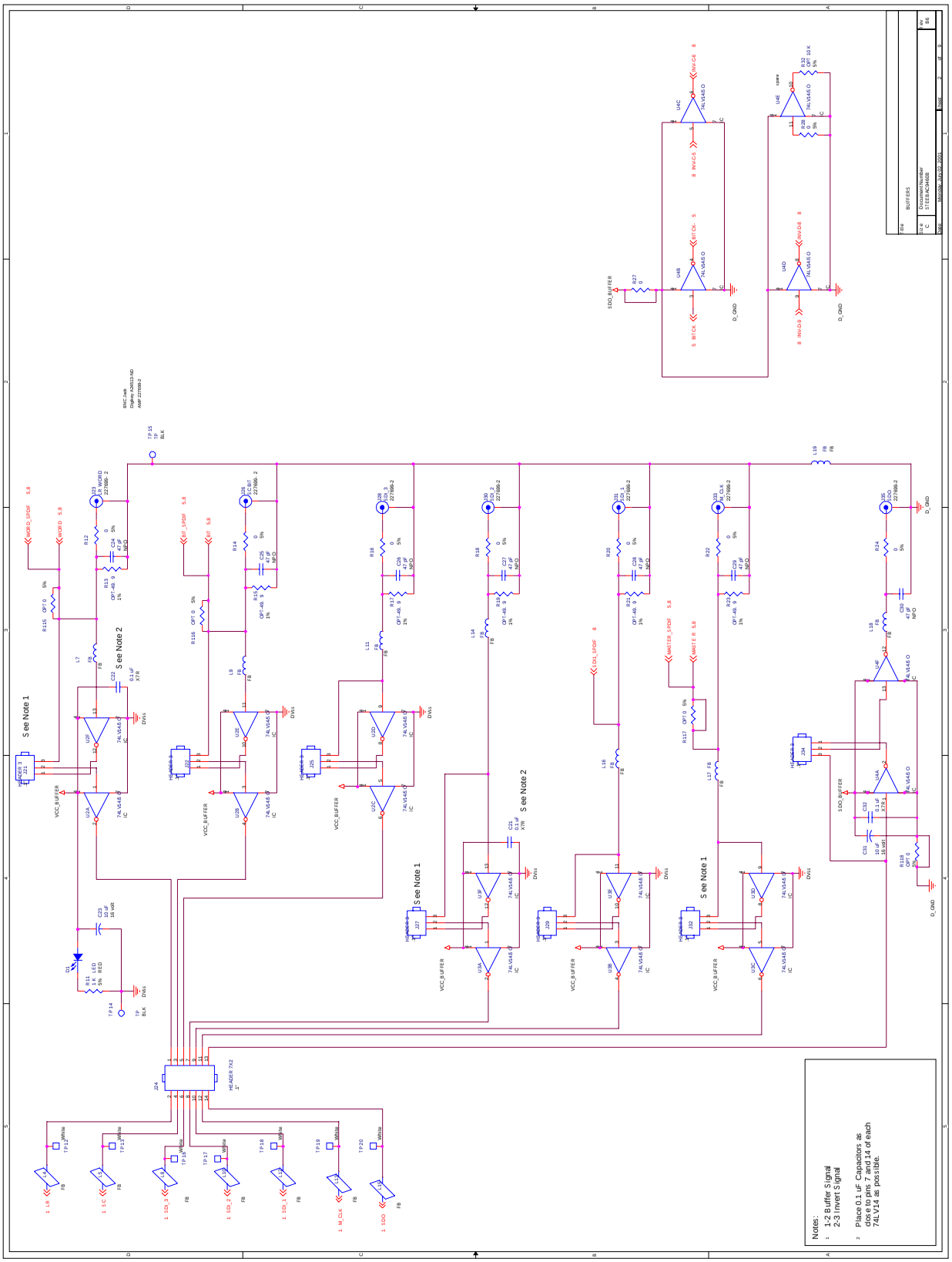
Only STAC9460 and STAC9462 audio codecs contain ADCs. ADC performance measurements can be achieved using either an internal loopback of the signal within the STAC9460/62 or with an external loopback of the signal by connecting SDO to SDI on the evaluation board. (The signal path for an external loopback test will include the DAC.)

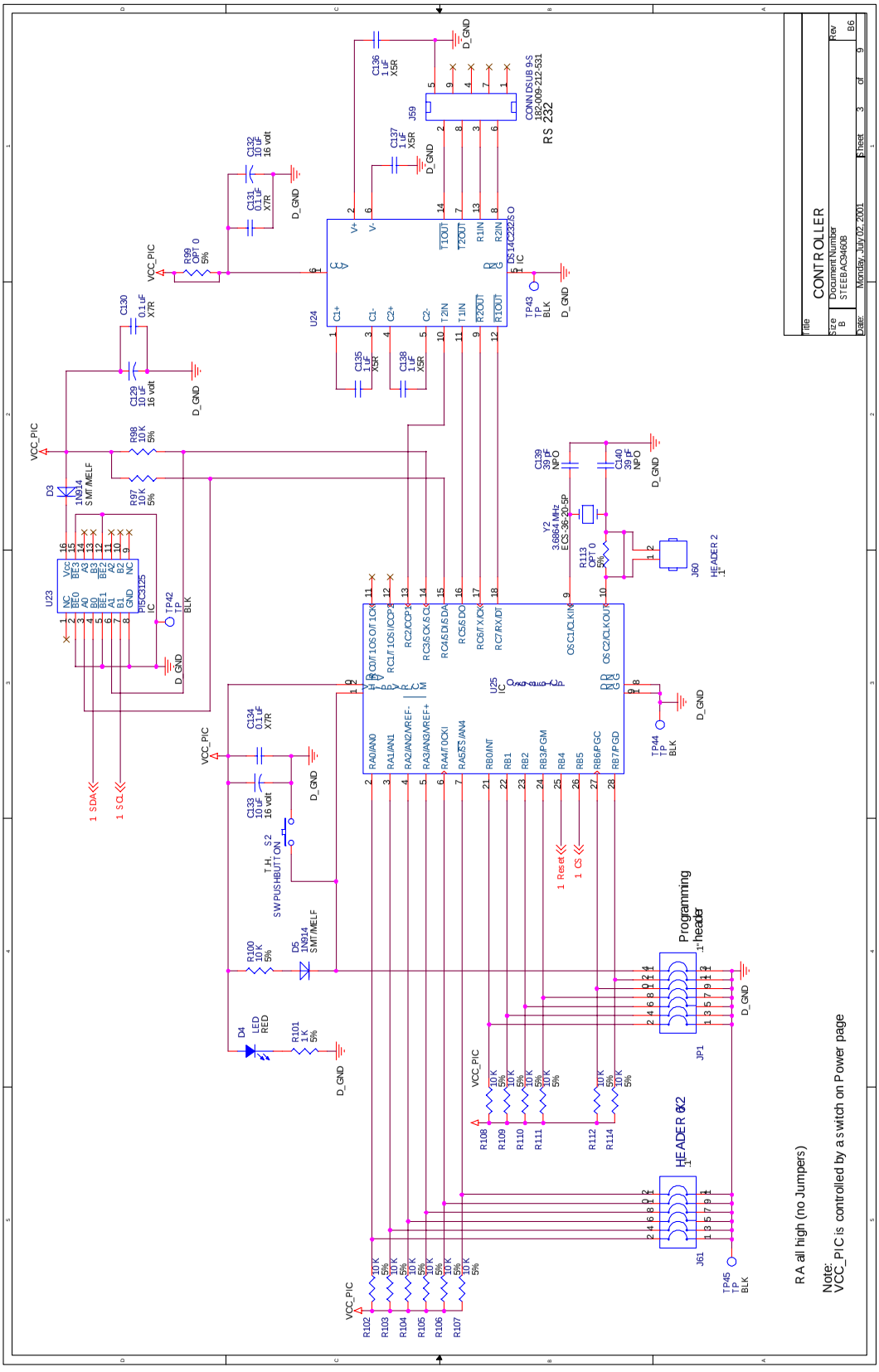
For an internal loopback test, use the 9460_la2_adc_int_loopback.txt configuration script and the 9460_ADC_int_loop_FFT.at2c test procedure. For an external loopback test, use the 9460_la2_adc_ext_loopback.txt configuration script and the 9460_ADC_ext_loop_FFT.at2c test procedure. Use the 9460_ADC_THDvAMPL_sweep.at2c test procedure to perform a sweep of ADC THD+N measurements versus input amplitude, in either internal or external loopback mode.

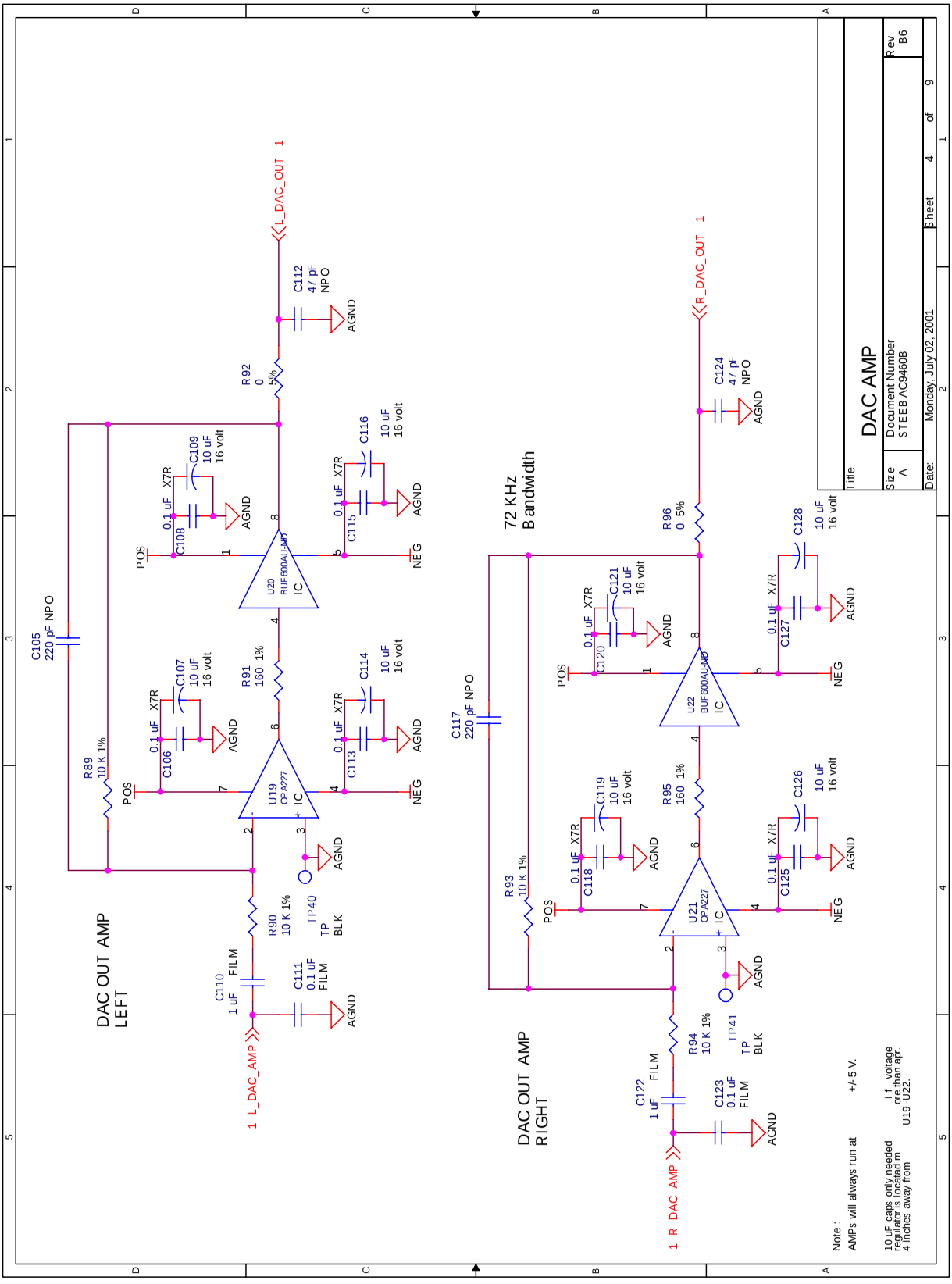
7. EVALUATION BOARD SCHEMATICS

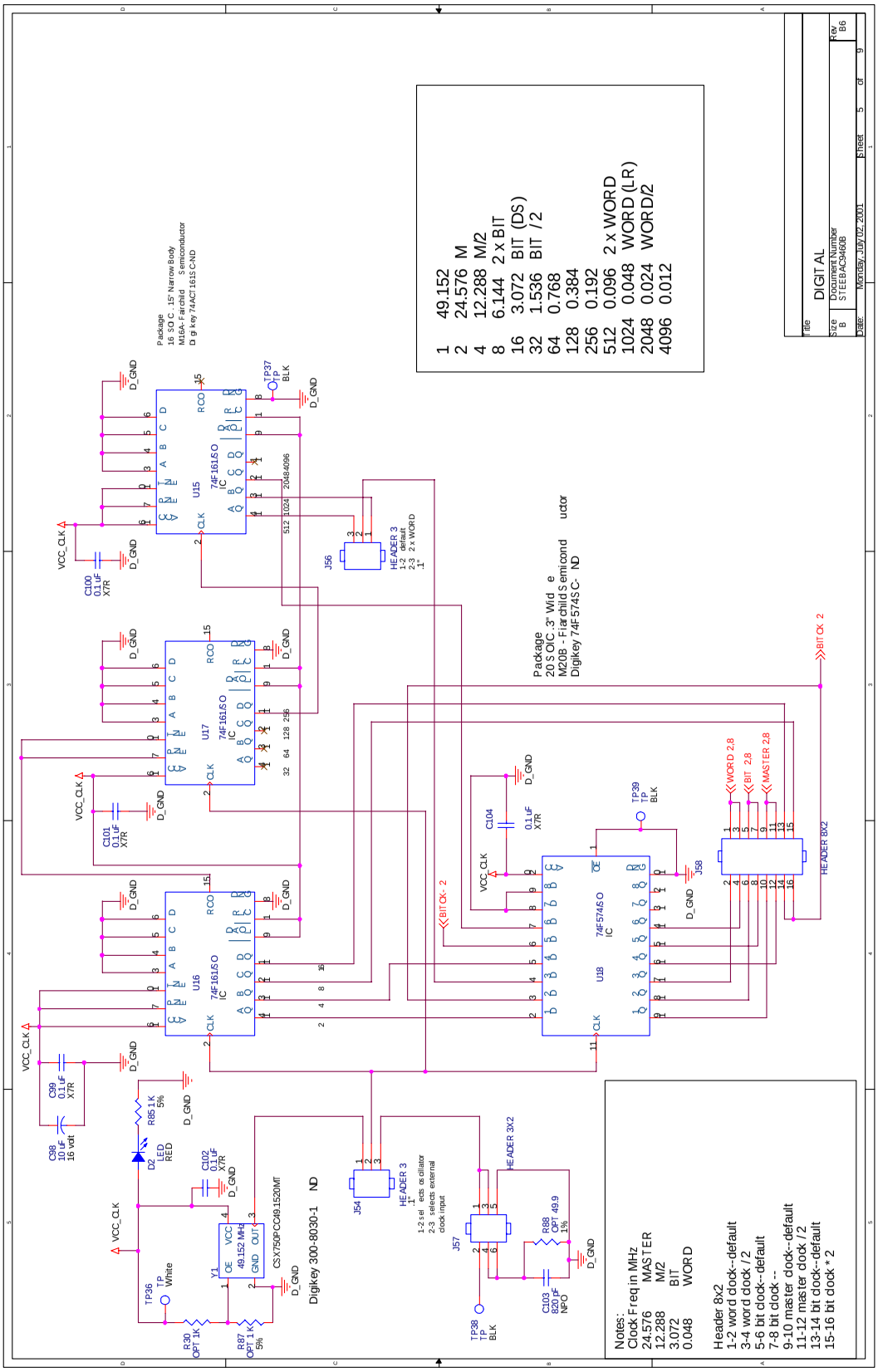
The following pages contain schematics for the STEEBAC9460B evaluation board.

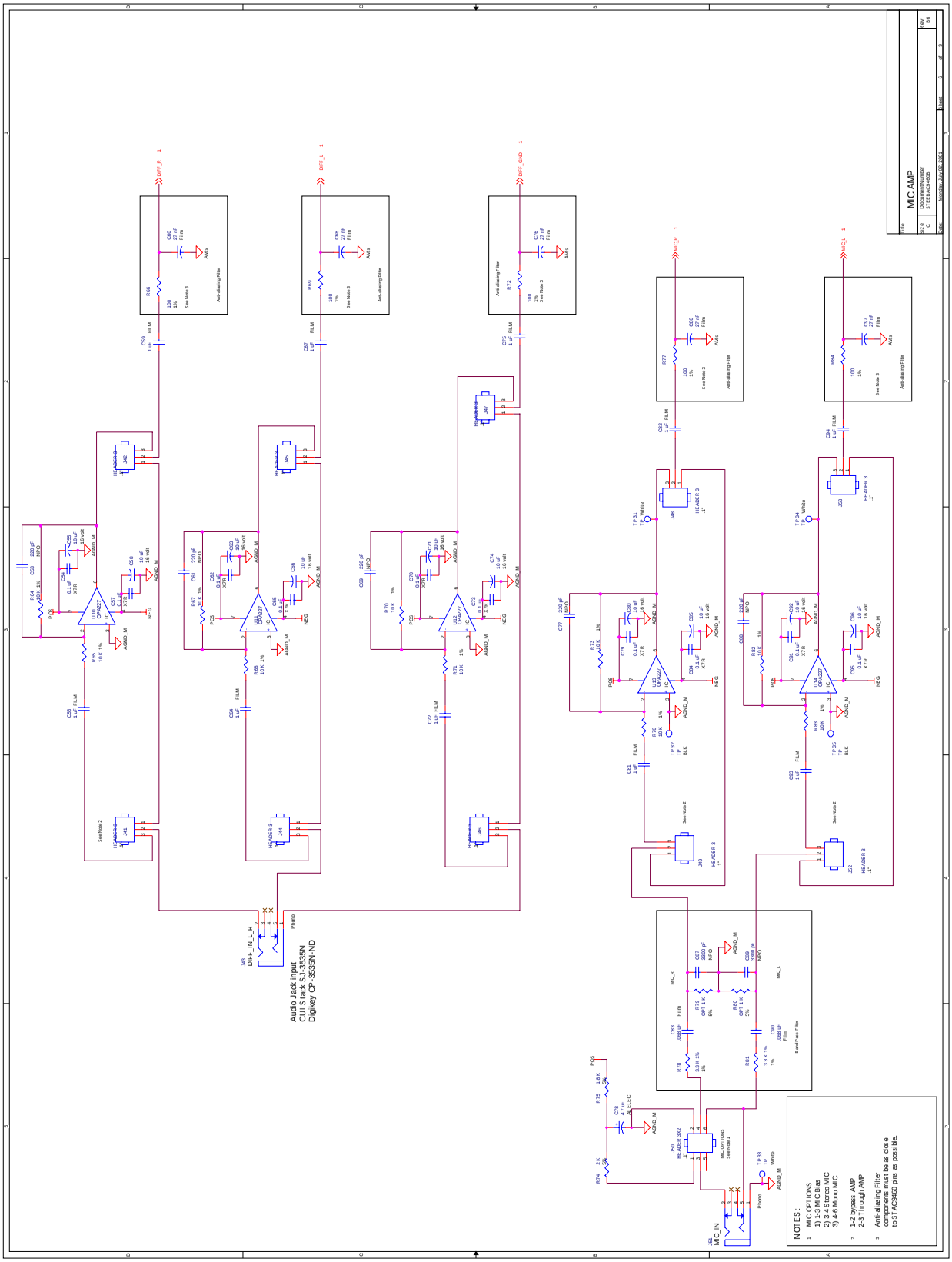

RCA Jack
Mouser 16P-J097
FRONT_L
REAR_L
CENTER
FRONT_R
REAR_R
LFE
See Note 1
See Note 2
See Note 3
See Note 4
U1
STAC9460
NOTES:
DAC AMP OPTION headers
1-2 Bypass AMP
2-3 Amp in use
4 Capacitors must be close to pins 6 and 7 of STAC9460 as possible.
1-2 Disable STAC9460 by CS pulled high
3-4 Enable or Disable STAC9460 CS controlled by PIC (R register 8, Bit 5) Microprocessor
5-6 Enable STAC9460 by CS pulled low
.1 uF Capacitor must be as close to pins 8 and 9 of STAC9460 as possible.
I-2 C

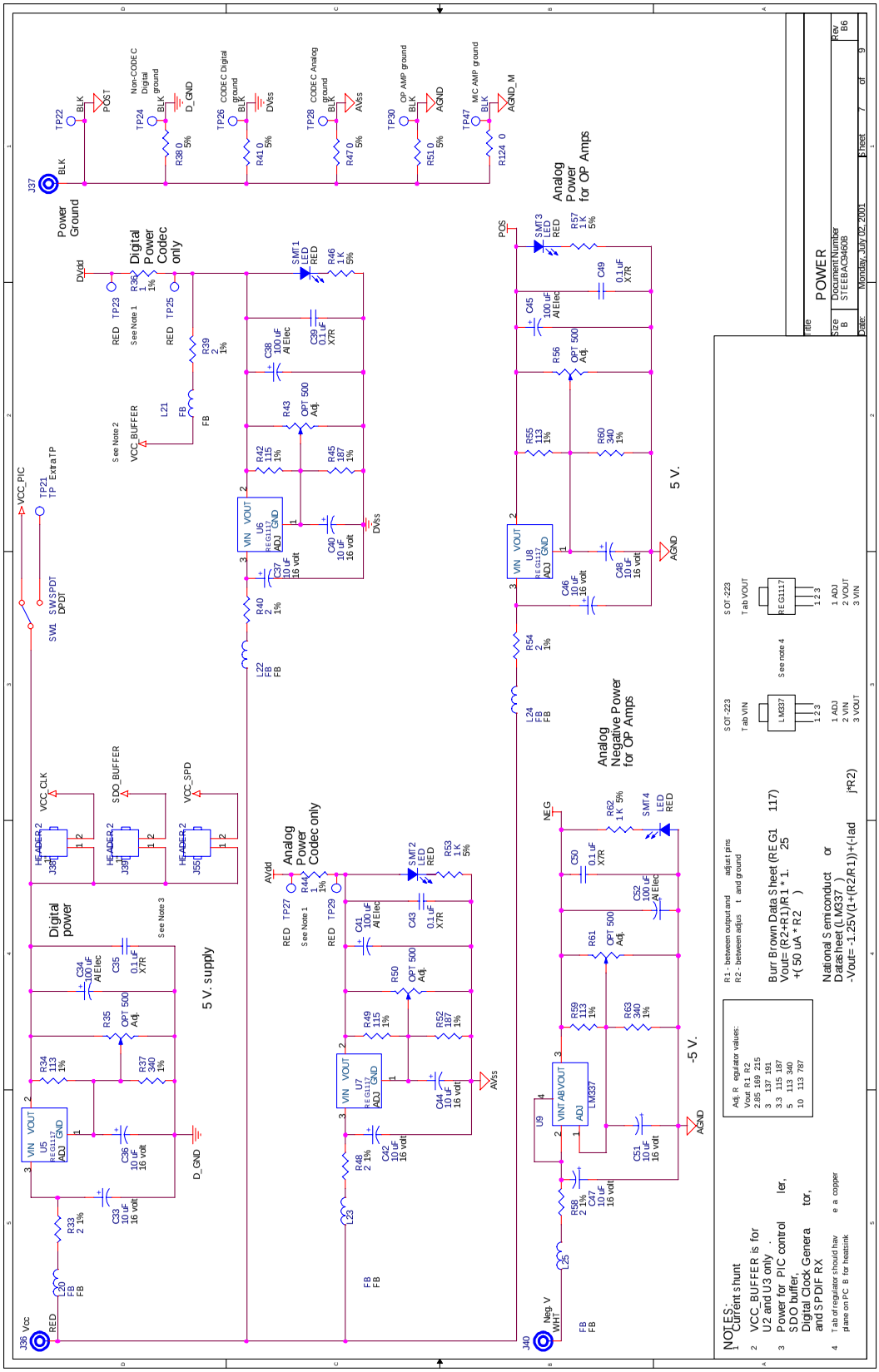

BUFFERS
Notes:
1. 1-2 Buffer Signal
2-3 Invert Signal
2. Place 0.1 uF Capacitors as close to pins 7 and 14 of each 74LV04 as possible.

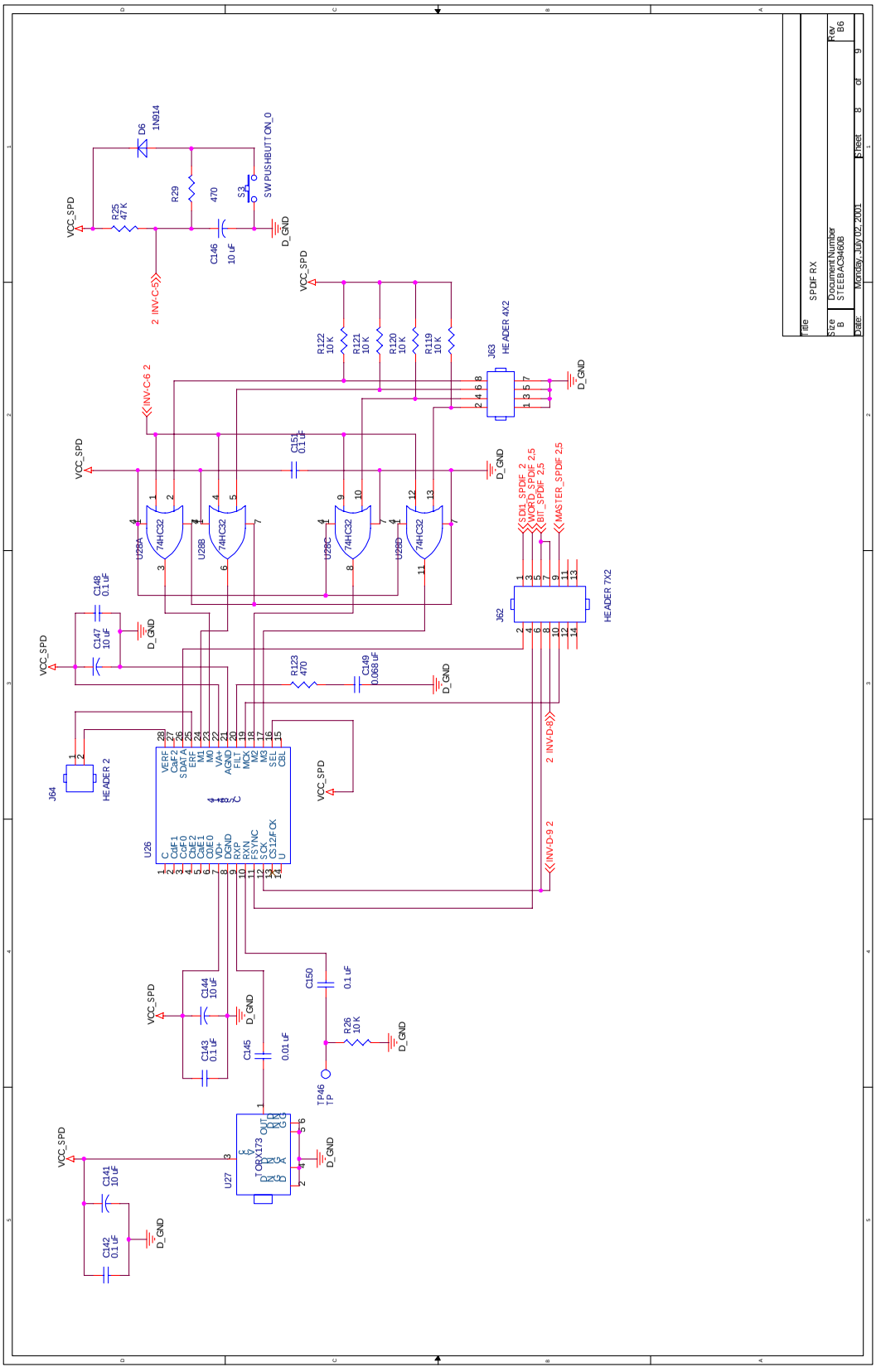

CONTROLLER
RS 232
Programming header
HEADER 8X2
HEADER 2
Note:
VCC_PIC is controlled by a switch on Power page
R A all high (no Jumpers)

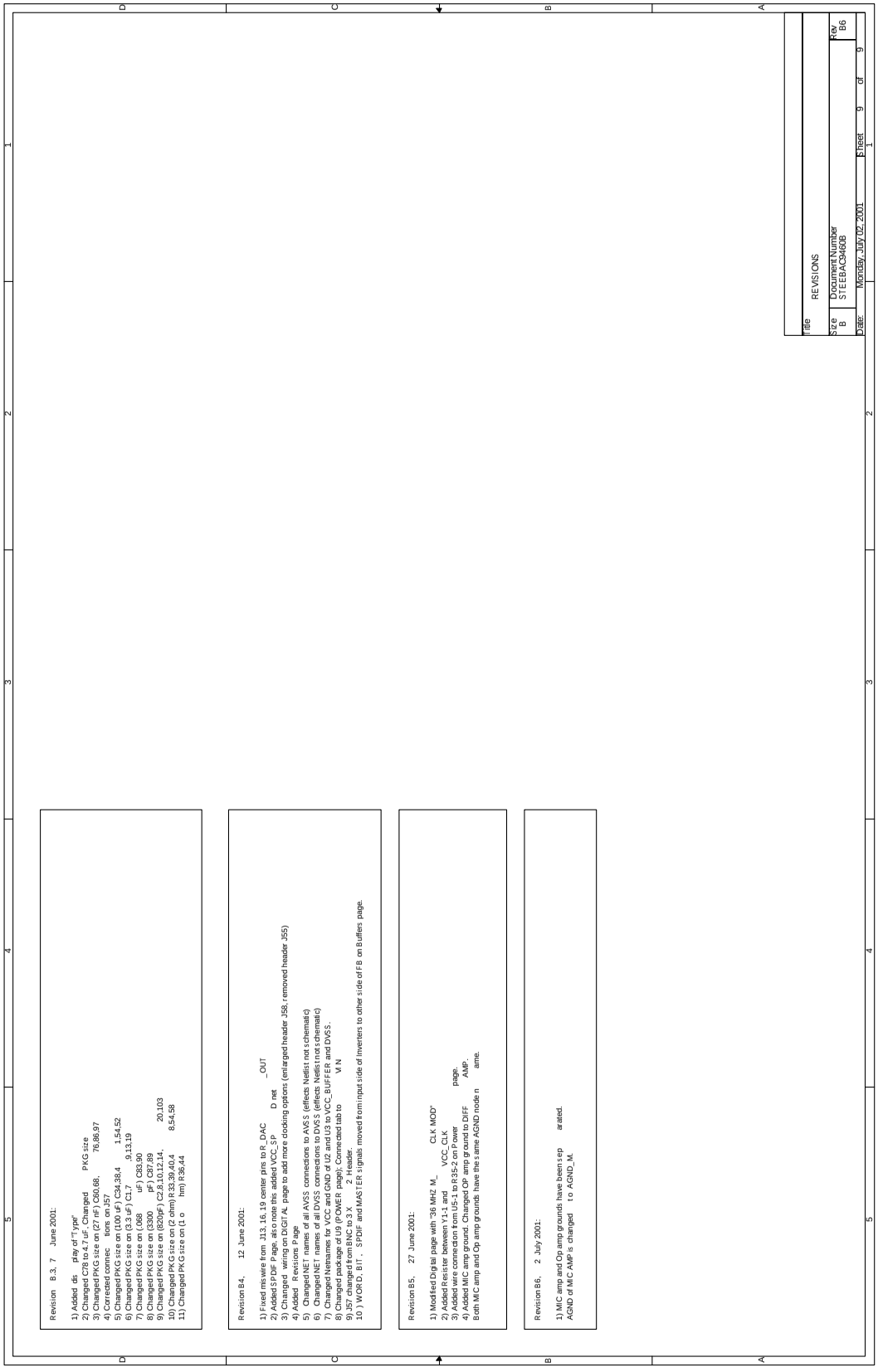

DAC OUT AMP
LEFT
DAC OUT AMP
RIGHT
72 KHz
Bandwidth
L_DAC_OUT 1
R_DAC_OUT 1
1 L_DAC_AMP
1 R_DAC_AMP
U19 OPA227 IC
U20 BUF600AU-MD IC
U21 OPA227 IC
U22 BUF600AU-MD IC
R89 10 K 1%
R90 10 K 1%
R91 160 1%
R92 0 5%
R93 10 K 1%
R94 10 K 1%
R95 160 1%
R96 0 5%
C105 220 pF NPO
C106 0.1 uF X7R
C107 10 uF 16 volt
C108 0.1 uF X7R
C109 10 uF 16 volt
C110 1 uF FILM
C111 0.1 uF FILM
C112 47 pF NPO
C113 0.1 uF X7R
C114 10 uF 16 volt
C115 0.1 uF X7R
C116 10 uF 16 volt
C117 220 pF NPO
C118 0.1 uF X7R
C119 10 uF 16 volt
C120 0.1 uF X7R
C121 10 uF 16 volt
C122 1 uF FILM
C123 0.1 uF FILM
C124 47 pF NPO
C125 0.1 uF X7R
C126 10 uF 16 volt
C127 0.1 uF X7R
C128 10 uF 16 volt
TP40 TP BLK
TP41 TP BLK
POS
NEG
AGND
Title
DAC AMP
Size A
Document Number STEEBAC9460B
Rev B6
Date: Monday, July 02, 2001
Sheet 4 of 9
Note :
AMPs will always run at +/- 5 V.
10 uF caps only needed if voltage regulators located more than 4 inches away from U19 -U22.


1 49.152
2 24.576 M
4 12.288 M/2
8 6.144 2 x BIT
16 3.072 BIT (DS)
32 1.536 BIT /2
64 0.768
128 0.384
256 0.192
512 0.096 2 x WORD
1024 0.048 WORD (LR)
2048 0.024 WORD/2
4096 0.012
Notes:
Clock Freq in MHz
24.576 MASTER
12.288 M/2
3.072 BIT
0.048 WORD
Header 8x2
1-2 word clock--default
3-4 word clock / 2
5-6 bit clock--default
7-8 bit clock --
9-10 master clock--default
11-12 master clock / 2
13-14 bit clock--default
15-16 bit clock * 2
Digikey 300-8030-1 ND
Package
16 SOIC .15" Narrow Body
M16A - Fairchild Semiconductor
Dig Key 74ACT16245CMD
Package
20 SOIC .3" Wide
M20B - Fiarchild Semicond
Digikey 74F574SC- ND
Title
DIGITAL
Size B
Document Number
STEEBAC9460B
Rev B6
Date: Monday, July 02, 2001
Sheet 5 of 9


MIC AMP
NOTES :
MIC OPTIONS
1) 1-3 MIC Bias
2) 3-4 Stereo MIC
3) 4-6 Mono MIC
1-2 bypass AMP
2-3 Through AMP
Anti aliasing Filter
components must be as close
to ST AC9460 pins as possible.
Audio Jack Input
CUI Stack SJ-3535N
Digikey CP-3535N-ND


Power Ground
Digital Power Codec only
Analog Power for OP Amps
Analog Power Codec only
Analog Negative Power for OP Amps
Digital power
5 V. supply
5 V.
-5 V.
VCC_PIC
SW1 SWSPDT DPDT
VCC_CLK
SDO_BUFFER
VCC_SPD
VCC_BUFFER
POS
NEG
AVdd
DVdd
AGND
AVss
DVss
D_GND
Neg V
J36 Vcc
J40
NOTES:
1 Current shunt
2 VCC_BUFFER is for U2 and U3 only .
3 Power for PIC control ler, SDO buffer, Digital Clock Genera tor, and SPDIF RX
4 Tab of regulator should hav e a copper plane on PC B for heatsink
Burr Brown Data Sheet (REG 117)
Vout= (R2+R1)/R1 * 1. 25
+(50 uA * R2)
National S emiconduct or Datasheet (LM337)
-Vout= -1.25V(1+(R2/R1))+(-Iad j*R2)
Title POWER
Size B
Document Number STEEBAC9460B
Rev B5
Date: Monday, July 02, 2001
Sheet 7 of 9


SPDF RX
Document Number
STEEBAC9460B
Monday, July 02, 2001
VCC_SPD
D_GND
HEADER 4X2
HEADER 7X2
HEADER 2
74HC32
TORX173
SWPUSHBUTTON_0
1N914
SDI1_SPDF_2
WORD_SPDF 2.5
BIT_SPDF 2.5
MASTER_SPDF 2.5
2 INV-C-5
INV-C-6 2
2 INV-D-8
INV-D-9 2


Revision 8.3. 7 June 2001:
1) Added dis play of "Type"
2) Changed C78 to 4.7 uF. Changed PKG size
3) Changed PKG size on (27 nF) C60,68, 76,86,97
4) Corrected connec tions on J57
5) Changed PKG size on (100 uF) C34,38,4 1,54,52
6) Changed PKG size on (3.3 uF) C1,7 9,13,19
7) Changed PKG size on (.068 uF) C83,90
8) Changed PKG size on (3300 pF) C87,89
9) Changed PKG size on (820pF) (C2,8,10,12,14, 20,103
10) Changed PKG size on (2 ohm) R 33,39,40,4 8,54,58
11) Changed PKG size on (1 o hm) R36,44
Revision B4, 12 June 2001:
1) Fixed mis wire from U13, 16, 19 center pins to R_DAC _OUT
2) Added SPDIF Page, als o note this added VCC_SP D net
3) Changed wiring on DIGITAL page to add more clocking options (enlarged header J58, removed header J55)
4) Added Revision Page
5) Changed NET names of all AVSS connections to AVSS (effects Netlist not schematic)
6) Changed NET names of all DVSS connections to DVSS (effects Netlist not schematic)
7) Changed Netnames for VCC and GND of U2 and U3 to VCC_BUFFER and DVSS.
8) Changed package of U9 (POWER page); Connected tab to VI N
9) J57 changed from BNC to 3 X 2 Header.
10) WORD, BIT , SPDIF and MASTER signals moved from input side of inverters to other side of FB on Buffers page.
Revision B5, 27 June 2001:
1) Modified Digital page with "36 MHz M_ CLK MOD"
2) Added Resistor between Y1-1 and VCC_CLK
3) Added wire connection from U5-1 to R35-2 on Power page.
4) Added MIC amp ground. Changed OP amp ground to DIFF AMP.
Both MIC amp and Op amp grounds have the s ame AGND node n ame.
Revision B6, 2 July 2001:
1) MIC amp and Op amp grounds have been s ep arated.
AGND of MIC AMP is changed t o AGND_M.
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