

DALLAS

SEMICONDUCTOR

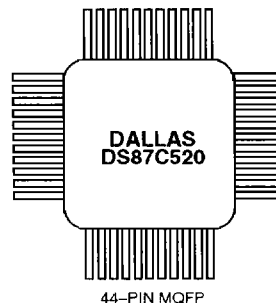
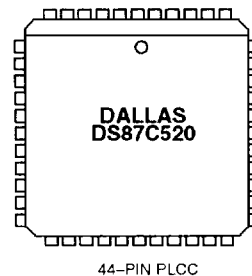
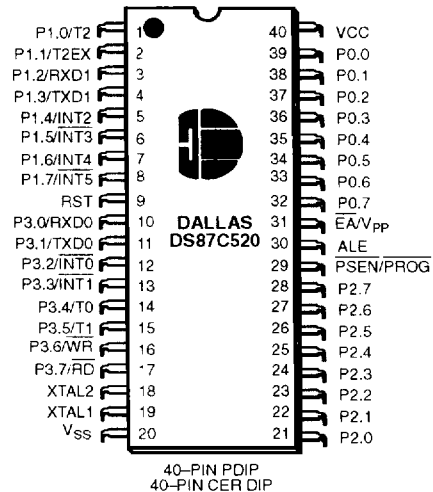
DS87C520

EPROM High-Speed Micro

FEATURES

- 80C52 compatible
 - 8051 pin and instruction set compatible
 - Four 8-bit I/O ports
 - Three 16-bit timer/counters
 - 256 bytes scratchpad RAM
- Large On-chip Memory
 - 16K bytes EPROM (OTP)
 - 1K byte extra on-chip SRAM for MOVX
- ROMSIZE™ Feature
 - Selects effective on-chip ROM size from 0 to 16K
 - Allows access to entire external memory map
 - Dynamically adjustable by software
 - Useful as boot block for external FLASH
- High-Speed Architecture
 - 4 clocks/machine cycle (8051 = 12)
 - Runs DC to 33 MHz clock rates
 - Single-cycle instruction in 121 ns
 - Dual data pointer
 - Optional variable length MOVX to access fast/slow RAM/peripherals
- Power Management Mode
 - Programmable clock source to save power
 - CPU runs from (crystal/64) or (crystal/1024)
 - Provides automatic hardware and software exit
- EMI Reduction Mode disables ALE
- Two full-duplex hardware serial ports
- High integration controller includes:
 - Power-fail reset
 - Early-warning power-fail interrupt
 - Programmable Watchdog timer
- 13 total interrupt sources with 6 external
- Available in 40-pin PDIP, 44-pin PLCC, 44-pin PQFP, and 40-pin windowed CERDIP

PACKAGE OUTLINE



DESCRIPTION

The DS87C520 is a fast 8051 compatible microcontroller. It features a redesigned processor core without wasted clock and memory cycles. As a result, it executes every 8051 instruction between 1.5 and 3 times faster than the original for the same crystal speed. Typical applications will see a speed improvement of 2.5 times using the same code and the same crystal. The DS87C520 offers a maximum crystal speed of 33 MHz, resulting in apparent execution speeds of 82.5 MHz (approximately 2.5X).

The DS87C520 is pin compatible with all three packages of the standard 8051 and includes standard resources such as three timer/counters, serial port, and four 8-bit I/O ports. It features 16K bytes of EPROM with an extra 1K byte of data RAM. Both OTP and windowed packages are available.

Besides greater speed, the micro includes a second full hardware serial port, seven additional interrupts, programmable watchdog timer, brown-out monitor, and

power-fail reset. The DS87C520 also provides dual data pointers (DPTRs) to speed block data memory moves. It also can adjust the speed of MOVX data memory access from two to nine machine cycles for flexibility in selecting external memory and peripherals.

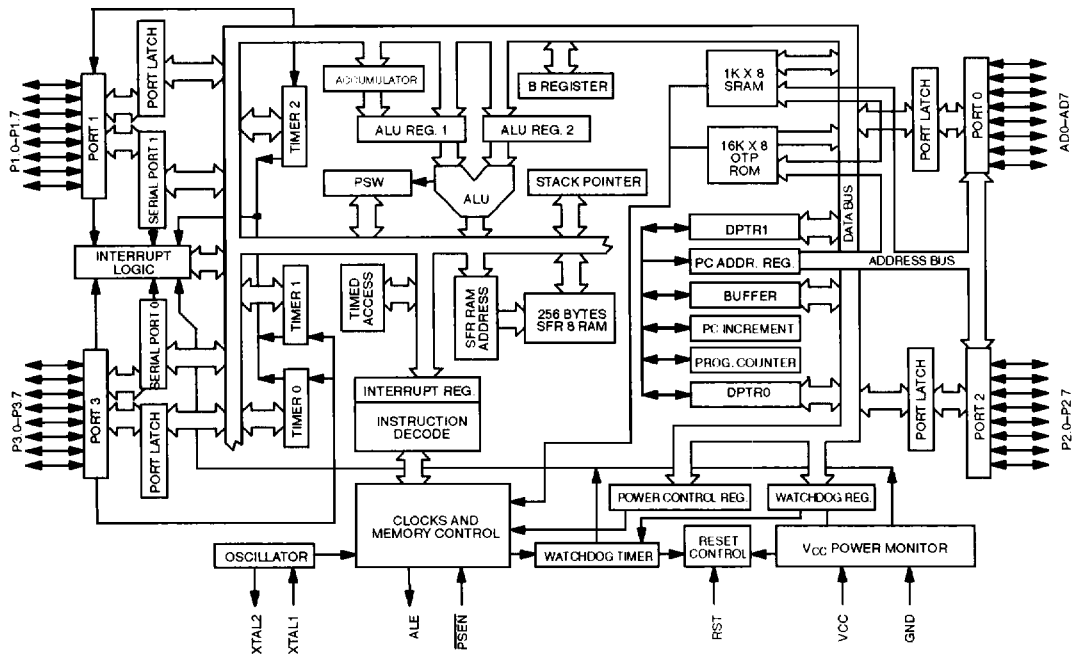
A new Power Management Mode (PMM) is useful for portable applications. This feature allows software to select a lower speed clock as the main time base. While normal operation has a machine cycle rate of 4 clocks per cycle, the PMM runs the processor at 64 or 1024 clocks per cycle. For example, at 12 MHz, standard operation has a machine cycle rate of 3 MHz. In Power Management Mode, software can select either 187.5 KHz or 11.7 KHz machine cycle rate. There is a corresponding reduction in power consumption when the processor runs slower.

The EMI reduction feature allows software to select a reduced emission mode. This disables the ALE signal when it is unneeded.

ORDERING INFORMATION:

PART NUMBER	PACKAGE	MAX. CLOCK SPEED	TEMPERATURE RANGE
DS87C520-MCL	40-pin plastic DIP	33 MHz	0°C to 70°C
DS87C520-QCL	44-pin PLCC	33 MHz	0°C to 70°C
DS87C520-FCL	44-pin PQFP	33 MHz	0°C to 70°C
DS87C520-MNL	40-pin plastic DIP	33 MHz	-40°C to +85°C
DS87C520-QNL	44-pin PLCC	33 MHz	-40°C to +85°C
DS87C520-FNL	44-pin PQFP	33 MHz	-40°C to +85°C
DS87C520-WCL	40-pin windowed CERDIP	33 MHz	0°C to 70°C

DS87C520 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

DIP	PLCC	PQFP	SIGNAL NAME	DESCRIPTION
40	44	38	V _{CC}	V _{CC} – +5V.
20	22, 23, 1	16, 17, 39	GND	GND – Digital circuit ground.
9	10	4	RST	RST – Input. The RST input pin contains a Schmitt voltage input to recognize external active high Reset inputs. The pin also employs an internal pull-down resistor to allow for a combination of wired OR external Reset sources. An RC is not required for power-up, as the DS87C520 provides this function internally.
18 19	20 21	14 15	XTAL2 XTAL1	XTAL1, XTAL2 – The crystal oscillator pins XTAL1 and XTAL2 provide support for parallel resonant, AT cut crystals. XTAL1 acts also as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
29	32	26	PSEN	PSEN – Output. The Program Store Enable output. This signal is commonly connected to optional external ROM memory as a chip enable. PSEN will provide an active low pulse and is driven high when external ROM is not being accessed.

DIP	PLCC	PQFP	SIGNAL NAME	DESCRIPTION																											
30	33	27	ALE	ALE – Output. The Address Latch Enable output functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. ALE is forced high when the DS87C520 is in a Reset condition. ALE can also be disabled using the EMI reduction mode.																											
39 38 37 36 35 34 33 32	43 42 41 40 39 38 37 36	37 36 35 34 33 32 31 30	P0.0 (AD0) P0.1 (AD1) P0.2 (AD2) P0.3 (AD3) P0.4 (AD4) P0.5 (AD5) P0.6 (AD6) P0.7 (AD7)	Port 0 (AD0–7) – I/O. Port 0 is an <i>open-drain</i> 8-bit bi-directional I/O port. As an alternate function Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to a logic 0, the port transitions to a bi-directional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals. When used as a memory bus, the port provides active high drivers. The reset condition of Port 0 is tri-state. Pull-up resistors are required when using Port 0 as an I/O port.																											
1–8	2–9	40–44 1–3	P1.0–P1.7	Port 1 – I/O. Port 1 functions as both an 8-bit bi-directional I/O port and an alternate functional interface for Timer 2 I/O, new External Interrupts, and new Serial Port 1. The reset condition of Port 1 is with all bits at a logic 1. In this state, a weak pull-up holds the port high. This condition also serves as an input state, a weak pull-up holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pull-up. When software writes a 0 to any port pin, the DS87C520 will activate a strong pull-down that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pull-up. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate modes of Port 1 are outlined as follows. <table border="0"> <thead> <tr> <th>Port</th> <th colspan="2">Alternate Function</th> </tr> </thead> <tbody> <tr> <td>P1.0</td> <td>T2</td> <td>External I/O for Timer/Counter 2</td> </tr> <tr> <td>P1.1</td> <td>T2EX</td> <td>Timer/Counter 2 Capture/Reload Trigger</td> </tr> <tr> <td>P1.2</td> <td>RXD1</td> <td>Serial Port 1 Input</td> </tr> <tr> <td>P1.3</td> <td>TXD1</td> <td>Serial Port 1 Output</td> </tr> <tr> <td>P1.4</td> <td>INT2</td> <td>External Interrupt 2 (Positive Edge Detect)</td> </tr> <tr> <td>P1.5</td> <td>INT3</td> <td>External Interrupt 3 (Negative Edge Detect)</td> </tr> <tr> <td>P1.6</td> <td>INT4</td> <td>External Interrupt 4 (Positive Edge Detect)</td> </tr> <tr> <td>P1.7</td> <td>INT5</td> <td>External Interrupt 5 (Negative Edge Detect)</td> </tr> </tbody> </table>	Port	Alternate Function		P1.0	T2	External I/O for Timer/Counter 2	P1.1	T2EX	Timer/Counter 2 Capture/Reload Trigger	P1.2	RXD1	Serial Port 1 Input	P1.3	TXD1	Serial Port 1 Output	P1.4	INT2	External Interrupt 2 (Positive Edge Detect)	P1.5	INT3	External Interrupt 3 (Negative Edge Detect)	P1.6	INT4	External Interrupt 4 (Positive Edge Detect)	P1.7	INT5	External Interrupt 5 (Negative Edge Detect)
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DIP	PLCC	PQFP	SIGNAL NAME	DESCRIPTION																											
21 22 23 24 25 26 27 28	24 25 26 27 28 29 30 31	18 19 20 21 22 23 24 25	P2.0 (A8) P2.1 (A9) P2.2 (A10) P2.3 (A11) P2.4 (A12) P2.5 (A13) P2.6 (A14) P2.7 (A15)	Port 2 (A8–15) – I/O. Port 2 is a bi-directional I/O port. The reset condition of Port 2 is logic high. In this state, a weak pull-up holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pull-up. When software writes a 0 to any port pin, the DS87C520 will activate a strong pull-down that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pull-up. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function Port 2 can function as MSB of the external address bus. This bus can be used to read external ROM and read/write external RAM memory or peripherals.																											
10–17	11, 13–19	5, 7–13	P3.0–P3.7	<p>Port 3 – I/O. Port 3 functions as both an 8-bit bi-directional I/O port and an alternate functional interface for External Interrupts, Serial Port 0, Timer 0 and 1 Inputs, and \overline{RD} and \overline{WR} strobes. The reset condition of Port 3 is with all bits at a logic 1. In this state, a weak pull-up holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pull-up. When software writes a 0 to any port pin, the DS87C520 will activate a strong pull-down that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pull-up. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below.</p> <table border="0"> <thead> <tr> <th>Port</th> <th>Alternate Mode</th> <th></th> </tr> </thead> <tbody> <tr> <td>P3.0</td> <td>RXD0</td> <td>Serial Port 0 Input</td> </tr> <tr> <td>P3.1</td> <td>TXD0</td> <td>Serial Port 0 Output</td> </tr> <tr> <td>P3.2</td> <td>$\overline{INT0}$</td> <td>External Interrupt 0</td> </tr> <tr> <td>P3.3</td> <td>$\overline{INT1}$</td> <td>External Interrupt 1</td> </tr> <tr> <td>P3.4</td> <td>T0</td> <td>Timer 0 External Input</td> </tr> <tr> <td>P3.5</td> <td>T1</td> <td>Timer 1 External Input</td> </tr> <tr> <td>P3.6</td> <td>\overline{WR}</td> <td>External Data Memory Write Strobe</td> </tr> <tr> <td>P3.7</td> <td>\overline{RD}</td> <td>External Data Memory Read Strobe</td> </tr> </tbody> </table>	Port	Alternate Mode		P3.0	RXD0	Serial Port 0 Input	P3.1	TXD0	Serial Port 0 Output	P3.2	$\overline{INT0}$	External Interrupt 0	P3.3	$\overline{INT1}$	External Interrupt 1	P3.4	T0	Timer 0 External Input	P3.5	T1	Timer 1 External Input	P3.6	\overline{WR}	External Data Memory Write Strobe	P3.7	\overline{RD}	External Data Memory Read Strobe
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31	35	29	\overline{EA}	\overline{EA} – Input. Connect to ground to force the DS87C530 to use an external ROM. The internal RAM is still accessible as determined by register settings. Connect \overline{EA} to V_{CC} to use internal ROM.																											
–	12 34	6 28	NC	NC – Reserved. These pins should not be connected. They are reserved for use with future devices in this family.																											

COMPATIBILITY

The DS87C520 is a fully static CMOS 8051 compatible microcontroller designed for high performance. In most cases the DS87C520 can drop into an existing socket for the 80C51, 80C52, 87C51, or 87C52 to improve the operation significantly. While remaining familiar to 8051 family users, it has many new features. In general, software written for existing 8051 based systems works without modification on the DS87C520. The exception is critical timing since the High-Speed Micro performs its instructions much faster than the original for any given crystal selection. The DS87C520 runs the standard 8051 family instruction set and is pin compatible with DIP, PLCC or QFP packages.

The DS87C520 provides three 16-bit timer/counters, full-duplex serial port (2), 256 bytes of direct RAM plus 1K byte of extra MOVX RAM. I/O ports have the same operation as a standard 8051 product. Timers will default to a 12 clock per cycle operation to keep their timing compatible with original 8051 family systems. However, timers are individually programmable to run at the new 4 clocks per cycle if desired. The PCA is not supported.

The DS87C520 provides several new hardware features implemented by new Special Function Registers. A summary of these SFRs is provided below.

PERFORMANCE OVERVIEW

The DS87C520 features a high speed 8051 compatible core. Higher speed comes not just from increasing the clock frequency, but from a newer, more efficient design.

This updated core does not have the dummy memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the DS87C520, the same machine cycle takes four clocks. Thus the fastest instruction, 1 machine cycle, executes three times faster for the same crystal frequency. Note that these are identical instructions. The majority of instructions on the DS87C520 will see the full 3 to 1 speed improvement. Some instructions will get between 1.5 and 2.4 to 1 improvement. All instructions are faster than the original 8051.

The numerical average of all opcodes gives approximately a 2.5 to 1 speed improvement. Improvement of

individual programs will depend on the actual instructions used. Speed sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3 to 1 improved opcodes makes dramatic speed improvements likely for any code. These architecture improvements and 0.8 μm CMOS produce a peak instruction cycle in 121 ns (8.25 MIPs). The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions in the DS87C520 perform the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops can be calculated using a table in the High-Speed Micro User's Guide. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at 4 clocks per increment to take advantage of faster processor operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C520, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles but the "MOV direct, direct" uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C520 usually uses one instruction cycle for each instruction byte. Examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just four clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the High-Speed Micro User's Guide for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS87C520. This allows the DS87C520 to have many new features but use the same instruction set as the 8051. When writing software to use a new feature, an equate statement defines the SFR to an assem-

bler or compiler. This is the only change needed to access the new function. The DS87C520 duplicates the SFRs contained in the standard 80C52. Table 2 shows the register addresses and bit locations. Many are standard 80C52 registers. The High-Speed Micro User's Guide describes all SFRs.

SPECIAL FUNCTION REGISTER LOCATIONS Table 2

* *New functions are in bold*

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
PORT 0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
STK POINTER									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	0	0	0	0	0	0	0	SEL	86h
PCON	SMOD_0	SMOD0	–	–	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/ \bar{T}	M1	M0	GATE	C/ \bar{T}	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	8Eh
PORT1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	IE5	IE4	IE3	IE2	XT/RG	RGMD	RGSL	BGS	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
PORT2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
PORT3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	–	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	C0h
SBUF1	SB7	SB6	SB5	SB4	SB3	SB2	SB1	SB0	C1h
ROMSIZE	–	–	–	–	–	RS2	RS1	RS0	C2h
PMR	CD1	CD0	SWB	–	XTOFF	ALEOFF	DME1	DME0	C4h
STATUS	PIP	HIP	LIP	XTUP	SPTA1	SPRA1	SPTA0	SPRA0	C5h

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T $\bar{2}$	CP/RL $\bar{2}$	C8h
T2MOD	–	–	–	–	–	–	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	SMOD 1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT	D8h
ACC									E0h
EIE	–	–	–	EWDI	EX5	EX4	EX3	EX2	E8h
B									F0h
EIP	–	–	–	PWDI	PX5	PX4	PX3	PX2	F8h

MEMORY RESOURCES

Like the 8051, the DS87C520 uses three memory areas. These are program (ROM), data (RAM), and scratchpad RAM (registers). The DS87C520 contains on-chip quantities of all three areas.

The total memory configuration of the DS87C520 is 16K bytes of ROM, 1K byte of data SRAM and 256 bytes of scratchpad or direct RAM. The 1K byte of data space SRAM is read/write accessible and is memory mapped. This on-chip SRAM is reached by the MOVX instruction. It is not used for executable memory. The scratchpad area is 256 bytes of register mapped RAM and is identical to the RAM found on the 80C52. There is no conflict or overlap among the 256 bytes and the 1K as they use different addressing modes and separate instructions.

PROGRAM MEMORY ACCESS

On-chip ROM begins at address 0000h and is contiguous through 3FFFh (16K). Exceeding the maximum address of on-chip ROM will cause the DS87C520 to access off-chip memory. However, the maximum on-chip decoded address is selectable by software using the ROMSIZE™ feature. Software can cause the DS87C520 to behave like a device with less on-chip memory. This is beneficial when overlapping external memory, such as FLASH, is used.

The maximum memory size is dynamically variable. Thus a portion of memory can be removed from the memory map to access off-chip memory, then restored

to access on-chip memory. In fact, all of the on-chip memory can be removed from the memory map allowing the full 64K memory space to be addressed from off-chip memory. ROM addresses that are larger than the selected maximum are automatically fetched from outside the part via Ports 0 and 2. A depiction of the ROM memory map is shown in Figure 2.

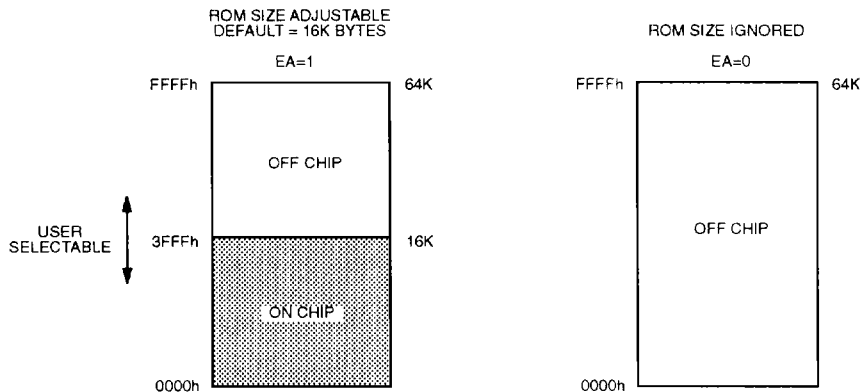
The ROMSIZE register is used to select the maximum on-chip decoded address for ROM. Bits RS2, RS1, RS0 have the following affect.

RS2	RS1	RS0	Maximum on-chip ROM Address
0	0	0	0K
0	0	1	1K
0	1	0	2K
0	1	1	4K
1	0	0	8K
1	0	1	16K (default)
1	1	0	Invalid – reserved
1	1	1	Invalid – reserved

The reset default condition is a maximum on-chip ROM address of 16K bytes. Thus no action is required if this feature is not used. When accessing external program memory, the first 16K bytes would be inaccessible. To select a smaller effective ROM size, software must alter bits RS2–RS0. Altering these bits requires a Timed Access procedure as explained below.

The ROMSIZE register should be manipulated from a safe area in the program memory map. This is a program memory address that will not be affected by the change. For example, do not select a maximum ROM size of 4K from an internal ROM address of 5K. This would cause current address to switch from internal to external and cause invalid operation. Similarly, do not instantly switch from external to internal memory. For example, do not select a maximum internal ROM address of 16K from an external ROM address of 12K.

ROM MEMORY MAP Figure 2



DATA MEMORY ACCESS

Unlike many 8051 derivatives, the DS87C520 contains on-chip data memory. It also contains the standard 256 bytes of RAM accessed by direct instructions. These areas are separate. The MOVX instruction accesses the on-chip data memory. Although physically on-chip, software treats this area as though it was located off-chip. The 1K byte of SRAM is between address 0000h and 03FFh.

Access to the on-chip data RAM is optional under software control. When enabled by software, the data SRAM is between 0000h and 03FFh. Any MOVX instruction that uses this area will go to the on-chip RAM while enabled. MOVX addresses greater than 1K automatically go to external memory through Ports 0 and 2.

Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip ROM access also occurs if the \overline{EA} pin is a logic 0. \overline{EA} overrides all bit settings. The PSEN signal will go active (low) to serve as a chip enable or output enable when Ports 0 and 2 fetch from external ROM.

When disabled, the 1K memory area is transparent to the system memory map. Any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on Ports 0 and 2. This also is the default condition. This default allows the DS87C520 to drop into an existing system that uses these addresses for other hardware and still have full compatibility.

The on-chip data area is software selectable using two bits in the Power Management Register at location C4h. This selection is dynamically programmable. Thus access to the on-chip area becomes transparent to reach off-chip devices at the same addresses. The control bits are DME1 (PMR.1) and DME0 (PMR.0). They have the following operation:

DATA MEMORY ACCESS CONTROL Table 3

DME1	DME0	DATA MEMORY ADDRESS	MEMORY FUNCTION
0	0	0000h – FFFFh	External Data Memory *Default condition
0	1	0000h – 03FFh 0400h – FFFFh	Internal SRAM Data Memory External Data Memory
1	0	Reserved	Reserved
1	1	0000h – 03FFh 0400h – FFFBh FFFC h	Internal SRAM Data Memory Reserved – no external access Read access to the status of lock bits

Notes on the status byte read at FFFCh with DME 1, 0 = 1, 1. Bits 2–0 reflect the programmed status of the security lock bits LB2–LB0. They are individually set to a logic 1 to correspond to a security lock bit that has been programmed. These status bits allow software to verify that the part has been locked before running if desired. The bits are read only.

STRETCH MEMORY CYCLE

The DS87C520 allows software to adjust the speed of off–chip data memory access. The micro is capable of performing the MOVX in as little as two instruction cycles. The on–chip SRAM uses this speed and any MOVX instruction directed internally uses two cycles. However, the time can be stretched for interface to external devices. This allows access to both fast memory and slow memory or peripherals with no glue logic. Even in high–speed systems, it may not be necessary or desirable to perform off–chip data memory access at full speed. In addition, there are a variety of memory mapped peripherals such as LCDs or UARTs that are slow.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. It allows the user to select a Stretch value between zero and seven. A Stretch of zero will result in a two machine cycle MOVX. A Stretch of seven will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to a one resulting in a three cycle MOVX for any external access. There-

fore, off–chip RAM access is not at full speed. This is a convenience to existing designs that may not have fast RAM in place. Internal SRAM access is always at full speed regardless of the Stretch setting. When desiring maximum speed, software should select a Stretch value of zero. When using very slow RAM or peripherals, select a larger Stretch value. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a Stretch value between one and seven causes the microcontroller to Stretch the read/write strobe and all related timing. Also, setup and hold times are increased by one clock when using any Stretch greater than 0. This results in a longer read/write strobe and relaxed interface timing, allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is in the Electrical Specifications. Table 4 shows the resulting strobe widths for each Stretch value. The memory Stretch uses the Clock Control Special Function Register at SFR location 8Eh. The Stretch value is selected using bits CKCON.2–0. In the table, these bits are referred to as M2 through M0. The first Stretch (default) allows the use of common 120 ns RAMs without dramatically lengthening the memory access.

DATA MEMORY CYCLE STRETCH VALUES Table 4

CKCON.2-0			MEMORY CYCLES	RD OR WR STROBE WIDTH IN CLOCKS	STROBE WIDTH TIME @ 33 MHz
M2	M1	M0			
0	0	0	2 (forced internal)	2	60 ns
0	0	1	3 (default external)	4	121 ns
0	1	0	4	8	242 ns
0	1	1	5	12	364 ns
1	0	0	6	16	485 ns
1	0	1	7	20	606 ns
1	1	0	8	24	727 ns
1	1	1	9	28	848 ns

DUAL DATA POINTER

The timing of block moves of data memory is faster using the DS87C520 Dual Data Pointer (DPTR). The standard 8051 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the DS87C520, this data pointer is called DPTR 0, located at SFR addresses 82h and 83h. These are the original locations. Using DPTR0 requires no modification of standard code. The new DPTR at SFR 84h and 85h is called DPTR1. The DPTR Select bit (DPS) chooses the active pointer. Its location is the lsb of the SFR location 86h. No other bits in register 86h have any effect and are 0. The user switches between data pointers by toggling the lsb of register 86h. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore it takes only one instruction to switch from a source to a destination address. Using the Dual Data Pointer saves code from needing to save source and destination addresses when doing a block move. The software simply switches between DPTR0 and 1 once software loads them. The relevant register locations are as follows:

DPL	82h	Low byte original DPTR
DPH	83h	High byte original DPTR
DPL1	84h	Low byte new DPTR
DPH1	85h	High byte new DPTR
DPS	86h	DPTR Select (lsb)

POWER MANAGEMENT

Along with the standard IDLE and power down (STOP) modes of the standard 80C52, the DS87C520 provides a new Power Management Mode. This mode allows the processor to continue functioning, yet to save power

compared with full operation. The DS87C520 also features several enhancements to STOP mode that make it more useful.

POWER MANAGEMENT MODE (PMM)

Power Management Mode offers a complete scheme of reduced internal clock speeds that allow the CPU to run software but to use substantially less power. During default operation, the DS87C520 uses four clocks per machine cycle. Thus the instruction cycle rate is Clock/4. At 33 MHz crystal speed, the instruction cycle speed is 8.25 MHz (33/4). In PMM, the microcontroller continues to operate but uses an internally divided version of the clock source. This creates a lower power state without external components. It offers a choice of two reduced instruction cycle speeds (and two clock sources—discussed below). The speeds are (Clock/64) and (Clock/1024).

Software is the only mechanism to invoke the PMM. Table 5 illustrates the instruction cycle rate in PMM for several common crystal frequencies. Since power consumption is a direct function of operating speed, PMM 1 eliminates most of the power consumption while still allowing a reasonable speed of processing. PMM 2 runs very slow and provides the lowest power consumption without stopping the CPU. This is illustrated in Table 6. Note that PMM provides a lower power condition than IDLE mode. This is because in IDLE, all clocked functions such as timers run at a rate of crystal divided by 4. Since wake-up from PMM is as fast as or faster than from IDLE and PMM allows the CPU to operate (even if doing NOPs), there is little reason to use IDLE in new designs.

INSTRUCTION CYCLE RATE Table 5

CRYSTAL SPEED	FULL OPERATION (4 CLOCKS)	PMM 1 (64 CLOCKS)	PMM 2 (1024 CLOCKS)
1.8432 MHz	460.8 KHz	28.8 KHz	1.8 KHz
11.0592 MHz	2.765 MHz	172.8 KHz	10.8 KHz
22 MHz	5.53 MHz	345.6 KHz	21.6 KHz
25 MHz	6.25 MHz	390.6 KHz	24.4 KHz
33 MHz	8.25 MHz	515.6 KHz	32.2 KHz

OPERATING CURRENT ESTIMATES IN PMM Table 6

CRYSTAL SPEED	FULL OPERATION (4 CLOCKS)	PMM 1 (64 CLOCKS)	PMM 2 (1024 CLOCKS)
1.8432 MHz	3.1 mA	1.2 mA	1.0 mA
3.57 MHz	5.3 mA	1.6 mA	1.1 mA
11.0592 MHz	15.5 mA	4.8 mA	4.0 mA
16 MHz	21 mA	7.1 mA	6.0 mA
22 MHz	25.5 mA	8.3 mA	6.5 mA
25 MHz	31 mA	9.7 mA	8.0 mA
33 MHz	36 mA	12.0 mA	10.0 mA

CRYSTALESS PMM

A major component of power consumption in PMM is the crystal amplifier circuit. The DS87C520 allows the user to switch CPU operation to an internal ring oscillator and turn off the crystal amplifier. The CPU would then have a clock source of approximately 4 MHz, divided by either 4, 64, or 1024. The ring is not accurate so software can not perform precision timing. However, this mode allows an additional saving of between 0.5 and 6.0 mA depending on the actual crystal frequency. While this saving is of little use when running at 4 clocks per instruction cycle, it makes a major contribution when running in PMM1 or PMM2.

PMM OPERATION

Software invokes the PMM by setting the appropriate bits in the SFR area. The basic choices are divider speed and clock source. There are three speeds (4, 64, and 1024) and two clock sources (crystal and ring). Both the decisions and the controls are separate. Software will typically select the clock speed first. Then, it will perform the switch to ring operation if desired. Lastly, software can disable the crystal amplifier if desired.

There are two ways of exiting PMM. Software can remove the condition by reversing the procedure that invoked PMM or hardware can (optionally) remove it. To resume operation at a divide by 4 rate under software control, simply select 4 clocks per cycle, then crystal based operation if relevant. When disabling the crystal as the time base in favor of the ring oscillator, there are timing restrictions associated with restarting the crystal operation. Details are described below.

There are three registers containing bits that are concerned with PMM functions. They are Power Management Register (PMR; C4h), Status (STATUS; C5h), and External Interrupt Flag (EXIF; 91h)

Clock Divider

Software can select the instruction cycle rate by selecting bits CD1 (PMR.7) and CD0 (PMR.6) as follows:

CD1	CD0	Cycle rate
0	0	Reserved
0	1	4 clocks (default)
1	0	64 clocks
1	1	1024 clocks

The selection of instruction cycle rate will take effect after a delay of one instruction cycle. Note that the clock divider choice applies to all functions including timers. Since baud rates are altered, it will be difficult to conduct serial communication while in PMM. There are minor restrictions on accessing the clock selection bits. The processor must be running in a 4 clock state to select either 64 (PMM1) or 1024 (PMM2) clocks. This means software cannot go directly from PMM1 to PMM2 or visa versa. It must return to a 4 clock rate first.

Switchback

To return to a 4 clock rate from PMM, software can simply select the CD1 and CD0 clock control bits to the 4 clocks per cycle state. However, the DS87C520 provides several hardware alternatives for automatic Switchback. If Switchback is enabled, then the DS87C520 will automatically return to a 4 clock per cycle speed when an interrupt occurs from an enabled, valid external interrupt source. A Switchback will also occur when a UART detects the beginning of a serial start bit if the serial receiver is enabled. Note the beginning of a start bit does not generate an interrupt; this occurs on reception of a complete serial word. The automatic Switchback on detection of a start bit allows hardware to correct baud rates in time for a proper serial reception. A switchback will also occur when a byte is written to the SBUF SFR for transmission.

Switchback is enabled by setting the SWB bit (PMR.5) to a 1 in software. For an external interrupt, Switchback will occur only if the interrupt source could really generate the interrupt. For example, if $\overline{INT0}$ is enabled but has a low priority setting, then Switchback will not occur on $\overline{INT0}$ if the CPU is servicing a high priority interrupt. A serial Switchback will occur only if the serial receiver function is enabled (REN=1), or if the SBUF register is written to.

When SWB=1, the user software will not be able to select a reduced clock mode if the UART is active. For example, the processor will prohibit the PMM by not allowing a write to CD1 and CD0 if a serial start bit arrived and SWB=1. Since the reception of a serial start bit or an interrupt priority lockout is normally undetectable by software in an 8051, the Status register features several new flags that are useful. These are described below.

Status

Information in the Status register assists decisions about switching into PMM. This register contains information about the level of active interrupts and the activity on the serial ports.

The DS87C520 supports three levels of interrupt priority. These levels are Power-fail, High, and Low. Bits STATUS.7–5 indicate the service status of each level. If PIP (Power-fail Interrupt Priority; STATUS.7) is a 1, then the processor is servicing this level. If either HIP (High Interrupt Priority; STATUS.6) or LIP (Low Interrupt Priority; STATUS.5) is high, then the corresponding level is in service.

Software should not rely on a lower priority level interrupt source to remove PMM (Switchback) when a higher level is in service. Check the current priority service level before entering PMM. If the current service level locks out a desired Switchback source, then it would be advisable to wait until this condition clears before entering PMM.

Alternately, software can prevent an undesired exit from PMM by entering a low priority interrupt service level before entering PMM. This will prevent other low priority interrupts from causing a Switchback.

Status also contains information about the state of the serial ports. Serial Port Zero Receive Activity (SPRAO; STATUS.0) indicates a serial word is being received on Serial Port 0 when this bit is set to a 1. Serial Port Zero Transmit Activity (SPTAO; STATUS.1) indicates that the serial port is still shifting out a serial transmission. STATUS.2 and STATUS.3 provide the same information for Serial Port 1, respectively. While one of these bits is set, hardware prohibits software from entering PMM (CD1 and CD0 are write protected) since this would corrupt the corresponding serial transmissions.

Crystal/Ring Operation

The DS87C520 allows software to choose the clock source as an independent selection from the instruction cycle rate. The user can select crystal-based or ring oscillator-based operation under software control. Power-on reset default is the crystal (or external clock) source. The ring may save power depending on the actual crystal speed. To save still more power, software can then disable the crystal amplifier. This process requires two steps. Reversing the process also requires two steps.

The XT/\overline{RG} bit (EXIF.3) selects the crystal or ring as the clock source. Setting $XT/\overline{RG}=1$ selects the crystal. Setting $XT/\overline{RG}=0$ selects the ring. The RGMD (EXIF.2) bit serves as a status bit by indicating the active clock source. RGMD=0 indicates the CPU is running from the crystal. RGMD=1 indicates it is running from the ring. When operating from the ring, disable the crystal amplifier by setting the XTOFF bit (PMR.3) to a 1. This can only be done when $XT/\overline{RG}=0$.

When changing the clock source, the selection will take effect after a one instruction cycle delay. This applies to changes from crystal to ring and vice versa. However, this assumes that the crystal amplifier is running. In most cases, when the ring is active, software previously disabled the crystal to save power. If ring operation is being used and the system must switch to crystal operation, the crystal must first be enabled. Set the XTOFF bit to a 0. At this time, the crystal oscillation will begin. The DS87C520 then provides a warm-up delay to make certain that the frequency is stable. Hardware will set the XTUP bit (STATUS.4) to a 1 when the crystal is ready for

use. Then software should write XT/\overline{RG} to a 1 to begin operating from the crystal. Hardware prevents writing XT/\overline{RG} to a 1 before XTUP=1. The delay between XTOFF=0 and XTUP=1 will be 65,536 crystal clocks in addition to the crystal cycle startup time.

Switchback has no effect on the clock source. If software selects a reduced clock divider and enables the ring, a Switchback will only restore the divider speed. The ring will remain as the time base until altered by software. If there is serial activity, Switchback usually occurs with enough time to create proper baud rates. This is not true if the crystal is off and the CPU is running from the ring. If sending a serial character that wakes the system from crystaless PMM, then it should be a dummy character of no importance with a subsequent delay for crystal startup.

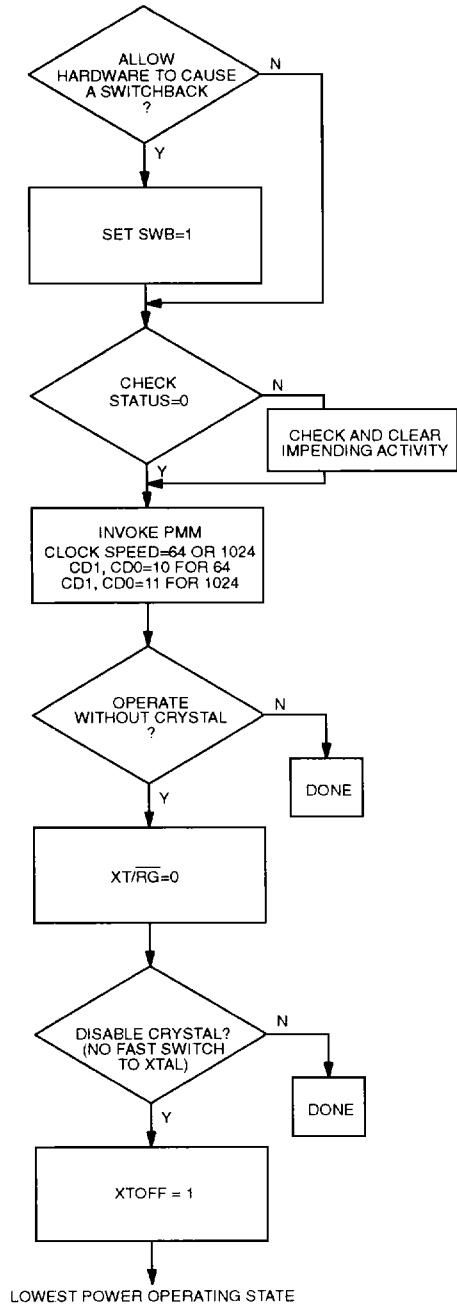
Figure 3 illustrates a typical decision set associated with PMM. The following table is a summary of the bits relating to PMM and its operation.

PMM CONTROL AND STATUS BIT SUMMARY Table 7

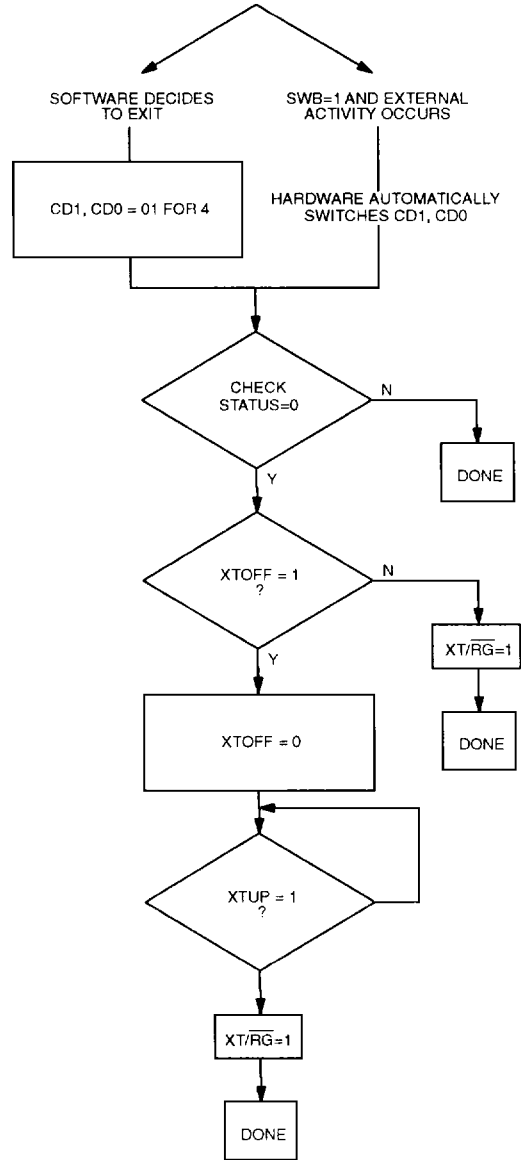
BIT NAME	LOCATION	FUNCTION	RESET	WRITE ACCESS
XT/\overline{RG}	EXIF.3	Control. $XT/\overline{RG}=1$, runs from crystal or external clock; $XT/\overline{RG}=0$, runs from internal ring oscillator.	X	0 to 1 only when XTUP=1 and XTOFF=0
RGMD	EXIF.2	Status. RGMD=1, CPU clock = ring; RGMD=0, CPU clock = crystal.	0	None
CD1, CD0	PMR.7, PMR.6	Control. CD1,0=01, 4 clocks; CS1,0=10, PMM1; CD1,0=11, PMM2.	0, 1	Write CD1,0=10 or 11 only from CD1,0=01
SWB	PMR.5	Control. SWB=1, hardware invokes switchback to 4 clocks, SWB=0, no hardware switchback.	0	Unrestricted
XTOFF	PMR.3	Control. Disables crystal operation after ring is selected.	0	1 only when $XT/\overline{RG}=0$
PIP	STATUS.7	Status. 1 indicates a power-fail interrupt in service.	0	None
HIP	STATUS.6	Status. 1 indicates high priority interrupt in service.	0	None
LIP	STATUS.5	Status. 1 indicates low priority interrupt in service.	0	None
XTUP	STATUS.4	Status. 1 indicates that the crystal has stabilized.	1	None
SPTA1	STATUS.3	Status. Serial transmission on serial port 1.	0	None
SPRA1	STATUS.2	Status. Serial word reception on serial port 1.	0	None
SPTA0	STATUS.1	Status. Serial transmission on serial port 0.	0	None
SPRA0	STATUS.0	Status. Serial word reception on serial port 0.	0	None

INVOKING AND CLEARING PMM Figure 3

ENTER POWER MANAGEMENT MODE



EXITING POWER MANAGEMENT MODE



IDLE MODE

Setting the lsb of the Power Control register (PCON; 87h) invokes the IDLE mode. IDLE will leave internal clocks, serial ports and timers running. Power consumption drops because the CPU is not active. Since clocks are running, the IDLE power consumption is a function of crystal frequency. It should be approximately 1/2 of the operational power at a given frequency. The CPU can exit the IDLE state with any interrupt or a reset. IDLE is available for backward software compatibility. The system can now reduce power consumption to below IDLE levels by using PMM1 or PMM2 and running NOPs.

STOP MODE ENHANCEMENTS

Setting bit 1 of the Power Control register (PCON; 87h) invokes the STOP mode. STOP mode is the lowest power state since it turns off all internal clocking. The I_{CC} of a standard STOP mode is approximately 1 μ A (but is specified in the Electrical Specifications). The CPU will exit STOP mode from an external interrupt or a reset condition. Internally generated interrupts (timer, serial port, watchdog) are not useful since they require clocking activity.

The DS87C520 provides two enhancements to the STOP mode. As documented below, the DS87C520 provides a band-gap reference to determine Power-fail Interrupt and Reset thresholds. The default state is that the band-gap reference is off while in STOP mode. This allows the extremely low power state mentioned above. A user can optionally choose to have the band-gap enabled during STOP mode. With the band-gap reference enabled, PFI and Power-fail Reset are functional and are a valid means for leaving STOP mode. This allows software to detect and compensate for a brown-out or power supply sag, even when in STOP mode. In STOP mode with the band-gap enabled, I_{CC} will be approximately 50 μ A compared with 1 μ A with the band-gap off. If a user does not require a Power-fail Reset or Interrupt while in STOP mode, the band-gap can remain disabled. Only the most power sensitive applications should turn off the band-gap, as this results in an uncontrolled power-down condition.

The control of the band-gap reference is located in the Extended Interrupt Flag register (EXIF; 91h). Setting BGS (EXIF.0) to a 1 will keep the band-gap reference enabled during STOP mode. The default or reset condi-

tion is with the bit at a logic 0. This results in the band-gap being off during STOP mode. Note that this bit has no control of the reference during full power, PMM, or IDLE modes.

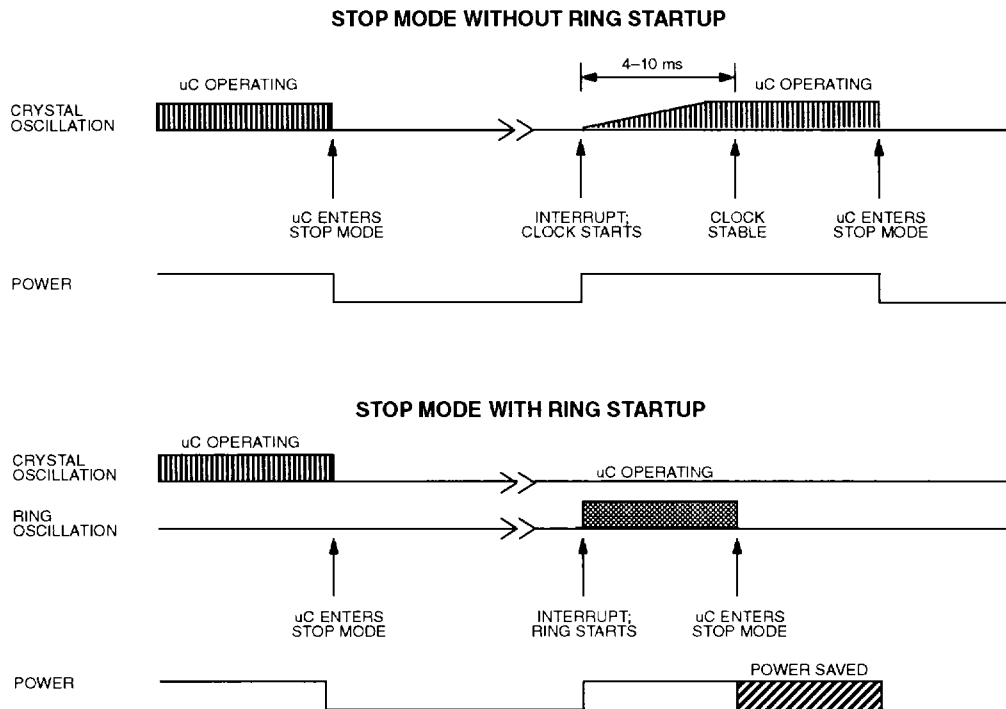
The second feature allows an additional power saving option while also making STOP easier to use. This is the ability to start instantly when exiting STOP mode. It is the internal ring oscillator that provides this feature. This ring can be a clock source when exiting STOP mode in response to an interrupt. The benefit of the ring oscillator is as follows.

Using STOP mode turns off the crystal oscillator and all internal clocks to save power. This requires that the oscillator be restarted when exiting STOP mode. Actual start-up time is crystal dependent, but is normally at least 4 ms. A common recommendation is 10 ms. In an application that will wake-up, perform a short operation, then return to sleep, the crystal start-up can be longer than the real transaction. However, the ring oscillator will start instantly. Running from the ring, the user can perform a simple operation and return to sleep before the crystal has even started. If a user selects the ring to provide the start-up clock and the processor remains running, hardware will automatically switch to the crystal once a power-on reset interval (65536 clocks) has expired. Hardware uses this value to assure proper crystal start even though power is not being cycled.

The ring oscillator runs at approximately 4 MHz but will not be a precise value. Do not conduct real-time precision operations (including serial communication) during this ring period. Figure 3 shows how the operation would compare when using the ring, and when starting up normally. The default state is to exit STOP mode without using the ring oscillator.

The RGSL – Ring Select bit at EXIF.1 (EXIF; 91h) controls this function. When RGSL=1, the CPU will use the ring oscillator to exit STOP mode quickly. As mentioned above, the processor will automatically switch from the ring to the crystal after a delay of 65,536 crystal clocks. For a 3.57 MHz crystal, this is approximately 18 ms. The processor sets a flag called RGMD–Ring Mode, located at EXIF.2, that tells software that the ring is being used. The bit will be a logic 1 when the ring is in use. Attempt no serial communication or precision timing while this bit is set, since the operating frequency is not precise.

RING OSCILLATOR EXIT FROM STOP MODE Figure 4



Note: Diagram assumes that the operation following STOP requires less than 18 ms to complete.

EMI REDUCTION

The DS87C520 allows software to reduce EMI. One of the major contributors to radiated noise in an 8051 based system is the toggling of ALE. The DS87C520 allows software to disable ALE when not used by setting the ALE OFF (PMR.2) bit to a 1. When ALEOFF=1, ALE will still toggle during an off-chip MOVX. However, ALE will remain in a static mode when performing on-chip memory access. The default state of ALEOFF=0 so ALE toggles at a frequency of XTAL/4.

PERIPHERAL OVERVIEW

The DS87C520 provides several of the most commonly needed peripheral functions in microcomputer-based systems. These new functions include a second serial port, Power-fail Reset, Power-fail Interrupt, and a programmable Watchdog Timer. These are described below, and more details are available in the High-Speed Micro User's Guide.

SERIAL PORTS

The DS87C520 provides a serial port (UART) that is identical to the 80C52. In addition it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.2 (RXD1) and P1.3 (TXD1). It has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1 at C0h, SBUF1 at C1h) to the original. The new serial port can only use Timer 1 for timer generated baud rates.

TIMER RATE CONTROL

There is one important difference between the DS87C520 and 8051 regarding timers. The original 8051 used 12 clocks per cycle for timers as well as for

machine cycles. The DS87C520 architecture normally uses four clocks per machine cycle. However, in the area of timers and serial ports, the DS87C520 will default to 12 clocks per cycle on reset. This allows existing code with real-time dependencies such as baud rates to operate properly.

If an application needs higher speed timers or serial baud rates, the user can select individual timers to run at the 4 clock rate. The Clock Control register (CKCON; 8Eh) determines these timer speeds. When the relevant CKCON bit is a logic 1, the DS87C520 uses four clocks per cycle to generate timer speeds. When the bit is a 0, the DS87C520 uses 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

POWER FAIL RESET

The DS87C520 uses a precision band-gap voltage reference to decide if V_{CC} is out of tolerance. While powering up, the internal monitor circuit maintains a reset state until V_{CC} rises above the V_{RST} level. Once above this level, the monitor enables the crystal oscillator and counts 65536 clocks. It then exits the reset state. This power-on reset (POR) interval allows time for the oscillator to stabilize.

A system needs no external components to generate a power-related reset. Anytime V_{CC} drops below V_{RST} , as in power failure or a power drop, the monitor will generate and hold a reset. It occurs automatically, needing no action from the software. Refer to the Electrical Specifications for the exact value of V_{RST} .

POWER FAIL INTERRUPT

The voltage reference that sets a precise reset threshold also generates an optional early warning Power-Fail Interrupt (PFI). When enabled by software, the processor will vector to program memory address 0033h if V_{CC} drops below V_{PFW} . PFI has the highest priority. The PFI enable is in the Watchdog Control SFR (WDCON – D8h). Setting WDCON.5 to a logic 1 will enable the PFI.

Application software can also read the PFI flag at WDCON.4. A PFI condition sets this bit to a 1. The flag is independent of the interrupt enable and software must manually clear it.

WATCHDOG TIMER

To prevent software from losing control, the DS87C520 includes a programmable Watchdog Timer. The Watchdog is a free running timer that sets a flag if allowed to reach a preselected time-out. It can be (re)started by software.

A typical application is to select the flag as a reset source. When the Watchdog times out, it sets its flag which generates reset. Software must restart the timer before it reaches its time-out or the processor is reset.

Software can select one of four time-out values. Then, it restarts the timer and enables the reset function. After enabling the reset function, software must then restart the timer before its expiration or hardware will reset the CPU. Both the Watchdog Reset Enable and the Watchdog Restart control bits are protected by a "Timed Access" circuit. This prevents errant software from accidentally clearing the Watchdog. Time-out values are precise since they are a function of the crystal frequency as shown in Table 8. For reference, the time periods at 33 MHz also are shown.

The Watchdog also provides a useful option for systems that do not require a reset circuit. It will set an interrupt flag 512 clocks before setting the reset flag. Software can optionally enable this interrupt source. The interrupt is independent of the reset. A common use of the interrupt is during debug, to show developers where the Watchdog times out. This indicates where the Watchdog must be restarted by software. The interrupt also can serve as a convenient time-base generator or can wake-up the processor from power saving modes.

The Watchdog function is controlled by the Clock Control (CKCON – 8Eh), Watchdog Control (WDCON – D8h), and Extended Interrupt Enable (EIE – E8h) SFRs. CKCON.7 and CKCON.6 are WD1 and WD0 respectively and they select the Watchdog time-out period as shown in Table 8.

WATCHDOG TIME-OUT VALUES Table 8

WD1	WD0	INTERRUPT TIME-OUT	TIME (33 MHz)	RESET TIME-OUT	TIME (33 MHz)
0	0	2^{17} clocks	3.9718 ms	$2^{17} + 512$ clocks	3.9874 ms
0	1	2^{20} clocks	31.77 ms	$2^{20} + 512$ clocks	31.79 ms
1	0	2^{23} clocks	254.20 ms	$2^{23} + 512$ clocks	254.21 ms

As shown above, the Watchdog Timer uses the crystal frequency as a time base. A user selects one of four counter values to determine the time-out. These clock counter lengths are $2^{17}=131,072$ clocks; $2^{20}=1,048,576$; $2^{23}=8,388,608$ clocks; and $2^{26}=67,108,864$ clocks. The times shown in Table 8 above are with a 33 MHz crystal frequency. Once the counter chain has completed a full interrupt count, hardware will set an interrupt flag. Regardless of whether the user enables this interrupt, there are then 512 clocks left until the reset flag is set. Software can enable the interrupt and reset individually. Note that the Watchdog is a free running timer and does not require an enable. There are five control bits in special function registers that affect the Watchdog Timer and two status flags that report to the user. WDIF (WDCON.3) is the interrupt flag that is set at timer termination when there are 512 clocks remaining until the reset flag is set. WTRF (WDCON.2) is the flag that is set when the timer has completely timed out. This flag is normally associated with a CPU reset and allows software to determine the reset source.

EWT (WDCON.1) is the enable for the Watchdog timer reset function. RWT (WDCON.0) is the bit that software uses to restart the Watchdog Timer. Setting this bit restarts the timer for another full interval. Application software must set this bit before the time-out. Both of these bits are protected by Timed Access discussed below. As mentioned previously, WD1 and 0 (CKCON.7 and 6) select the time-out. Finally, the user can enable the Watchdog Interrupt using EWDI (EIE.4). The Special Function Register map is shown above.

INTERRUPTS

The DS87C520 provides 13 interrupt sources with three priority levels. The Power-fail Interrupt (PFI) has the highest priority. Software can assign high or low priority to other sources. All interrupts that are new to the 8051 family, except for the PFI, have a lower natural priority than the originals.

INTERRUPT SOURCES AND PRIORITIES Table 9

NAME	DESCRIPTION	VECTOR	NATURAL PRIORITY	8051/DALLAS
PFI	Power Fail Interrupt	33h	1	DALLAS
INT0	External Interrupt 0	03h	2	8051
TF0	Timer 0	0Bh	3	8051
INT1	External Interrupt 1	13h	4	8051
TF1	Timer 1	1Bh	5	8051
SCON0	TI0 or RI0 from serial port 0	23h	6	8051
TF2	Timer 2	2Bh	7	8051
SCON1	TI1 or RI1 from serial port 1	3Bh	8	DALLAS
INT2	External Interrupt 2	43h	9	DALLAS
INT3	External Interrupt 3	4Bh	10	DALLAS
INT4	External Interrupt 4	53h	11	DALLAS
INT5	External Interrupt 5	5Bh	12	DALLAS
WDTI	Watchdog Time-Out Interrupt	63h	13	DALLAS
RTCI	Real-Time clock Interrupt	6Bh	14	DALLAS

TIMED ACCESS PROTECTION

It is useful to protect certain SFR bits from an accidental write operation. The Timed Access procedure stops an errant CPU from accidentally changing these bits. It requires that the following instructions precede a write of a protected bit.

```
MOV          0C7h, #0AAh
MOV          0C7h, #55h
```

Writing an AAh then a 55h to the Timed Access register (location C7h) opens a 3 cycle window for write access. The window allows software to modify a protected bit(s). If these instructions do not immediately precede the write operation, then the write will not take effect. The protected bits are:

EXIF.0	BGS	Band-gap Select
WDCON.6	POR	Power-on Reset flag
WDCON.1	EWT	Enable Watchdog Reset
WDCON.0	RWT	Restart Watchdog
WDCON.3	WDIF	Watchdog Interrupt Flag
ROMSIZE.2	RS2	ROM size select 2
ROMSIZE.1	RS1	ROM size select 1
ROMSIZE.0	RS0	ROM size select 0

EPROM PROGRAMMING

The DS87C520 follows standards for a 16K byte EPROM version in the 8051 family. It is available in a UV erasable, ceramic windowed package and in plastic

packages for one-time user-programmable versions. The part has unique signature information so programmers can support its specific EPROM options.

PROGRAMMING PROCEDURE

The DS87C520 should run from a clock speed between 4 and 6 MHz when programmed. The programming fixture should apply address information for each byte to the address lines and the data value to the data lines. The control signals must be manipulated as shown in Table 10. The diagram in Figure 5 shows the expected electrical connection for programming. Note that the programmer must apply addresses in demultiplexed fashion to Ports 1 and 2 with data on Port 0. Waveforms and timing are provided in the Electrical Specifications.

Program the DS87C520 as follows:

1. Apply the address value,
2. Apply the data value,
3. Select the programming option from Table 10 using the control signals,
4. Increase the voltage on V_{PP} from 5V to 12.75V if writing to the EPROM,
5. Pulse the \overline{PROG} signal five times for EPROM array and 25 times for encryption table, lock bits, and other EPROM bits,
6. Repeat as many times as necessary.

EPROM PROGRAMMING MODES Table 10

MODE	RST	PSEN	ALE/PROG	EA/VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data	H	L	PL	12.75V	L	H	H	H	H
Verify Code Data	H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3Fh	H	L	PL	12.75V	L	H	H	L	H
Program Lock Bits									
	LB1	H	L	PL	12.75V	H	H	H	H
	LB2	H	L	PL	12.75V	H	H	H	L
	LB3	H	L	PL	12.75V	H	L	H	L
Program Option Register Address FCh	H	L	PL	12.75V	L	H	H	L	L
Read Signature or Option Registers 30, 31, 60, FCh	H	L	H	H	L	L	L	L	L

* PL indicates pulse to a logic low.

EPROM LOCK BITS Table 11

LEVEL	LOCK BITS			PROTECTION
	LB1	LB2	LB3	
1	U	U	U	No program lock. Encrypted verify if encryption table was programmed.
2	P	U	U	Prevent MOV _C instructions in external memory from reading program bytes in internal memory. EA is sampled and latched on reset. Allow no further programming of EPROM.
3	P	P	U	Level 2 plus no verify operation. Also, prevent MOV _X instructions in external memory from reading SRAM (MOV _X) in internal memory.
4	P	P	P	Level 3 plus no external execution.

SECURITY OPTIONS

The DS87C520 employs a standard three-level lock that restricts viewing of the EPROM contents. A 64-byte Encryption Array allows the authorized user to verify memory by presenting the data in encrypted form.

Lock Bits

The security lock consists of three lock bits. These bits select a total of four levels of security. Higher levels provide increasing security but also limit application flexibility. Table 11 shows the security settings. Note that the programmer cannot directly read the state of the security lock. User software has access to this information as described in the Memory section.

Encryption Array

The Encryption Array allows an authorized user to verify EPROM without allowing the true memory to be dumped. During a verify, each byte is Exclusive NORed (XNOR) with a byte in the Encryption Array. This results in a true representation of the EPROM while the Encryption is unprogrammed (FFh). Once the Encryption Array is programmed in a non-FFh state, the verify value will be encrypted.

For encryption to be effective, the Encryption Array must be unknown to the party that is trying to verify memory. The entire EPROM also should be a non-FFh state or the Encryption Array can be discovered.

The Encryption Array is programmed as shown in Table 10. Note that the programmer cannot read the array. Also note that the verify operation always uses the

Encryption Array. The array has no impact while FFh. Simply programming the array to a non-FFh state will cause the encryption to function.

OTHER EPROM OPTIONS

The DS87C520 has user selectable options that must be set before beginning software execution. These options use EPROM bits rather than SFRs.

Program the EPROM selectable options as shown in Table 10. The Option Register sets or reads these selections. The bits in the Option Control Register have the following function:

Bit 7–4 Reserved, program to a 1.

Bit 3 Watchdog POR default. Set=1; Watchdog reset function is disabled on power-up. Set=0; Watchdog reset function is enabled automatically.

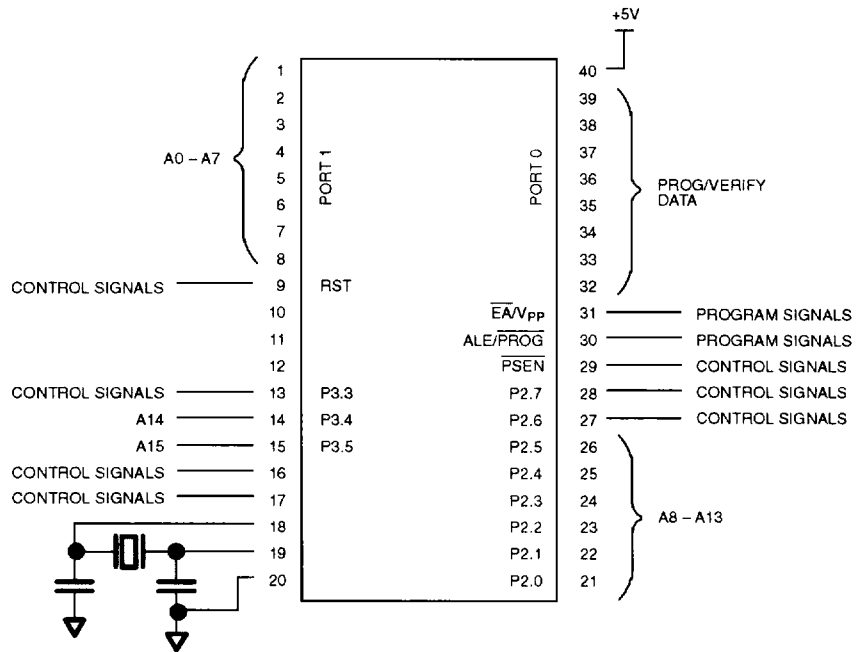
Bit 2–0 Reserved. Program to a 1.

SIGNATURE

The Signature bytes identify the product and programming revision to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h. This information is as follows::

Address	Value	Meaning
30h	DAh	Manufacturer
31h	20h	Model
60h	01h	Extension

EPROM PROGRAMMING CONFIGURATION Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground

-0.3V to +7.0V

Operating Temperature

0°C to 70°C

Storage Temperature

-55°C to +125°C

Soldering Temperature

260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{CC}=4.0V$ to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Power Fail Warning	V_{PFW}	4.25	4.38	4.5	V	1
Minimum Operating Voltage	V_{RST}	4.0	4.13	4.25	V	1
Supply Current Active Mode	I_{CC}		30		mA	2
Supply Current Idle Mode	I_{IDLE}		15		mA	3
Supply Current Stop Mode	I_{STOP}		1		μA	4
Supply Current Stop Mode, Band-gap	I_{SPBG}		50		μA	4, 5
Input Low Level	V_{IL}	-0.3		+0.8	V	1
Input High Level	V_{IH}	2.0		$V_{CC}+0.3$	V	1
Input High Level XTAL1 and RST	V_{IH2}	3.5		$V_{CC}+0.3$	V	1
Output Low Voltage @ $I_{OL}=1.6$ mA	V_{OL1}		0.15	0.45	V	1
Output Low Voltage Port 0 @ $I_{OL}=3.2$ mA	V_{OL2}		0.15	0.45	V	1
Output High Voltage Ports 1, 2, 3, ALE, PSEN @ $I_{OH}=-50$ μA	V_{OH1}	2.4			V	1, 7
Output High Voltage Ports 1, 2, 3 @ $I_{OH}=-50$ μA	V_{OH2}	2.4			V	1, 8
Output High Voltage Ports 1, 2, 3 @ $I_{OH}=-1.5$ mA	V_{OH3}	2.4			V	1, 9
Output High Voltage Port 0 in Bus Mode $I_{OH}=-800$ μA	V_{OH4}	2.4			V	1, 6
Input Low Current Ports 1, 2, 3 @ 0.45V	I_{IL}			-50	μA	
Transition Current from 1 to 0 Ports 1, 2, 3 @ 2V	I_{TL}			-650	μA	10
Input Leakage Port 0, \overline{EA}	I_L	-10		+10	μA	11
RST Pull-down Resistance	R_{RST}	50		150	k Ω	

NOTES:

1. All voltages are referenced to ground.
2. Active current is measured with a 25 MHz clock source driving XTAL1, max V_{CC} between V_{CC} and GND, RST at max V_{CC} , all other pins disconnected.
3. Idle mode current is measured with a 25 MHz clock source driving XTAL1, max V_{CC} between V_{CC} and GND, RST at ground, all other pins disconnected.
4. Stop mode current measured with XTAL1 and RST grounded, max V_{CC} between V_{CC} and GND, all other pins disconnected.
5. Band-gap reference is enabled.
6. When addressing.
7. During a reset condition.
8. At a steady state, not being pulled below V_{IH} externally.
9. During a 0 to 1 transition, a one-shot drives the ports hard for two oscillator clock cycles. Maximum drive occurs at 2.4V.
10. Ports 1, 2, and 3 source transition current when being pulled down externally. Current reaches its maximum at approximately 2V.
11. V_{IN} between ground and $V_{CC} - 0.3V$.
12. Industrial temperature version meets all specifications between $-40^{\circ}C$ and $+85^{\circ}C$.

**EXTERNAL PROGRAM MEMORY
AC ELECTRICAL CHARACTERISTICS**
(0°C to 70°C; V_{CC}=4.0V to 5.5V)

PARAMETER	SYMBOL	33 MHz		VARIABLE CLOCK		NOTES
		MIN	MAX	MIN	MAX	
Oscillator Frequency	1/t _{CLCL}	0	33	0	33	MHz
ALE Pulse Width	t _{LHLL}	40		(3t _{CLCL} /2)-5		ns
Port 0 Address Valid to ALE Low	t _{AVLL}	10		(t _{CLCL} /2)-5		ns
Address Hold after ALE Low	t _{LLAX}	10		(t _{CLCL} /2)-5		ns
ALE Low to Valid Instruction In	t _{LLIV}		56		2.5t _{CLCL} -20	ns
ALE Low to $\overline{\text{PSEN}}$ Low	t _{LLPL}	10		(t _{CLCL} /2)-5		ns
$\overline{\text{PSEN}}$ Pulse Width	t _{PLPH}	55		2t _{CLCL} - 5		ns
$\overline{\text{PSEN}}$ Low to Valid Instr. In	t _{PLIV}		41		2t _{CLCL} -20	ns
Input Instruction Hold after $\overline{\text{PSEN}}$	t _{PXIX}	0		0		ns
Input Instruction Float after $\overline{\text{PSEN}}$	t _{PXIZ}		26		t _{CLCL} -5	ns
Port 0 Address to Valid Instr. In	t _{AVIV}		71		3t _{CLCL} -20	ns
Port 2 Address to Valid Instr. In	t _{AVIV2}		81		3.5t _{CLCL} -25	ns
$\overline{\text{PSEN}}$ Low to Address Float	t _{PLAZ}		0		0	ns

NOTES:

1. All signals rated over operating temperature.
2. All signals characterized with load capacitance of 80 pF except Port 0, ALE, $\overline{\text{PSEN}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ with 100 pF.
3. Interfacing to memory devices with float times (turn off times) over 25 ns may cause contention. This will not damage the parts, but will cause an increase in operating current.

MOVX CHARACTERISTICS USING STRETCH MEMORY CYCLES (0°C to 70°C; V_{CC}=4.0V to 5.5V)

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
Data Access ALE Pulse Width	t _{LHLL2}	(3t _{CLCL} /2)-5 2t _{CLCL} -5		ns	t _{MCS} =0 t _{MCS} >0
Address Hold after ALE Low for MOVX Write	t _{LLAX2}	(t _{CLCL})/2-5		ns	
\overline{RD} Pulse Width	t _{RLRH}	2t _{CLCL} -5 t _{MCS} -10		ns	t _{MCS} =0 t _{MCS} >0
\overline{WR} Pulse Width	t _{WLWH}	2t _{CLCL} -5 t _{MCS} -10		ns	t _{MCS} =0 t _{MCS} >0
\overline{RD} Low to Valid Data In	t _{RLDV}		2t _{CLCL} -20 t _{MCS} -20	ns	t _{MCS} =0 t _{MCS} >0
Data Hold after Read	t _{RHDX}	0		ns	
Data Float after Read	t _{RHDZ}		t _{CLCL} -5 2t _{CLCL} -5	ns	t _{MCS} =0 t _{MCS} >0
ALE Low to Valid Data In	t _{LLDV}		2.5t _{CLCL} -20 t _{MCS} +2t _{CLCL} -40	ns	t _{MCS} =0 t _{MCS} >0
Port 0 Address to Valid Data In	t _{AVDV1}		3t _{CLCL} -20 t _{MCS} +2t _{CLCL} -20	ns	t _{MCS} =0 t _{MCS} >0
Port 2 Address to Valid Data In	t _{AVDV2}		3.5t _{CLCL} -20 t _{MCS} +2.5t _{CLCL} -20	ns	t _{MCS} =0 t _{MCS} >0
ALE Low to \overline{RD} or \overline{WR} Low	t _{LLWL}	(t _{CLCL} /2)-5 (3t _{CLCL} /2)-5	(t _{CLCL} /2)+5 3t _{CLCL} /2+5	ns	t _{MCS} =0 t _{MCS} >0
Port 0 Address to \overline{RD} or \overline{WR} Low	t _{AVWL}	t _{CLCL} -5 (2t _{CLCL})-5		ns	t _{MCS} =0 t _{MCS} >0
Port 2 Address to \overline{RD} or \overline{WR} Low	t _{AVWL2}	(3t _{CLCL} /2)-5 (2.5t _{CLCL})-5		ns	t _{MCS} =0 t _{MCS} >0
Data Valid to \overline{WR} Transition	t _{QVWX}	-5		ns	
Data Hold after Write	t _{WHQX}	t _{CLCL} -5 2t _{CLCL} -5		ns	t _{MCS} =0 t _{MCS} >0
\overline{RD} Low to Address Float	t _{RLAZ}		-(t _{CLCL} /2)-5	ns	
\overline{RD} or \overline{WR} High to ALE High	t _{WHLH}	0 t _{CLCL} -5	10 t _{CLCL} +5	ns	t _{MCS} =0 t _{MCS} >0

NOTE: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

M2	M1	M0	MOVX CYCLES	t _{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles	4 t _{CLCL}
0	1	0	4 machine cycles	8 t _{CLCL}
0	1	1	5 machine cycles	12 t _{CLCL}
1	0	0	6 machine cycles	16 t _{CLCL}
1	0	1	7 machine cycles	20 t _{CLCL}
1	1	0	8 machine cycles	24 t _{CLCL}
1	1	1	9 machine cycles	28 t _{CLCL}

EXTERNAL CLOCK CHARACTERISTICS(0°C to 70°C; $V_{CC}=4.0V$ to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock High Time	t_{CHCX}	15			ns	
Clock Low Time	t_{CLCX}	15			ns	
Clock Rise Time	t_{CLCL}			10	ns	
Clock Fall Time	t_{CHCL}			10	ns	

SERIAL PORT MODE 0 TIMING CHARACTERISTICS(0°C to 70°C; $V_{CC}=4.0V$ to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Serial Port Clock Cycle Time SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XLXL}		$12t_{CLCL}$ $4t_{CLCL}$		ns ns	
Output Data Setup to Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{QVXH}		$10t_{CLCL}$ $3t_{CLCL}$		ns ns	
Output Data Hold from Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHGX}		$2t_{CLCL}$ t_{CLCL}		ns ns	
Input Data Hold after Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHDX}		t_{CLCL} t_{CLCL}		ns ns	
Clock Rising Edge to Input Data Valid SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHDV}		$11t_{CLCL}$ $3t_{CLCL}$		ns ns	

EXPLANATION OF AC SYMBOLS

In an effort to remain compatible with the original 8051 family, this device specifies the same parameters as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t	Time
A	Address
C	Clock
D	Input data
H	Logic level high
L	Logic level low
I	Instruction
P	\overline{PSEN}
Q	Output data
R	\overline{RD} signal
V	Valid
W	\overline{WR} signal
X	No longer a valid logic level
Z	Tristate

POWER CYCLE TIMING CHARACTERISTICS(0°C to 70°C; $V_{CC}=4.0V$ to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Start-up Time	t_{CSU}		1.8		ms	1
Power-on Reset Delay	t_{POR}			65536	t_{CLCL}	2

NOTES:

1. Start-up time for crystals varies with load capacitance and manufacturer. Time shown is for an 11.0592 MHz crystal manufactured by Fox.
2. Reset delay is a synchronous counter of crystal oscillations after crystal start-up. At 33 MHz, this time is 1.99 ms.

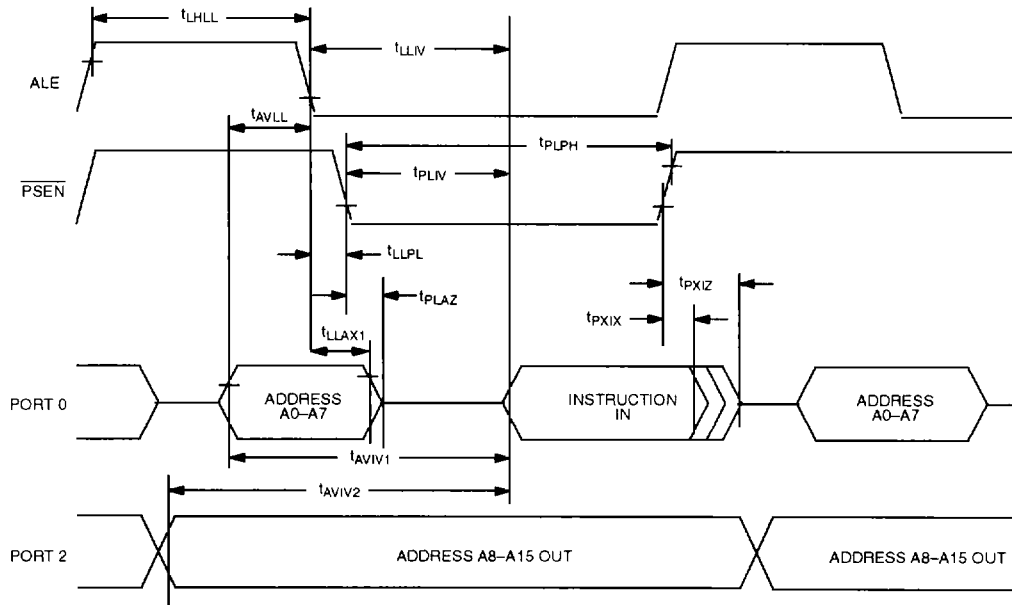
EPROM PROGRAMMING AND VERIFICATION(21°C to 27°C; $V_{CC}=4.5V$ to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Programming Voltage	V_{PP}	12.5		13.0	V	1
Programming Supply Current	I_{PP}			50	mA	
Oscillator Frequency	$1/t_{CLCL}$	4		6	MHz	
Address Setup to \overline{PROG} Low	t_{AVGL}	$48t_{CLCL}$				
Address Hold after \overline{PROG}	t_{GHAX}	$48t_{CLCL}$				
Data Setup to \overline{PROG} Low	t_{DVGL}	$48t_{CLCL}$				
Data Hold after \overline{PROG}	t_{GHDX}	$48t_{CLCL}$				
Enable High to V_{PP}	t_{EHS}	$48t_{CLCL}$				
V_{PP} Setup to \overline{PROG} Low	t_{SHGL}	10			μs	
V_{PP} Hold after \overline{PROG}	t_{GHSL}	10			μs	
\overline{PROG} Width	t_{GLGH}	90		110	μs	
Address to Data Valid	t_{AVQV}			$48t_{CLCL}$		
Enable Low to Data Valid	t_{ELQV}			$48t_{CLCL}$		
Data Float after Enable	t_{EHQZ}	0		$48t_{CLCL}$		
\overline{PROG} High to \overline{PROG} Low	t_{GHGL}	10			μs	

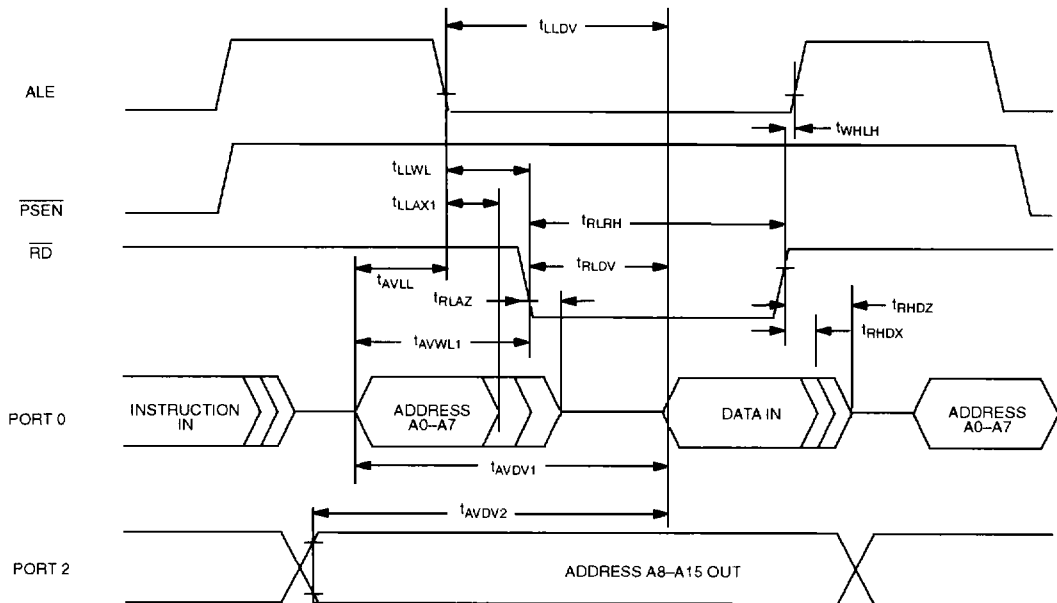
NOTE:

1. All voltages are referenced to ground.

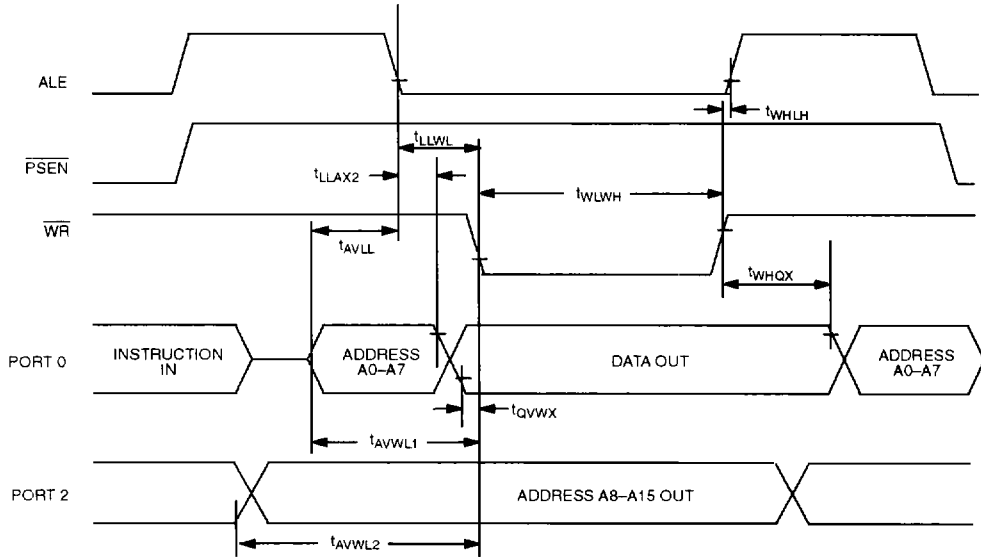
EXTERNAL PROGRAM MEMORY READ CYCLE



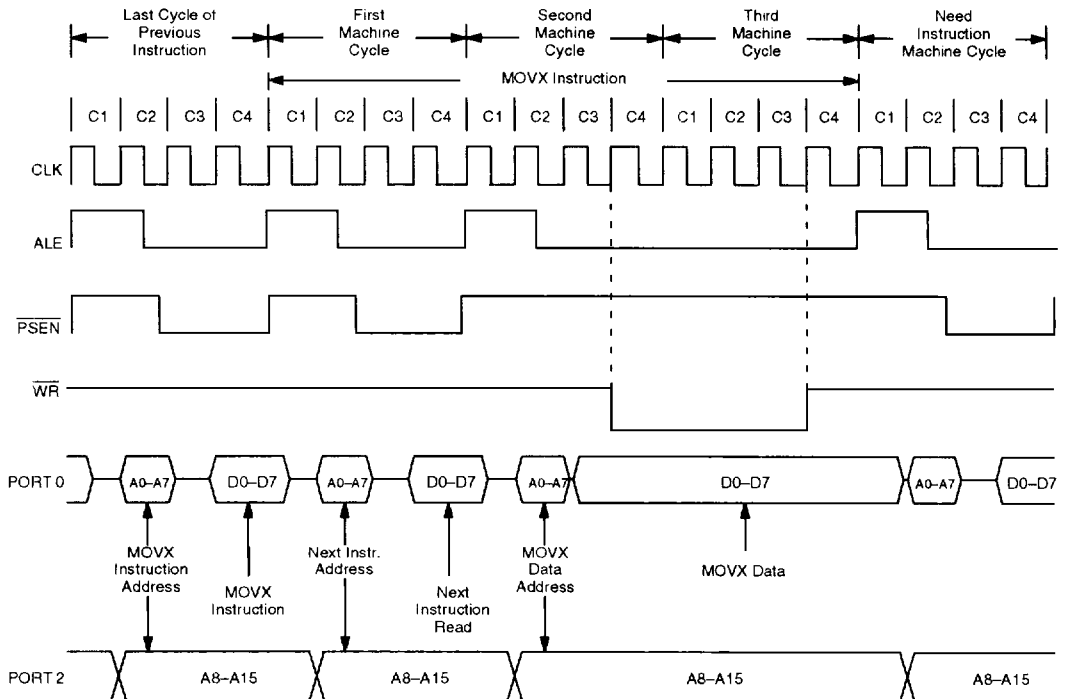
EXTERNAL DATA MEMORY READ CYCLE



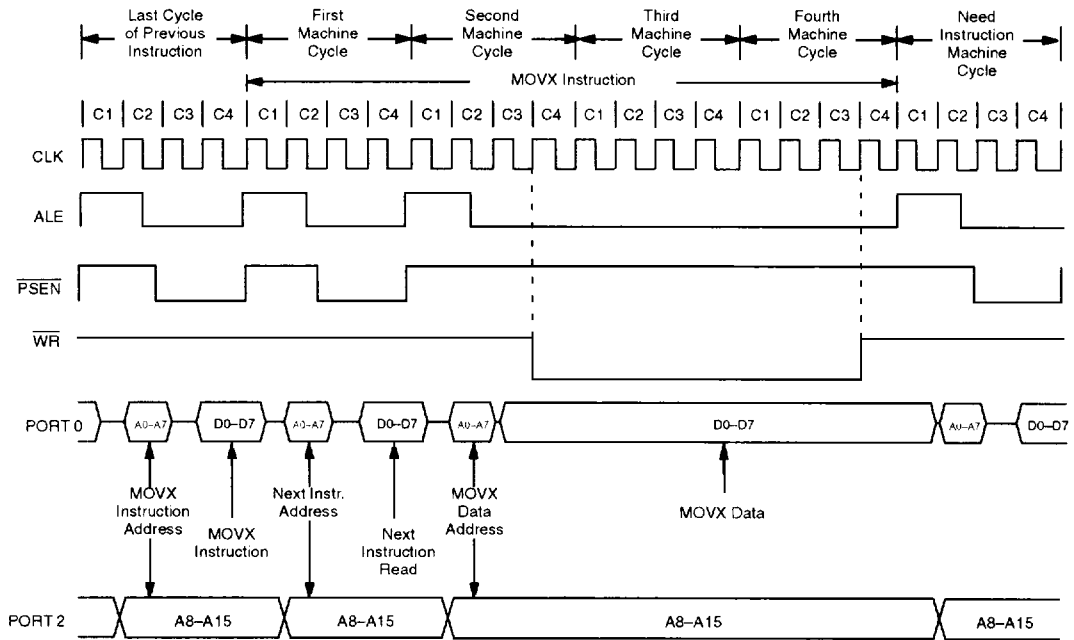
DATA MEMORY WRITE CYCLE



DATA MEMORY WRITE WITH STRETCH=1

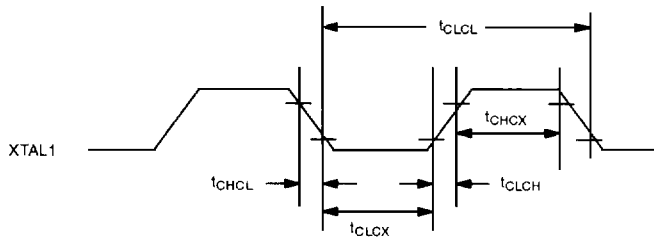


DATA MEMORY WRITE WITH STRETCH=2



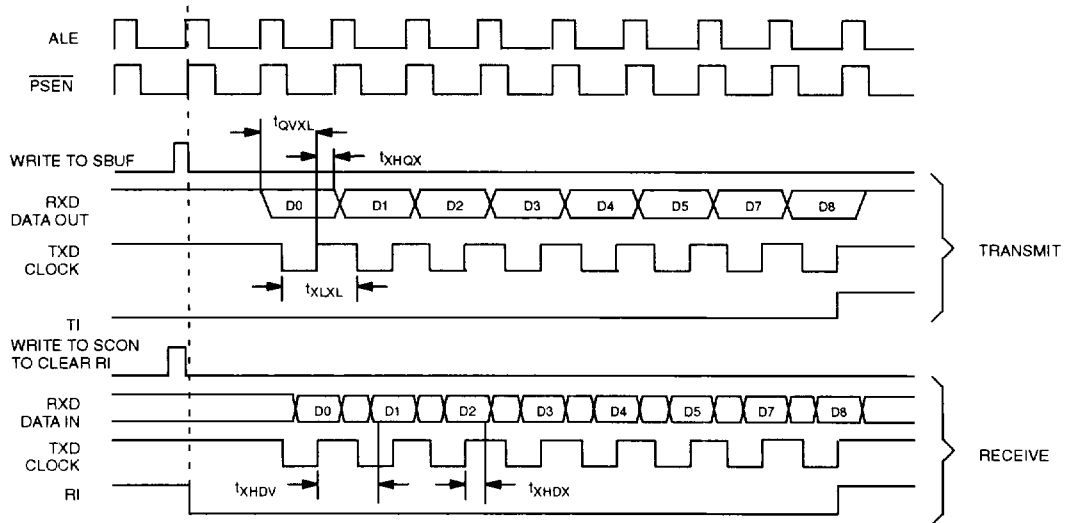
FOUR CYCLE DATA MEMORY WRITE
STRETCH VALUE=2

EXTERNAL CLOCK DRIVE

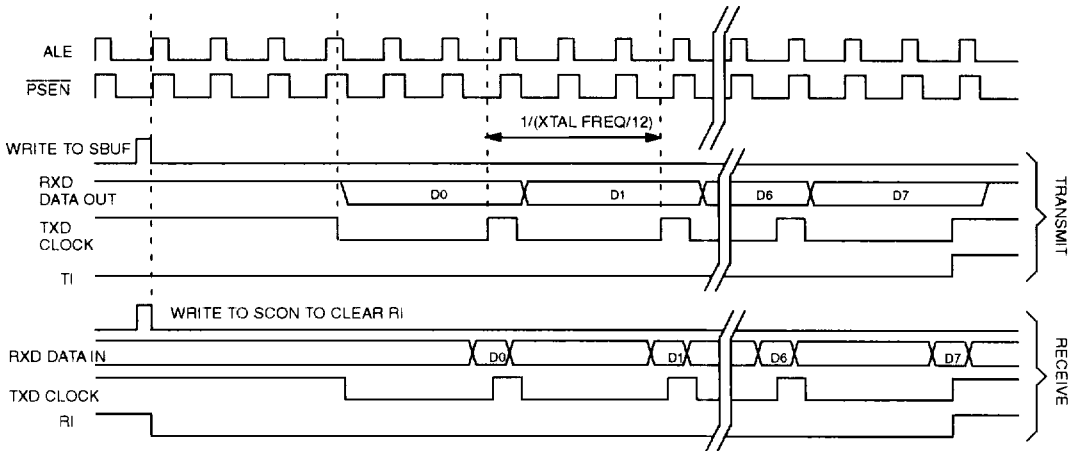


SERIAL PORT MODE 0 TIMING

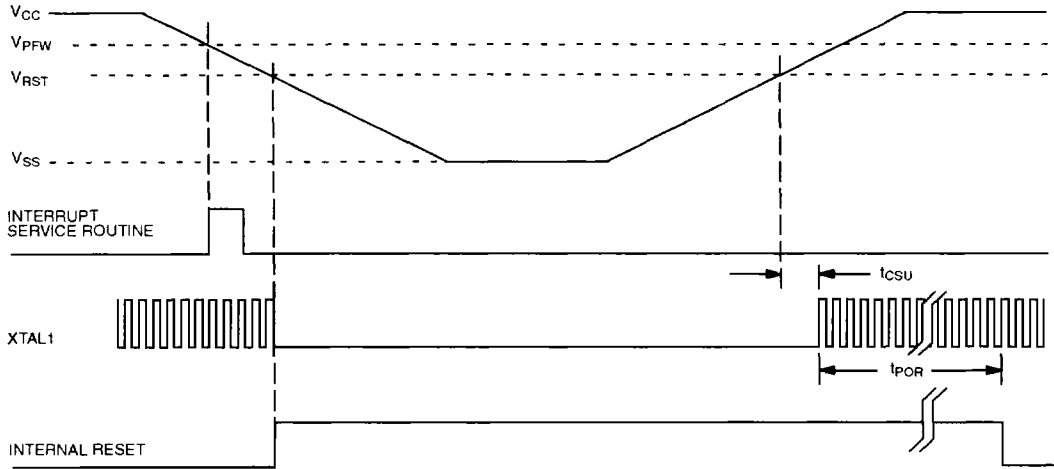
SERIAL PORT 0 (SYNCHRONOUS MODE)
 HIGH SPEED OPERATION SM2=1=>TXD CLOCK=XTAL/4



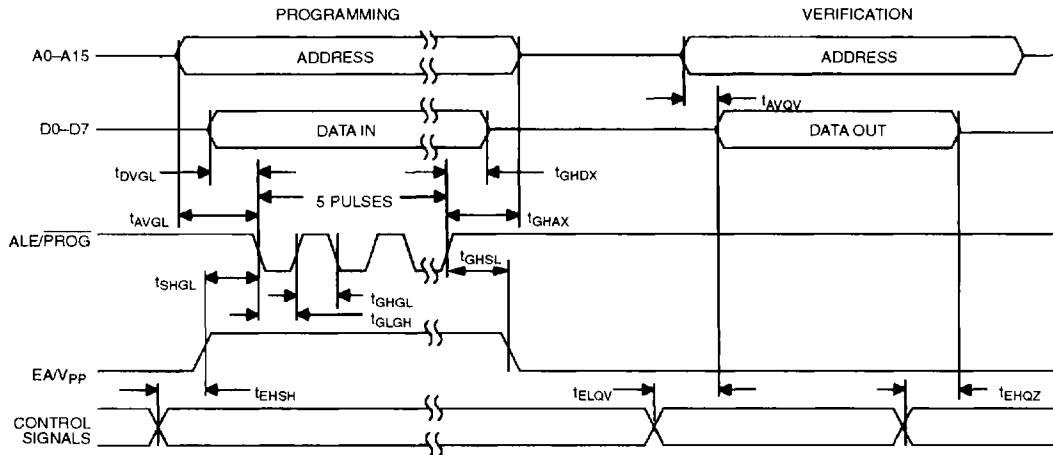
SERIAL PORT 0 (SYNCHRONOUS MODE)
 SM2=0=>TXD CLOCK=XTAL/12



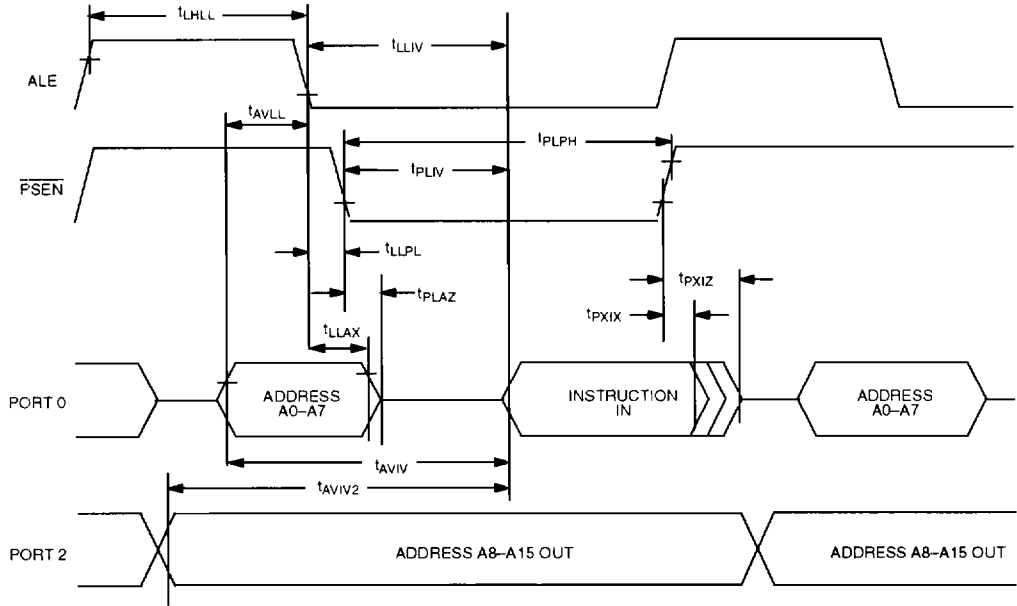
POWER CYCLE TIMING



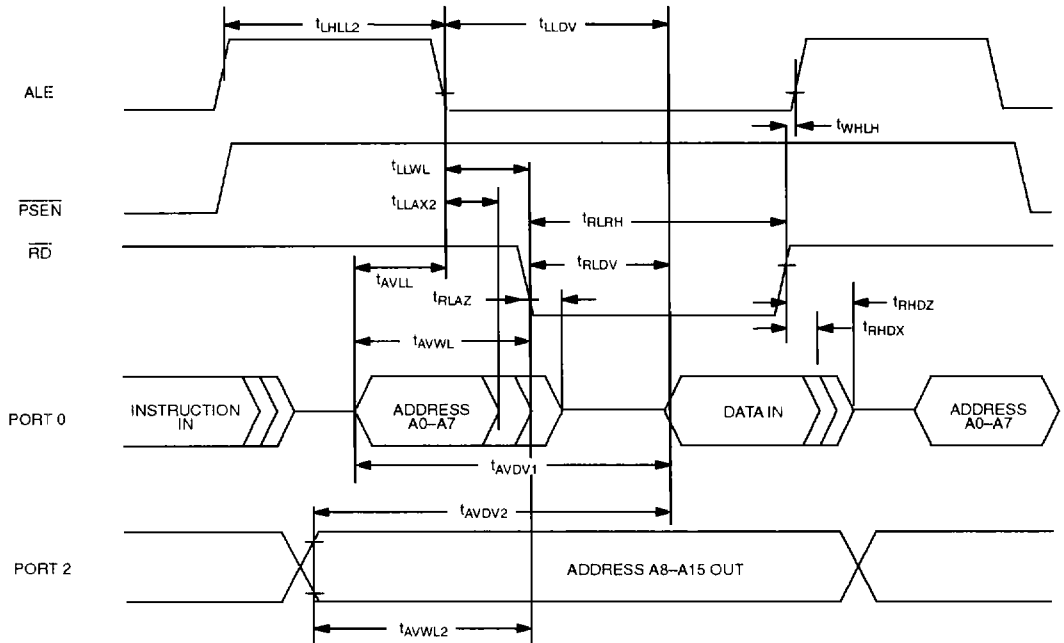
EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



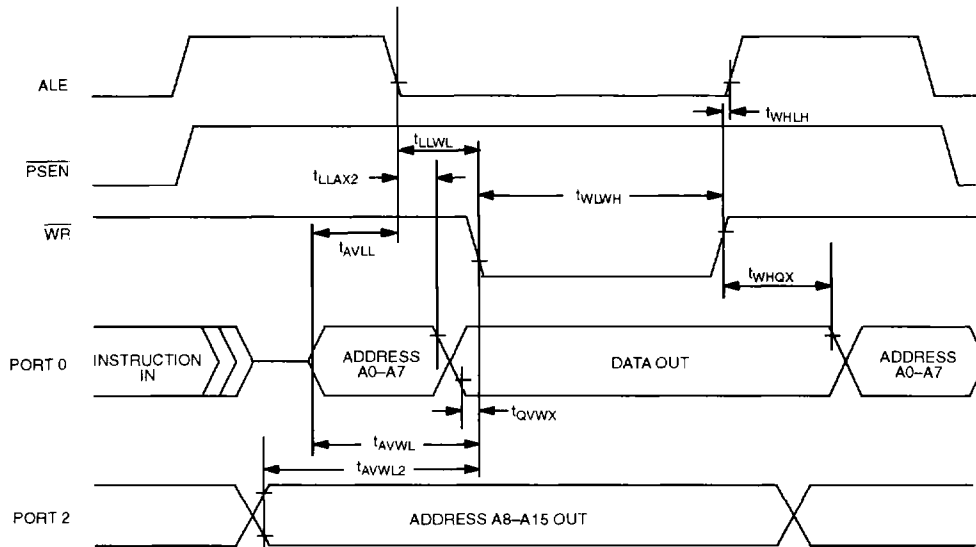
EXTERNAL PROGRAM MEMORY READ CYCLE



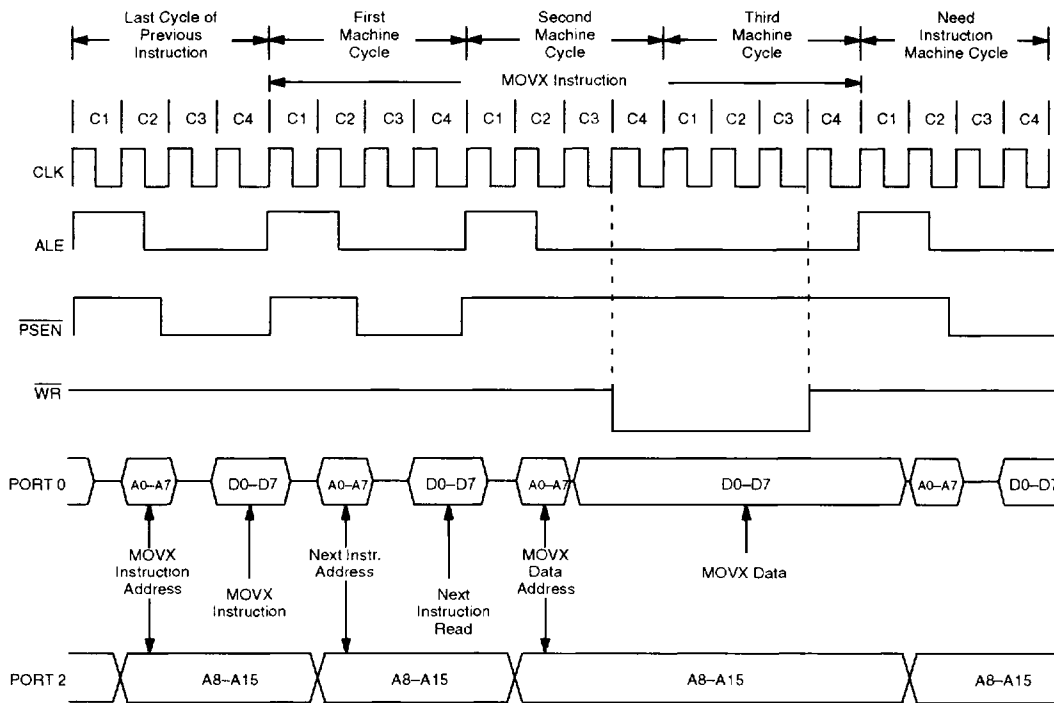
EXTERNAL DATA MEMORY READ CYCLE

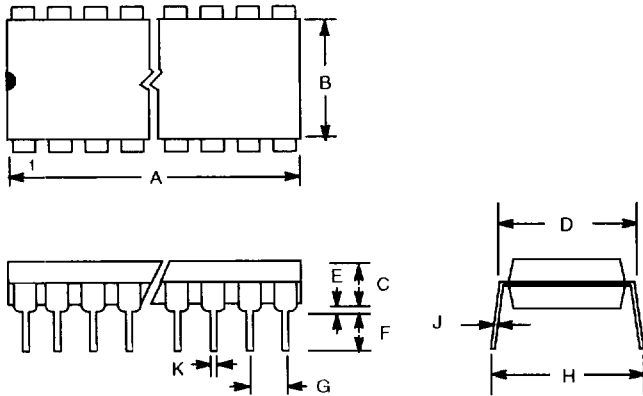


DATA MEMORY WRITE CYCLE



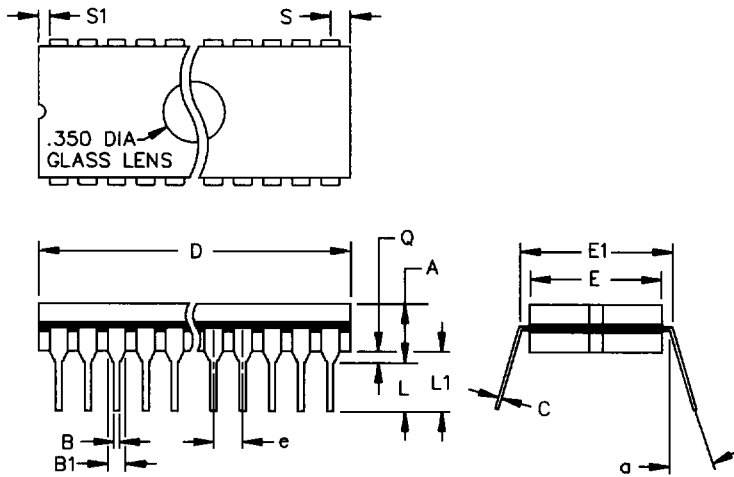
DATA MEMORY WRITE WITH STRETCH=1



40-PIN DIP (600 MIL)

PKG	40-PIN	
	DIM	MIN
A IN. MM	2.050 52.07	2.075 52.71
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.380	0.040 1.02
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.625 15.88	0.675 17.15
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 .56

40-PIN CER DIP

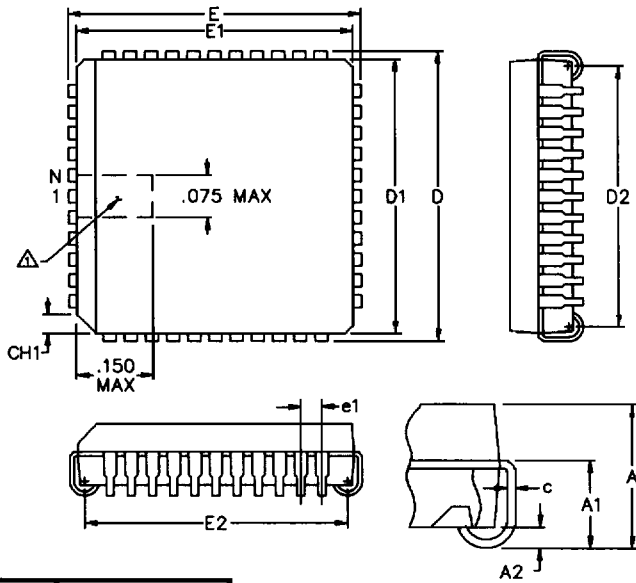


ALL DIMENSIONS ARE IN INCHES.

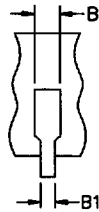
PKG	40-PIN	
	MIN	MAX
A	-	0.225
B	0.014	0.023
B1	0.038	0.065
C	0.006	0.015
D	-	2.096
E	0.510	0.620
E1	0.590	0.630
e	100 BSC	
L	0.125	0.200
L1	0.150	-
Q	0.020	0.060
S	-	0.098
S1	0.005	-
a	0°	15°

44-PIN PLCC

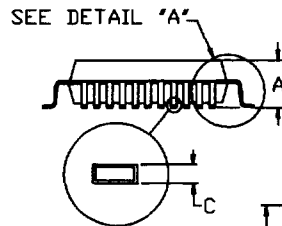
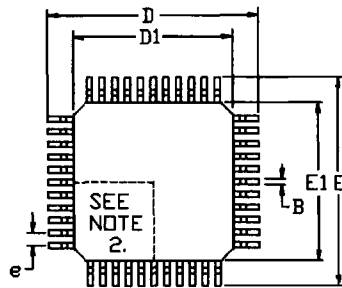
△ Pin 1 identifier to be located in zone indicated.



PKG	44-PIN	
DIM	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	-
B	0.026	0.033
B1	0.013	0.021
c	0.009	0.012
CH1	0.042	0.048
D	0.685	0.695
D1	0.650	0.656
D2	0.590	0.630
E	0.685	0.695
E1	0.650	0.656
E2	0.590	0.630
e1	0.050 BSC	
N	44	-

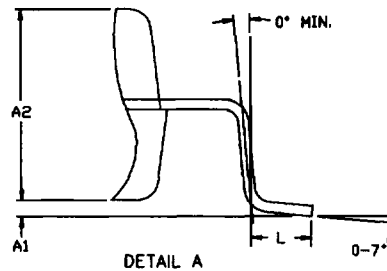


44-PIN MQFP (10 X 10 X 2)



NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIED ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.



DIMENSIONS ARE IN MILLIMETERS.

PKG	44-PIN	
DIM	MIN	MAX
A	-	2.45
A1	0.10	0.30
A2	1.95	2.10
D	13.65	14.30
D1	9.90	10.10
E	13.65	14.30
E1	9.90	10.10
L	0.65	0.95
e	0.80 BSC	
B	0.30	0.45
C	0.13	0.23