



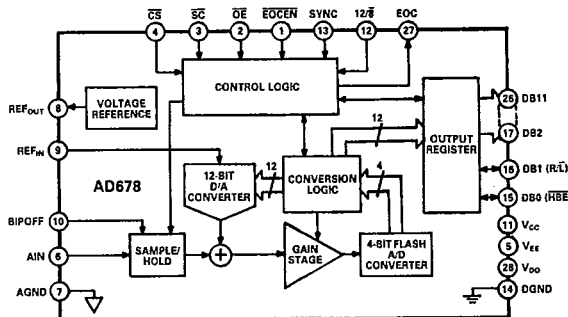
# 12-Bit 200 KSPS Complete Sampling ADC

T-51-10-12 AD678

**FEATURES**

- AC and DC Characterized and Specified
- 200k Conversions per Second
- 1 MHz Full Power Bandwidth
- 500 kHz Full Linear Bandwidth
- 72 dB S/N+D (K Grade)
- Twos Complement Data Format (Bipolar Mode)
- Straight Binary Data Format (Unipolar Mode)
- 10 MΩ Input Impedance
- 8-Bit or 16-Bit Bus Interface
- On-Board Reference and Clock
- 10 V Unipolar or Bipolar Input Range

AD678 FUNCTIONAL BLOCK DIAGRAM



3

**PRODUCT DESCRIPTION**

The AD678 is a complete, multipurpose 12-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The AD678 is similar to the AD1678 in that it is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD which are important in signal processing applications. In addition, the AD678 is fully specified for dc parameters which are important in measurement applications.

The AD678 offers a choice of digital interface formats; the 12 data bits can be accessed by a 16-bit bus in a single read operation or by an 8-bit bus in two read operations (8+4), with right or left justification. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD678 operates from +5 V and ±12 V supplies and dissipates 745 mW. A 28-pin plastic DIP and a 0.6" wide ceramic

DIP are available. Contact factory for surface-mount package options.

Screening to MIL-STD-883C Class B is also available.

**PRODUCT HIGHLIGHTS**

1. **COMPLETE INTEGRATION:** The AD678 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. **SPECIFICATIONS:** The AD678 is specified for both dc and ac parameters. DC specifications (such as INL, gain and offset) are important in control and measurement applications. AC specifications (such as S/N+D ratio, THD and IMD) are of value in signal processing applications.
3. **EASE OF USE:** The pinout is designed for easy board layout, and the choice of single or two read cycle output provides compatibility with 16- or 8-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
4. **RELIABILITY:** The AD678 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.

**AD678 ORDERING GUIDE**  
Temperature Range and Package Options<sup>1</sup>

Plastic DIP (N-28A) 0 to +70°C	PLCC (P-28A) 0 to +70°C	Ceramic DIP (D-28A) 0 to +70°C	Ceramic DIP (D-28A) -55°C to +125°C	Integral Nonlinearity T <sub>min</sub> to T <sub>max</sub>	S/N&D <sup>2</sup>
AD678JN	AD678JP	AD678JD	AD678SD	±1 LSB	71
AD678KN	AD678KP	AD678KD	AD678TD	±1/2 LSB	73

**NOTE**

<sup>1</sup>See Section 14 for package outline information.  
<sup>2</sup>Typical at 10 kHz, -0.5 dB input.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

## SPECIFICATIONS

T-51-10-12

**AC SPECIFICATIONS** ( $T_{\min}$  to  $T_{\max}$ ,  $V_{CC} = +12\text{ V} \pm 5\%$ ,  $V_{EE} = -12\text{ V} \pm 5\%$ ,  $V_{DD} = +5\text{ V} \pm 10\%$ ,  $f_{\text{SAMPLE}} = 200\text{ KSPS}$ ,  
 $f_{\text{IN}} = 10.06\text{ kHz}$  unless otherwise noted)<sup>1</sup>

Parameter	AD678J/S			AD678K/T			Units
	Min	Typ	Max	Min	Typ	Max	
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO @ +25°C $T_{\min}$ to $T_{\max}$	70	71		72	73		dB
	70	71		71	73		dB
TOTAL HARMONIC DISTORTION (THD) @ +25°C $T_{\min}$ to $T_{\max}$		-88	-80		-88	-80	dB
		0.004	0.010		0.004	0.010	%
		-85	-78		-85	-78	dB
		0.005	0.012		0.005	0.012	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		-87	-80		-87	-80	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD) <sup>2</sup> 2nd Order Products 3rd Order Products		-85	-80		-85	-80	dB
		-90	-80		-90	-80	dB

## NOTE

<sup>1</sup> $f_{\text{IN}}$  amplitude = -0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a -0 dB (9.997 V p-p) input signal.

<sup>2</sup> $f_{\text{A}} = 9.08\text{ kHz}$ ,  $f_{\text{B}} = 9.58\text{ kHz}$ , with  $f_{\text{SAMPLE}} = 200\text{ KSPS}$ . See Definition of Specifications section.

Specifications subject to change without notice.

**DIGITAL SPECIFICATIONS** (All device types  $T_{\min}$  to  $T_{\max}$ ,  $V_{CC} = +12\text{ V} \pm 5\%$ ,  $V_{EE} = -12\text{ V} \pm 5\%$ ,  $V_{DD} = +5\text{ V} \pm 10\%$ )

Parameter	Test Conditions	Min	Max	Units
<b>LOGIC INPUTS</b>				
$V_{\text{IH}}$	High Level Input Voltage	2.4		V
$V_{\text{IL}}$	Low Level Input Voltage		0.8	V
$I_{\text{IH}}$	High Level Input Current		10	$\mu\text{A}$
$I_{\text{IL}}$	Low Level Input Current		10	$\mu\text{A}$
$C_{\text{IN}}$	Input Capacitance		10	pF
<b>LOGIC OUTPUTS</b>				
$V_{\text{OH}}$	High Level Output Voltage	4.0		V
		2.4		V
$V_{\text{OL}}$	Low Level Output Voltage		0.4	V
$I_{\text{OZ}}$	High Z Leakage Current		10	$\mu\text{A}$
$C_{\text{OZ}}$	High Z Output Capacitance		10	pF

## NOTES

Specifications shown in boldface are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

**DC SPECIFICATIONS** ( $T_{\min}$  to  $T_{\max}$ ,  $V_{CC} = +12\text{ V} \pm 5\%$ ,  $V_{EE} = -12\text{ V} \pm 5\%$ ,  $V_{DD} = +5\text{ V} \pm 10\%$  unless otherwise indicated)

Parameter	AD678J			AD678K			Units
	Min	Typ	Max	Min	Typ	Max	
TEMPERATURE RANGE	0		+70	0		+70	°C
ACCURACY							
Resolution	12			12			Bits
Integral Linearity Error			$\pm 1$			$\pm 1/2$	LSB
Differential Linearity	11			12			Bits
Unipolar Zero Error (@ 25°C) <sup>1</sup>			$\pm 2$			$\pm 2$	LSB
Bipolar Zero Error (@ 25°C) <sup>1</sup>			$\pm 2$			$\pm 2$	LSB
Gain Error (@ 25°C) <sup>1,2</sup>			$\pm 8$			$\pm 4$	LSB
Temperature Drift (Coefficients)							
Unipolar Zero <sup>3</sup>			$\pm 2$ (10)			$\pm 1$ (5)	LSB (ppm/°C)
Bipolar Zero <sup>3</sup>			$\pm 2$ (10)			$\pm 1$ (5)	LSB (ppm/°C)
Gain <sup>3</sup>			$\pm 9$ (50)			$\pm 5$ (27)	LSB (ppm/°C)
Gain <sup>4</sup>			$\pm 2$ (10)			$\pm 2$ (10)	LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Range	0		+10	0		+10	V
Bipolar Range	-5		+5	-5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1		1		μs
Aperture Delay		10			10		ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage <sup>5</sup>	4.95		5.05	4.98		5.02	V
External Load							
Unipolar Mode			+1.5			+1.5	mA
Bipolar Mode			+0.5			+0.5	mA
POWER SUPPLIES							
Power Supply Rejection							
$V_{CC} = +12\text{ V} \pm 5\%$ <sup>6</sup>			$\pm 1$			$\pm 1$	LSB
$V_{EE} = -12\text{ V} \pm 5\%$			$\pm 1$			$\pm 1$	LSB
$V_{DD} = +5\text{ V} \pm 10\%$			$\pm 1$			$\pm 1$	LSB
Operating Current							
$I_{CC}$		18	20		18	20	mA
$I_{EE}$		25	34		25	34	mA
$I_{DD}$		8	12		8	12	mA
Power Consumption		560	745		560	745	mW

## NOTES

<sup>1</sup>Adjustable to zero. See Figures 6 and 7.<sup>2</sup>Includes internal voltage reference error.<sup>3</sup>Includes internal voltage reference drift.<sup>4</sup>Excludes internal voltage reference drift.<sup>5</sup>With maximum external load applied.<sup>6</sup>1.4 V of headroom is required between  $V_{CC}$  and AIN.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

## SPECIFICATIONS

T-51-10-12

DC SPECIFICATIONS ( $T_{\min}$  to  $T_{\max}$ ,  $V_{CC} = +12\text{ V} \pm 5\%$ ,  $V_{EE} = -12\text{ V} \pm 5\%$ ,  $V_{DD} = +5\text{ V} \pm 10\%$  unless otherwise indicated)

Parameter	AD678S			AD678T			Units
	Min	Typ	Max	Min	Typ	Max	
TEMPERATURE RANGE	-55		+125	-55		+125	°C
ACCURACY							
Resolution	12			12			Bits
Integral Linearity Error			±1			±1/2	LSB
Differential Linearity	11			12			Bits
Unipolar Zero Error (@ 25°C) <sup>1</sup>			±2			±2	LSB
Bipolar Zero Error (@ 25°C) <sup>1</sup>			±2			±2	LSB
Gain Error (@ 25°C) <sup>1,2</sup>			±8			±4	LSB
Temperature Drift (Coefficients)							
Unipolar Zero <sup>3</sup>			±4 (10)			±4 (10)	LSB (ppm/°C)
Bipolar Zero <sup>3</sup>			±4 (10)			±4 (10)	LSB (ppm/°C)
Gain <sup>3</sup>			±18 (44)			±18 (44)	LSB (ppm/°C)
Gain <sup>4</sup>			±4 (10)			±4 (10)	LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Range	0		+10	0		+10	V
Bipolar Range	-5		+5	-5		+5	V
Input Resistance	10			10			MΩ
Input Capacitance	10			10			pF
Input Settling Time			1				μs
Aperture Delay	10			10			ns
Aperture Jitter	150			150			ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage <sup>5</sup>	4.95		5.05	4.98		5.02	V
External Load							
Unipolar Mode			+1.5			+1.5	mA
Bipolar Mode			+0.5			+0.5	mA
POWER SUPPLIES							
Power Supply Rejection							
$V_{CC} = +12\text{ V} \pm 5\%$ <sup>6</sup>			±1			±1	LSB
$V_{EE} = -12\text{ V} \pm 5\%$			±1			±1	LSB
$V_{DD} = +5\text{ V} \pm 10\%$			±1			±1	LSB
Operating Current							
$I_{CC}$	18	20		18	20		mA
$I_{EE}$	25	34		25	34		mA
$I_{DD}$	8	12		8	12		mA
Power Consumption	560	745		560	745		mW

## NOTES

<sup>1</sup>Adjustable to zero. See Figures 6 and 7.<sup>2</sup>Includes internal voltage reference error.<sup>3</sup>Includes internal voltage reference drift.<sup>4</sup>Excludes internal voltage reference drift.<sup>5</sup>With maximum external load applied.<sup>6</sup>1.4 V of headroom is required between  $V_{CC}$  and AIN.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

**TIMING SPECIFICATIONS** (All grades,  $T_{min}$  to  $T_{max}$ ,  $V_{CC} = +12 V \pm 5\%$ ,  $V_{EE} = -12 V \pm 5\%$ ,  $V_{DD} = +5 V \pm 10\%$  unless otherwise noted)

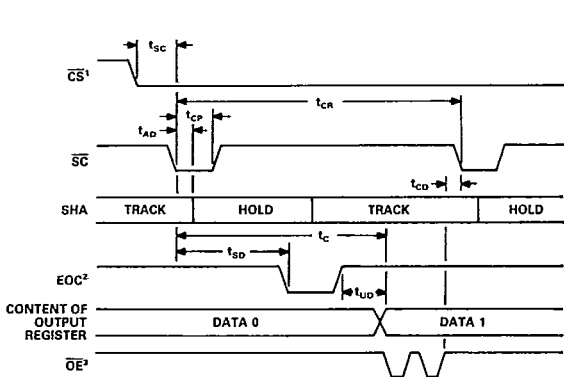
Parameter	Symbol	Min	Typ	Max	Units
SC Delay	$t_{SC}$	50			ns
Conversion Rate	$t_{CR}$		5		$\mu s$
			5.23		$\mu s^1$
Convert Pulse Width	$t_{CP}$	150			ns
Aperture Delay	$t_{AD}$	5		20	ns
Conversion Time <sup>2</sup>	$t_C$		3.9	4.47	$\mu s$
	$t_C$		4.1	4.70	$\mu s^3$
Status Delay	$t_{SD}$	0		400	ns
Access Time <sup>4</sup>	$t_{BA}$			100	ns
Float Delay <sup>5</sup>	$t_{FD}$	10		80	ns
Update Delay	$t_{UD}$			200	ns
Format Setup	$t_{FS}$	60			ns
OE Delay	$t_{OE}$	20			ns
Read Pulse Width	$t_{RP}$	100			ns <sup>6</sup>
		150			ns <sup>7</sup>
Conversion Delay	$t_{CD}$	150			ns
EOCEN Delay	$t_{EO}$	20			ns

3

NOTES

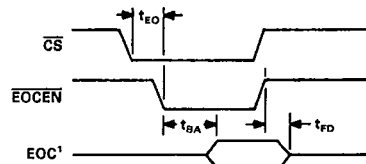
- <sup>1</sup>S, T grades in 8-bit read mode (see Figure 4).
- <sup>2</sup>Includes Acquisition Time.
- <sup>3</sup>S, T grades.
- <sup>4</sup>Measured from the falling edge of  $\overline{OE}/\overline{EOCEN}$  (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 3;  $C_{OUT} = 100$  pF.
- <sup>5</sup>Measured from the rising edge of  $\overline{OE}/\overline{EOCEN}$  (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 3;  $C_{OUT} = 10$  pF.
- <sup>6</sup>12-bit read mode.
- <sup>7</sup>8-bit read mode.

Specifications subject to change without notice.



- NOTES
- <sup>1</sup>IN ASYNCHRONOUS MODE, STATE OF  $\overline{CS}$  DOES NOT AFFECT OPERATION. SEE THE START CONVERSION TRUTH TABLE FOR DETAILS.
- <sup>2</sup> $\overline{EOCEN} = \text{LOW}$ ; FIGURE 2. IN SYNCHRONOUS MODE, EOC IS A THREE-STATE OUTPUT.
- <sup>3</sup>IN ASYNCHRONOUS MODE, EOC IS AN OPEN DRAIN OUTPUT.
- <sup>4</sup>DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing



- NOTE
- <sup>1</sup>SEE END-OF-CONVERT (EOC) PARAGRAPH FOR DETAILS.

Figure 2. EOC Timing

TEST	$V_{CP}$	$C_{OUT}$
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	5 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	0 V	10 pF

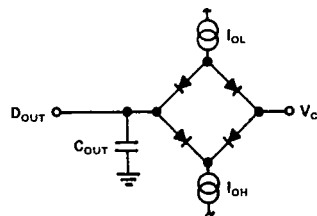


Figure 3. Load Circuit for Bus Timing Specifications

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

**CONVERSION CONTROL**

In synchronous mode (SYNC = HIGH), both Chip Select ( $\overline{CS}$ ) and Start Convert ( $\overline{SC}$ ) must be brought LOW to start a conversion.  $\overline{CS}$  should be LOW  $t_{SC}$  before  $\overline{SC}$  is brought LOW. In asynchronous mode (SYNC = LOW), a conversion is started by bringing  $\overline{SC}$  low, regardless of the state of  $\overline{CS}$ .

Before a conversion is started, End-of-Convert (EOC) is HIGH, and the sample-hold is in track mode. After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample. EOC goes HIGH when the conversion is finished.

In track mode, the sample-hold will settle to  $\pm 0.01\%$  (12 bits) in 1  $\mu s$  maximum. The acquisition time does not affect the throughput rate as the AD678 goes back into track mode more

than 1  $\mu s$  before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW if the maximum throughput rate is needed.

T-51-10-12

**END-OF-CONVERT**

In asynchronous mode, End-of-Convert (EOC) is an open drain output (requiring a minimum 3 k $\Omega$  pull-up resistor) enabled by End-of-Convert ENable ( $\overline{EOCEN}$ ). In synchronous mode, EOC is a three-state output which is enabled by  $\overline{EOCEN}$  and  $\overline{CS}$ . See the Conversion Status Truth Table for details. Access ( $t_{BA}$ ) and float ( $t_{FD}$ ) timing specifications do not apply in asynchronous mode where they are a function of the time constant formed by the 10 pF output capacitance and the pull-up resistor.

**12-BIT MODE CODING FORMAT (1 LSB = 2.44 mV)**

Unipolar Coding (Straight Binary)		Bipolar Coding (Twos Complement)	
$V_{IN}$	Output Code	$V_{IN}$	Output Code
0	000 . . . 0	-5.000 V	100 . . . 0
5.000 V	100 . . . 0	-0.002 V	111 . . . 1
9.9964 V	111 . . . 1	0	000 . . . 0
		+2.500 V	010 . . . 0
		+4.9964 V	011 . . . 1

**START CONVERSION TRUTH TABLE**

	INPUTS			STATUS
	SYNC	$\overline{CS}$	$\overline{SC}$	
Synchronous Mode	1	1	X	No Conversion
	1	0	$\downarrow$	Start Conversion
	1	$\downarrow$	0	Start Conversion (Not Recommended)
	1	0	0	Continuous Conversion
Asynchronous Mode	0	X	1	No Conversion
	0	X	$\downarrow$	Start Conversion
	0	X	0	Continuous Conversion

**NOTES**

- 1 = HIGH voltage level.
- 0 = LOW voltage level.
- X = Don't care.
- $\downarrow$  = HIGH to LOW transition. Must stay low for  $t = t_{CP}$ .

**CONVERSION STATUS TRUTH TABLE**

	INPUTS			OUTPUT	STATUS
	SYNC	$\overline{CS}$	$\overline{EOCEN}$	EOC	
Synchronous Mode	1	0	0	0	Converting
	1	0	0	1	Not Converting
	1	1	X	High Z	Either
	1	X	1	High Z	Either
Asynchronous Mode*	0	X	0	0	Converting
	0	X	1	High Z	Not Converting

**NOTES**

- 1 = HIGH voltage level.
- 0 = LOW voltage level.
- X = Don't care.
- \*EOC requires a pull-up resistor in asynchronous mode.

**OUTPUT ENABLE TRUTH TABLES**

**12-BIT MODE (12 $\overline{S}$  = HIGH)**

INPUTS	OUTPUT
$(\overline{CS} \text{ U } \overline{OE})$	DB11-DB0
1	High Z
$\downarrow$	Enable 12-Bit Output

**8-BIT MODE (12 $\overline{S}$  = LOW)**

	INPUTS			OUTPUTS											
	R/L	HBE	$(\overline{CS} \text{ U } \overline{OE})$	DB11 . . . DB4											
	X	X	1	High Z											
Unipolar Mode	1	0	$\downarrow$	0	0	0	0	a	b	c	d				
	1	1	$\downarrow$	e	f	g	h	i	j	k	l				
	0	0	$\downarrow$	a	b	c	d	e	f	g	h				
	0	1	$\downarrow$	i	j	k	l	0	0	0	0				
Bipolar Mode	1	0	$\downarrow$	a	a	a	a	a	b	c	d				
	1	1	$\downarrow$	e	f	g	h	i	j	k	l				
	0	0	$\downarrow$	a	b	c	d	e	f	g	h				
	0	1	$\downarrow$	i	j	k	l	0	0	0	0				

**NOTES**

- 1 = HIGH voltage level.
- 0 = LOW voltage level.
- X = Don't care.
- U = Logical OR.
- a = MSB.
- l = LSB.
- $\downarrow$  = HIGH to LOW transition. Must stay low for  $t = t_{RP}$ .

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Dynamic Performance - AD678

T-51-10-12

OUTPUT ENABLE OPERATION

The data bits (DB11-DB0) are three-state outputs enabled by Chip Select ( $\overline{CS}$ ) and Output Enable ( $\overline{OE}$ ).  $\overline{CS}$  should be LOW  $t_{OE}$  before  $\overline{OE}$  is brought LOW. Bits DB1 ( $R/\overline{L}$ ) and DB0 ( $\overline{HBE}$ ) are bidirectional. In 12-bit mode they are data output bits. In 8-bit mode they are inputs which define the format of the output register.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to  $REF_{OUT}$ ), output coding is twos complement binary.

When EOC goes HIGH, the output register contains the results of the previous conversion. A period of time  $t_{UD}$  is required for the present conversion results to be loaded into the output register. Bringing  $\overline{OE}$  LOW  $t_{OE}$  after  $\overline{CS}$  goes LOW makes the output register contents available on the data bits. A period of time  $t_{CD}$  is required after  $\overline{OE}$  is brought HIGH before the next  $\overline{SC}$  instruction is issued. This allows internal logic states to reset and guarantees minimum aperture jitter for the next conversion.

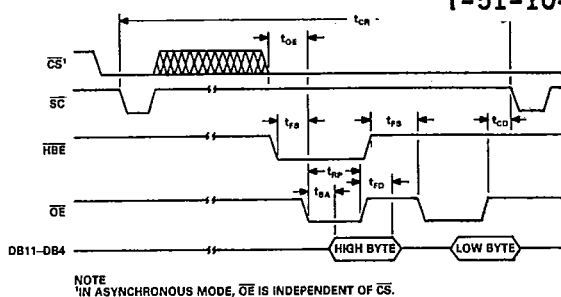
Output Enable ( $\overline{OE}$ ) must be toggled to update the output register in both 8- and 12-bit read modes.

Figure 4 illustrates the 8-bit read mode ( $12/\overline{8} = \text{LOW}$ ), where only DB11-DB4 are used as output lines onto an 8-bit bus. The output is read in two steps, with the high byte read first, followed by the low byte. High Byte Enable ( $\overline{HBE}$ ) controls the output sequence. The 12-bit result can be right or left justified depending on the state of  $R/\overline{L}$ . Note that for S and T grades, the 8-bit read mode results in a conversion rate of 5.23  $\mu\text{s}$ .

In 12-bit read mode ( $12/\overline{8} = \text{HIGH}$ ), a single READ operation accesses all 12 output bits on DB11-DB0 for interface to a 16-bit bus. Figure 5 provides the output timing relationships. Note that  $t_{CR}$  must be observed, in that  $\overline{SC}$  pulses should not be issued at intervals closer than 5  $\mu\text{s}$ . If  $\overline{SC}$  is asserted sooner than 5  $\mu\text{s}$ , conversion accuracy may deteriorate. For this reason,  $\overline{SC}$  should not be held LOW in an attempt to operate in a continuous convert mode.

POWER-UP

A conversion sequence, consisting of one  $\overline{SC}$  instruction, is required after power-up to reset internal logic.



NOTE  
IN ASYNCHRONOUS MODE,  $\overline{OE}$  IS INDEPENDENT OF  $\overline{CS}$ .

Figure 4. Output Timing, 8-Bit Read Mode

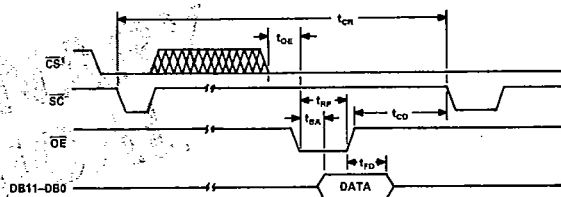


Figure 5. Output Timing, 12-Bit Read Mode

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

3

## Definition of Specifications

T-51-10-12

### NYQUIST FREQUENCY

An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

### SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

### TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

### PEAK SPURIOUS OR PEAK HARMONIC COMPONENT

The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

### INTERMODULATION DISTORTION (IMD)

With inputs consisting of sine waves at two frequencies,  $f_a$  and  $f_b$ , any device with nonlinearities will create distortion products, of order  $(m + n)$ , at sum and difference frequencies of  $m f_a \pm n f_b$ , where  $m, n = 0, 1, 2, 3 \dots$ . Intermodulation terms are those for which  $m$  or  $n$  is not equal to zero. For example, the second order terms are  $(f_a + f_b)$  and  $(f_a - f_b)$  and the third order terms are  $(2 f_a + f_b)$ ,  $(2 f_a - f_b)$ ,  $(f_a + 2 f_b)$  and  $(f_a - 2 f_b)$ . The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is  $-0.5$  dB from full scale (9.44 V p-p). The IMD products are normalized to a 0 dB input signal.

### BANDWIDTH

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-and-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than  $-0.1$  dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD678 has been designed to optimize input bandwidth, allowing the AD678 to undersample input signals with frequencies significantly above the converter's Nyquist frequency.

### APERTURE DELAY

Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ( $\overline{SC}$ ) to when the input signal is held for conversion. In synchronous mode, Chip Select ( $\overline{CS}$ ) should be LOW before  $\overline{SC}$  to minimize aperture delay.

### APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

### INPUT SETTLING TIME

Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

### DIFFERENTIAL LINEARITY (DNL)

In an ideal ADC, code transitions are 1LSB apart. Differential linearity is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes (NMC) are guaranteed.

This specification is 12 bits from  $T_{min}$  to  $T_{max}$  for the AD678K and T grades, which guarantees that all 4096 codes are present over temperature. The AD678J and S grades specify 11 bits NMC  $T_{min}$  to  $T_{max}$ , which means that missing codes do not occur adjacent to each other.

### UNIPOLAR ZERO ERROR

In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

### BIPOLAR ZERO ERROR

In the bipolar mode, the major carry transition (1111 1111 1111 to 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

### GAIN ERROR

The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for a 0-10 V range, 4.9963 volts for a  $\pm 5$  V range). The gain error is the deviation of the actual level at the last transition from the ideal level with the zero error trimmed out. This error can be adjusted as shown in the Input Connections and Calibration section.

### INTEGRAL LINEARITY ERROR (INL)

The ideal transfer function for a linear ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2LSB before the first code transition. "Full scale" is defined as a level 1 1/2LSB beyond the last code transition. Integral linearity error is the worst-case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

The AD678K and T grades are guaranteed for maximum integral linearity error of  $\pm 1/2$ LSB  $T_{min}$  to  $T_{max}$ . For these grades, this means that an analog value which falls exactly in the center of a given code will result in the correct digital output code. Values nearer the upper or lower transition of the code may produce the next upper or lower digital output code. The AD678J and S grades are guaranteed to  $\pm 1$ LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user adjustable.



## Definition of Specifications – AD678

**POWER SUPPLY REJECTION**

Variations in power supply will affect the full-scale calibration. This will result in a linear change in all lower-order codes. The specifications show the maximum change in the full-scale transition point due to a change in power-supply voltage from the nominal value.

**TEMPERATURE COEFFICIENT**

This is the maximum change in the parameter from the initial value (@ 25°C) to the value at  $T_{min}$  or  $T_{max}$ .

T-51-10-12

**AD678 PIN DESCRIPTION**

Symbol	Pin No.	Type	Name and Function
AGND	7	P	Analog Ground. This is the ground return for AIN only.
AIN	6	AI	Analog Signal Input.
BIPOFF	10	AI	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to $REF_{OUT}$ through 50 $\Omega$ resistor for $\pm 5$ V input bipolar mode and two complement binary output coding. See Figures 7 and 8.
$\overline{CS}$	4	DI	Chip Select. Active LOW.
DGND	14	P	Digital Ground
DB11-DB4	26-19	DO	Data Bits 11 through 4. In 12-bit format (see 12/8 pin), these pins provide the upper 8 bits of data. In 8-bit format, these pins provide all 12 bits in two bytes (see R/L pin). Active HIGH.
DB3, DB2	18, 17	DO	Data Bits 3 and 2. In 12-bit format, these pins provide Data Bit 3 and Data Bit 2. Active HIGH. In 8-bit format they are undefined and should be tied to $V_{DD}$ .
DB1 (R/L)	16	DO	In 12-bit format, Data Bit 1. Active HIGH.
DB0( $\overline{HBE}$ )	15	DO	In 12-bit format, Data Bit 0. Active HIGH.
EOC	27	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. In asynchronous mode, EOC is an open drain output and requires an external 3 k $\Omega$ pull-up resistor. See $\overline{EOCEN}$ and SYNC pins for information on EOC gating.
$\overline{EOCEN}$	1	DI	End-Of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{HBE}$ (DB0)	15	DI	In 8-bit format, High Byte Enable. If LOW, output contains high byte. If HIGH, output contains low byte.
$\overline{OE}$	2	DI	Output Enable. The falling edge of $\overline{OE}$ enables DB11-DB0 in 12-bit format and DB11-DB4 in 8-bit format. Gated with $\overline{CS}$ . Active LOW.
$REF_{IN}$	9	AI	Reference Input. +5 V input gives 10 V full scale range.
$REF_{OUT}$	8	AO	+5 V Reference Output. Tied to $REF_{IN}$ through 50 $\Omega$ resistor for normal operation.
R/L (DB1)	16	DI	In 8-bit format, Right/Left justified. Sets alignment of 12-bit result within 16-bit field. Tied to $V_{DD}$ for right-justified output and tied to DGND for left-justified output.
$\overline{SC}$	3	DI	Start Convert. Active LOW. See SYNC pin for gating.
SYNC	13	DI	SYNC Control. If tied to $V_{DD}$ (synchronous mode), $\overline{SC}$ , EOC and $\overline{EOCEN}$ are gated by $\overline{CS}$ . If tied to DGND (asynchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are independent of $\overline{CS}$ , and EOC is an open drain output. EOC requires an external 3 k $\Omega$ pull-up resistor in asynchronous mode.
$V_{CC}$	11	P	+12 V Analog Power.
$V_{EE}$	5	P	-12 V Analog Power.
$V_{DD}$	28	P	+5 V Digital Power.
12/8	12	DI	Twelve/eight bit format. If tied HIGH, sets output format to 12-bit parallel. If tied LOW, sets output format to 8-bit multiplexed.

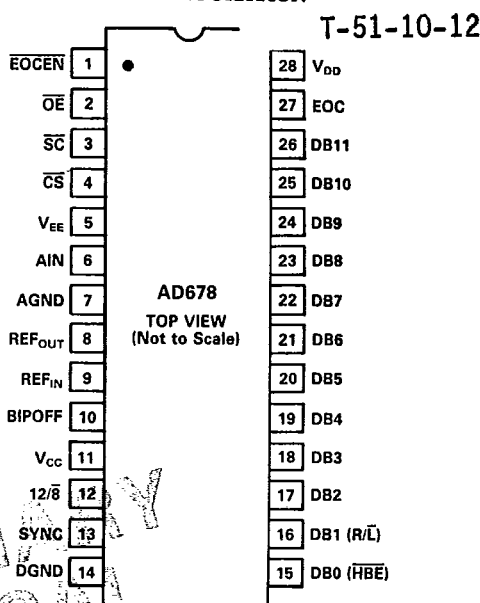
Type: AI = Analog Input.  
 AO = Analog Output.  
 DI = Digital Input (TTL and 5 V CMOS compatible).  
 DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are three-state drivers.  
 P = Power.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ABSOLUTE MAXIMUM RATINGS\*

Specification	With Respect To	Min	Max	Units
V <sub>CC</sub>	AGND	-0.3	+18	V
V <sub>EE</sub>	AGND	-18	+0.3	V
V <sub>CC</sub>	V <sub>EE</sub>	-0.3	+26.4	V
V <sub>DD</sub>	DGND	0	+7	V
AGND	DGND	-1	+1	V
A <sub>IN</sub> , REF <sub>IN</sub>	AGND	-12	+12	V
REF <sub>IN</sub>	V <sub>EE</sub>	0	V <sub>CC</sub>	V
REF <sub>IN</sub>	V <sub>CC</sub>	V <sub>EE</sub>	0	V
Digital Inputs	DGND	-0.5	+7	V
Digital Outputs	DGND	-0.5	V <sub>DD</sub> + 0.3	V
Max Junction Temperature			175	°C
Operating Temperature				
J and K Grades		0	+70	°C
S and T Grades		-55	+125	°C
Storage Temperature		-65	+150	°C
Lead Temperature (10 sec max)			+300	°C

PIN CONFIGURATION



\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The AD678 features input protection circuitry consisting of large, "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD678 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.



Application Information

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD678 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 1000 Ω. The 10 V p-p full-scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC.

The AD678 is factory trimmed to minimize linearity, offset and gain errors. In unipolar mode, the only external component that is required is a 50 Ω ±1% resistor. Two resistors are required in bipolar mode. If offset and gain are not critical (as in some ac applications), even these components can be eliminated.

In some applications, offset and gain errors need to be trimmed out completely. The following sections describe the correct procedure for these various situations.

UNIPOLAR RANGE INPUTS

Offset and gain errors can be trimmed out by using the configuration shown in Figure 6. This circuit allows approximately ±25 mV of offset trim range (±10 LSB) and ±0.5% of gain trim (±20 LSB).

The nominal offset is 1/2 LSB so that the analog range that corresponds to each code will be centered in the middle of that code (halfway between the transitions to the codes above and below it). Thus the first transition (from 0000 0000 0000 to 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (1.22 mV above ground for a 10 V range). To trim unipolar zero to this nominal value, apply a 1.22 mV signal to A<sub>IN</sub> and adjust R1 until the first transition is located.

The gain trim is done by adjusting R2. If the nominal value is required, apply a signal 1 1/2 LSB below full scale (9.9963 V for a 10 V range) and adjust R2 until the last transition is located (1111 1111 1110 to 1111 1111 1111).

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

## Application Information — AD678

T-51-10-12

If offset adjustment is not required, BIPOFF should be connected directly to AGND. If gain adjustment is not required, R2 should be replaced with a fixed  $50\ \Omega \pm 1\%$  metal film resistor. If  $REF_{OUT}$  is connected directly to  $REF_{IN}$ , the additional gain error will be approximately 1%.

**BIPOLAR RANGE INPUTS**

The connections for the bipolar mode are shown in Figure 7. In this mode, data output coding will be in two's-complement binary. This circuit will allow approximately  $\pm 25\ mV$  of offset trim range ( $\pm 10\ LSB$ ) and  $\pm 0.5\%$  of gain trim range (20 LSB).

Either or both of the trim pots can be replaced with  $50\ \Omega \pm 1\%$  fixed resistors if the AD678 accuracy limits are sufficient for the application. If the pins are shorted together, the additional offset and gain errors will be approximately 1%.

To trim bipolar zero to its nominal value, apply a signal  $1/2\ LSB$  below midrange ( $-1.22\ mV$  for a  $\pm 5\ V$  range) and adjust R1 until the major carry transition is located (1111 1111 1111 to 0000 0000 0000). To trim the gain, apply a signal  $1\ 1/2\ LSB$  below full scale ( $+4.9963\ V$  for a  $\pm 5\ V$  range) and adjust R2 to give the last positive transition (0111 1111 1110 to 0111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single-pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal  $1/2\ LSB$  above minus full scale ( $-4.9988\ V$  for a  $\pm 5\ V$  range) and adjust R1 until the minus full-scale transition is located (1000 0000 0000 to 1000 0000 001). Then perform the gain error trim as outlined above.

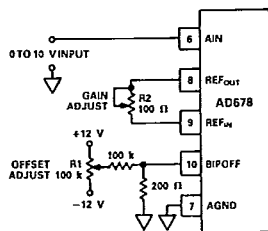


Figure 6. Unipolar Input Connections with Gain and Offset Trims

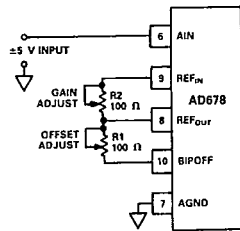


Figure 7. Bipolar Input Connections with Gain and Offset Trims

**BOARD LAYOUT**

Designing with high-resolution data converters requires careful attention to layout considerations. Trace impedance is the first issue. At the 12-bit level, a 5 mA current through a  $0.5\ \Omega$  trace will develop a voltage drop of 2.5 mV, which is 1 LSB for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high-accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return

routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD678 incorporates several features to help the user's layout. First of all, analog pins ( $V_{EE}$ , AIN, AGND,  $REF_{OUT}$ ,  $REF_{IN}$ , BIPOFF,  $V_{CC}$ ) are adjacent to help isolate analog from digital signals. In addition, the  $10\ M\Omega$  input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit design. Current through AGND is  $200\ \mu A$ , with no code-dependent variation. The only current through DGND is the return current for DB11-DB0 and EOC.

**SUPPLY DECOUPLING**

The AD678 power supplies should be well filtered, well regulated, and free from high-frequency noise. Switching power supplies are not recommended. These supplies generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and analog ground. A  $10\ \mu F$  tantalum capacitor in parallel with a  $0.1\ \mu F$  ceramic provides adequate decoupling. The power supply pins should be decoupled directly to DGND.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD678, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD678 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

**GROUNDING**

If a single AD678 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD678. If multiple AD678s are used or the AD678 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

**INTERFACING THE AD678 TO MICROPROCESSORS**

The I/O capabilities of the AD678 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD678 interface configurations.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

**AD678 TO TMS320C25**

In Figure 8 the AD678 is mapped into the TMS320C25 I/O space. AD678 conversions are initiated by issuing an OUT instruction to Port 8. EOC status and the conversion result are read in with an IN instruction to Port 8. A single wait state is inserted by generating the processor READY input from IS, Port 8 and MSC. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD678 read instruction.

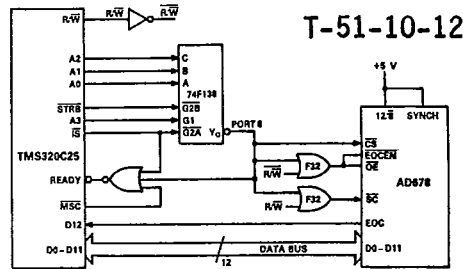


Figure 8. AD678 to TMS320C25 Interface

**AD678 TO 80186**

Figure 9 shows the AD678 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD678 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

In this application the AD678 is configured in the asynchronous mode, which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD678 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ operation resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6-MHz and 8-MHz 80186 processors.

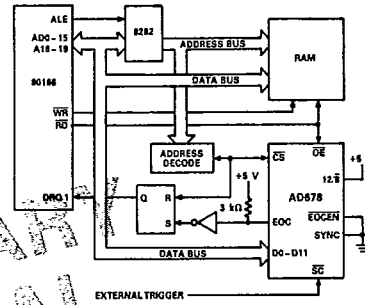


Figure 9. AD678 to 80186 DMA Interface

**AD678 TO Z80**

The AD678 can be interfaced to the Z80 processor in an I/O or memory mapped configuration. Figure 10 illustrates an I/O configuration, where the AD678 occupies several port addresses to allow separate polling of the EOC status and reading of the data. The lower address bit, A0, is used to select the high and low order bytes of the result. The AD678 R/L line is tied HIGH, resulting in right justified output data.

A useful feature of the Z80 is that a single wait state is automatically inserted during I/O operations, allowing the AD678 to be used with Z80 processors having clock speeds up to 8 MHz.

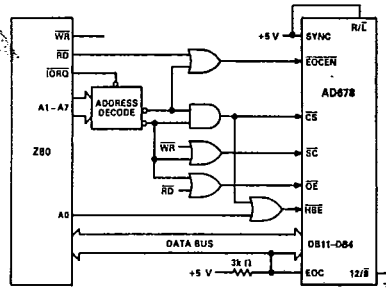


Figure 10. AD678 to Z80 Interface

**AD678 TO ANALOG DEVICES ADSP-2100A**

Figure 11 demonstrates the AD678 interfaced to an ADSP-2100A. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD678 data memory interface with two hardware wait states.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD678 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2100A immediately executes a data memory write instruction which asserts HBE. In the following cycle, the processor starts a data memory read (high byte read) by providing an address on the DMA bus. The decoded address generates OE for the converter. OE, together with logic and latches, is used to force the ADSP-2100A into a two cycle wait state by generating DMACK. The read operation is thus started and completed within 3 processor cycles (240 ns). HBE is released during "high byte read." This allows the processor to read the lower byte of data as soon as "high byte read" is complete. The low byte read operation executes in a similar manner to the first and is completed during the next 240 ns.

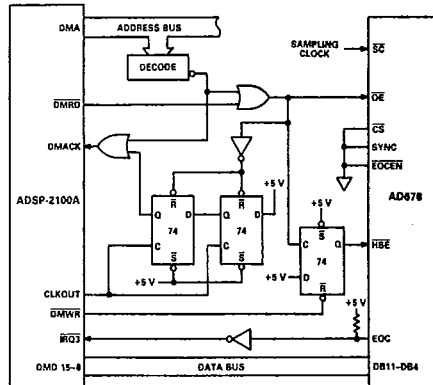


Figure 11. AD678 to ADSP-2100A Interface

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.