DATA SHEET

TDA8007B
Double multiprotocol IC card interface

Product specification
Supersedes data of 2000 Aug 29
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

Double multiprotocol IC card interface TDA8007B

FEATURES

- Control and communication through an 8-bit parallel interface, compatible with multiplexed or non-multiplexed memory access
- Specific ISO UART with parallel access on I/O for automatic convention processing, variable baud rate through frequency or division ratio programming, error management at character level for T = 0, extra guard time register
- 1 to 8 characters FIFO in reception mode
- Parity error counter in reception mode
- Dual V_{CC} generation (5 V ±5%, 65 mA (max.) or 3 V ±8%, 50 mA (max.) with controlled rise and fall times)
- Dual cards clock generation (up to 10 MHz), with two times synchronous frequency doubling
- Cards clock STOP HIGH, clock STOP LOW or 1.25 MHz (from internal oscillator) for cards Power-down mode
- Automatic activation and deactivation sequence through an independent sequencer
- Supports the asynchronous protocols T = 0 and T = 1 in accordance with ISO 7816 and EMV
- Versatile 24-bit time-out counter for Answer To Reset (ATR) and waiting times processing
- 22 Elementary Time Unit (ETU) counter for Block Guard Time (BGT)
- Supports synchronous cards
- Current limitations in the event of short-circuit
- Special circuitry for killing spikes during power-on/-off
- Supply supervisor for power-on/-off reset
- Step-up converter (supply voltage from 2.7 to 6 V), doubler, tripler or follower according to V_{CC} and V_{DD}
- Additional I/O pin allowing use of the ISO UART for another analog interface (pin I/OAUX)
- Additional interrupt pin allowing detection of level toggling on an external signal (pin INTAUX)
- Fast and efficient swapping between the 3 cards due to separate buffering of parameters for each card
- Chip select input allowing use of several devices in parallel and memory space paging
- Enhanced ESD protections on card side [6 kV (min.)]
- Software library for easy integration within the application
- Power-down mode for reducing current consumption when no activity.

APPLICATIONS

- Multiple smart card readers for multiprotocol applications (EMV banking, digital pay TV, access control, etc.).

GENERAL DESCRIPTION

The TDA8007B is a low cost card interface for dual smart card readers. Controlled through a parallel bus, it takes care of all ISO 7816, EMV and GSM11-11 requirements. It may be interfaced to the P0/P2 ports of a 80C51 family microcontroller, and be addressed as a memory through MOVX instructions. It may also be addressed on a non-multiplexed 8-bit data bus, by means of address registers AD0, AD1, AD2 and AD3. The integrated ISO UART and the time-out counters allow easy use even at high baud rates with no real time constraints. Due to its chip select and external I/O and INT features, it greatly simplifies the realization of any number of cards readers. It gives the cards and the reader a very high level of security, due to its special hardware against ESD, short-circuiting, power failure, etc. Its integrated step-up converter allows operation within a supply voltage range of 2.7 to 6 V.

A software library has been developed, taking care of all actions required for T = 0, T = 1 and synchronous protocols (see application reports).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8007BHL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.7	–	6	V
$I_{DD(pd)}$	supply current in power-down mode	V_{DD} = 3.3 V; cards inactive; XTAL oscillator stopped	–	–	350	µA
		V_{DD} = 3.3 V; cards active at V_{CC} = 5 V; CLK stopped; XTAL oscillator stopped	–	–	3	mA
$I_{DD(sm)}$	supply current in sleep mode	cards powered at 5 V but clock stopped	–	–	5.5	mA
$I_{DD(om)}$	supply current in operating mode	V_{DD} = 3.3 V; f_{XTAL} = 20 MHz; $V_{CC1} = V_{CC2}$ = 5 V; $I_{CC1} + I_{CC2}$ = 80 mA	–	–	315	mA
V_{CC}	output card supply voltage	including static loads (5 V card)	4.75	5.0	5.25	V
		with 40 nC dynamic loads on 200 nF capacitor (5 V card)	4.6	–	5.4	V
		including static loads (3 V card)	2.78	–	3.22	V
		with 24 nC dynamic loads on 200 nF capacitor (3 V card)	2.75	–	3.25	V
I_{CC}	output card supply current	operating; 5 V card	–	–	65	mA
		operating; 3 V card	–	–	50	mA
		overload detection	–	100	–	mA
$I_{CC1} + I_{CC2}$	sum of both cards currents		–	–	80	mA
SR	slew rate on V_{CC} (rise and fall)	$C_{L(max)}$ = 300 nF	0.05	0.16	0.22	V/µs
t_{deact}	deactivation cycle duration		–	–	150	µs
t_{act}	activation cycle duration		–	–	225	µs
f_{xtal}	crystal frequency		4	–	27	MHz
f_{op}	operating frequency	external frequency applied to pin XTAL1	0	–	25	MHz
T_{amb}	ambient temperature		–25	–	+85	°C

BLOCK DIAGRAM

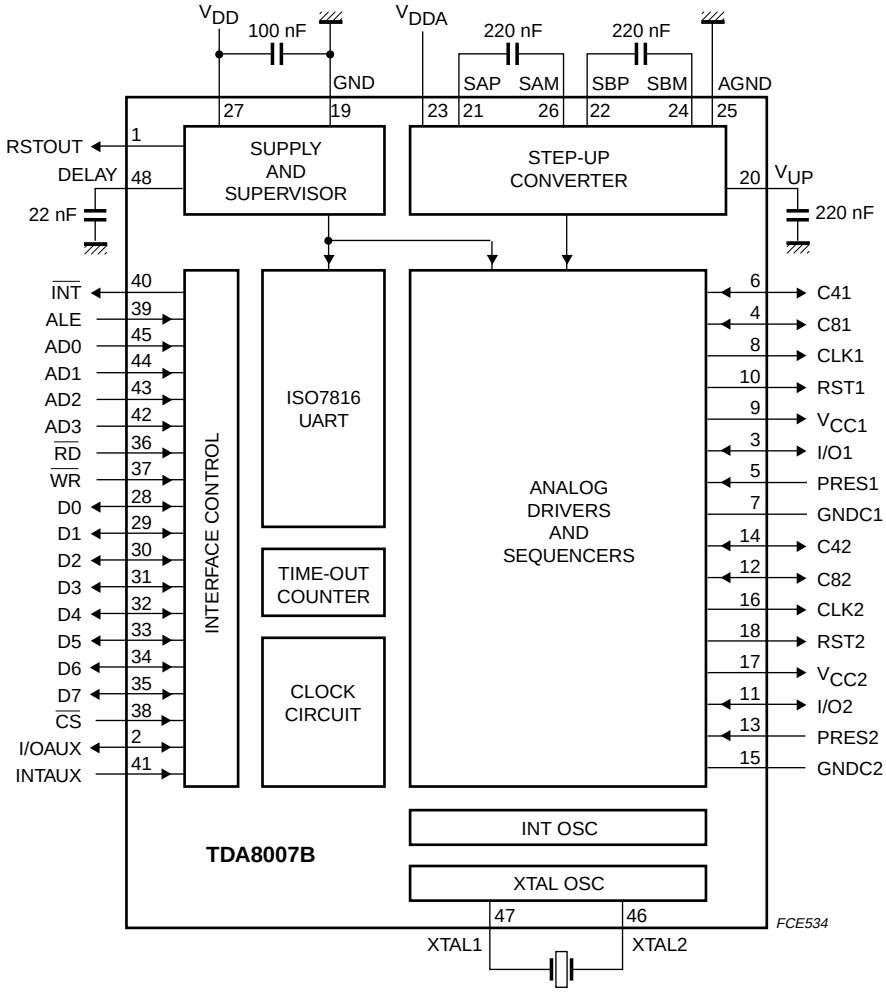


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RSTOUT	1	open-drain output for resetting external chips
I/OAUX	2	input or output for an I/O line issued of an auxiliary smart card interface
I/O1	3	data line to/from card 1 (ISO C7 contact)
C81	4	auxiliary I/O for ISO C8 contact (synchronous cards for instance) for card 1
PRES1	5	card 1 presence contact input (active HIGH or LOW by mask option)
C41	6	auxiliary I/O for ISO C4 contact (synchronous cards for instance) for card 1
GNDC1	7	ground for card 1
CLK1	8	clock output to card 1 (ISO C3 contact)
V_{CC1}	9	card 1 supply output voltage (ISO C1 contact)
RST1	10	card 1 reset output (ISO C2 contact)
I/O2	11	data line to/from card 2 (ISO C7 contact)
C82	12	auxiliary I/O for ISO C8 contact (synchronous cards for instance) for card 2
PRES2	13	card 2 presence contact input (active HIGH or LOW by mask option)
C42	14	auxiliary I/O for ISO C4 contact (synchronous cards for instance) for card 2
GNDC2	15	ground for card 2
CLK2	16	clock output to card 2 (ISO C3 contact)
V_{CC2}	17	card 2 supply output voltage (ISO C1 contact)
RST2	18	card 2 reset output (ISO C2 contact)
GND	19	ground connection
V_{UP}	20	output of the step-up converter
SAP	21	contact 1 for the step-up converter (connect a low ESR 220 nF capacitor between pins SAP and SAM)
SBP	22	contact 3 for the step-up converter (connect a low ESR 220 nF capacitor between pins SBP and SBM)
V_{DDA}	23	positive analog supply voltage for the step-up converter
SBM	24	contact 4 for the step-up converter (connect a low ESR 220 nF capacitor between pins SBP and SBM)
AGND	25	ground connection for the step-up converter
SAM	26	contact 2 for the step-up converter (connect a low ESR 220 nF capacitor between pins SAP and SAM)
V_{DD}	27	positive supply voltage
D0	28	data 0 or add 0
D1	29	data 1 or add 1
D2	30	data 2 or add 2
D3	31	data 3 or add 3
D4	32	data 4 or add 4
D5	33	data 5 or add 5
D6	34	data 6 or add 6
D7	35	data 7 or add 7
$\overline{RD}$	36	read selection signal (read or write in non-multiplexed configuration)

SYMBOL	PIN	DESCRIPTION
$\overline{WR}$	37	write selection signal (enable in case of non-multiplexed configuration)
$\overline{CS}$	38	chip select input (active HIGH or LOW)
ALE	39	address latch enable in case of multiplexed configuration (connect to V_{DD} in non-multiplexed configuration)
$\overline{INT}$	40	interrupt output (active LOW)
INTAUX	41	auxiliary interrupt input
AD3	42	register selection address 3
AD2	43	register selection address 2
AD1	44	register selection address 1
AD0	45	register selection address 0
XTAL2	46	connection pin for an external crystal
XTAL1	47	connection pin for an external crystal or input for an external clock signal
DELAY	48	connection pin for an external delay capacitor

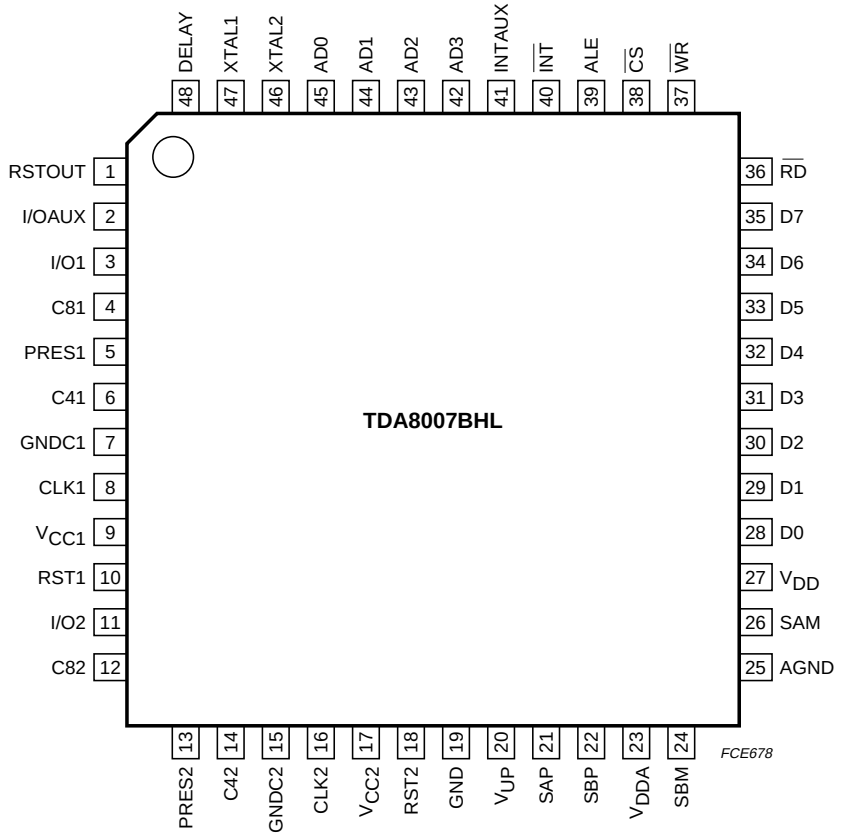


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Throughout this specification, it is assumed that the reader is aware of ISO 7816 norm terminology.

Interface control

The TDA8007B can be controlled via an 8-bit parallel bus (bits D0 to D7).

If a microcontroller with a multiplexed address/data bus (such as the 80C51) is used, then D0 to D7 may be directly connected to P0 to P7. When $\overline{CS}$ is LOW, the demultiplexing of address and data is performed internally using the ALE signal, a LOW pulse on pin $\overline{RD}$ allows the selected register to be read, a LOW pulse on pin $\overline{WR}$ allows the selected register to be written to. The TDA8007B automatically switches to the multiplexed bus configuration if a rising edge is detected on pin ALE. In this event, AD0 to AD3 play no role and may be tied to V_{DD} or GND. Using a 80C51 microcontroller, the TDA8007B is simply controlled with MOVX instructions.

If ALE is tied to V_{DD} or GND, then the TDA8007B will be in the non-multiplexed configuration. In this case, the address bits are external pins AD0 to AD3, $\overline{RD}$ is the read/$\overline{write}$ control signal, and $\overline{WR}$ is a data write or read active LOW enable signal.

In both configurations, the TDA8007B is selected only when $\overline{CS}$ is LOW. $\overline{INT}$ is an active LOW interrupt signal.

In non-multiplexed bus configuration, $\overline{CS}$ and $\overline{EN}$ play the same role.

In read operations (RD/$\overline{WR}$ is HIGH), the data corresponding to the chosen address is available on the bus when both $\overline{CS}$ and $\overline{EN}$ are LOW.

In write operations, the data present on the bus is written when signals RD/$\overline{WR}$, $\overline{CS}$ and $\overline{EN}$ become LOW.

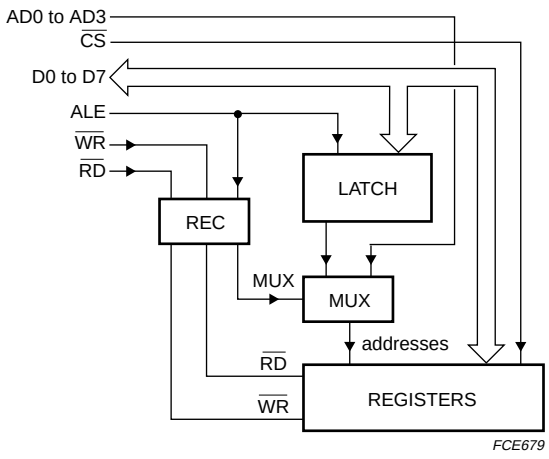


Fig.3 Multiplexed bus recognition.

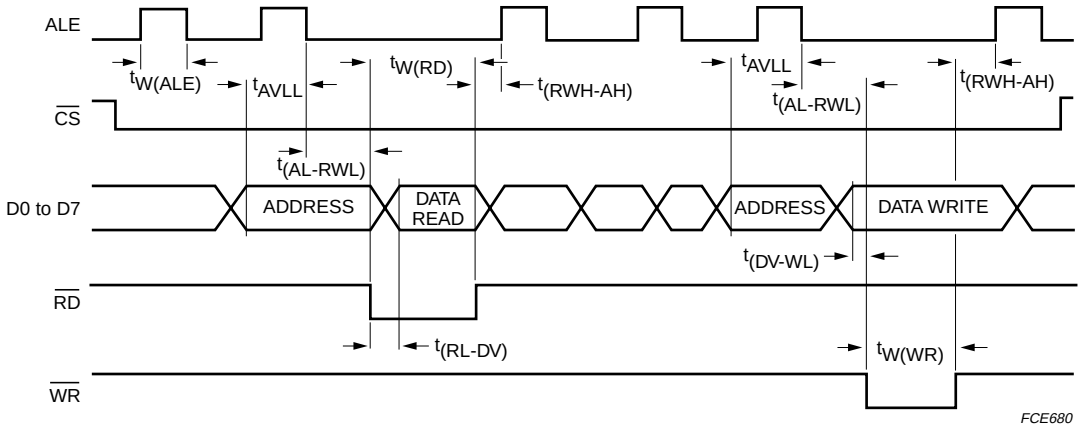


Fig.4 Control with multiplexed bus.

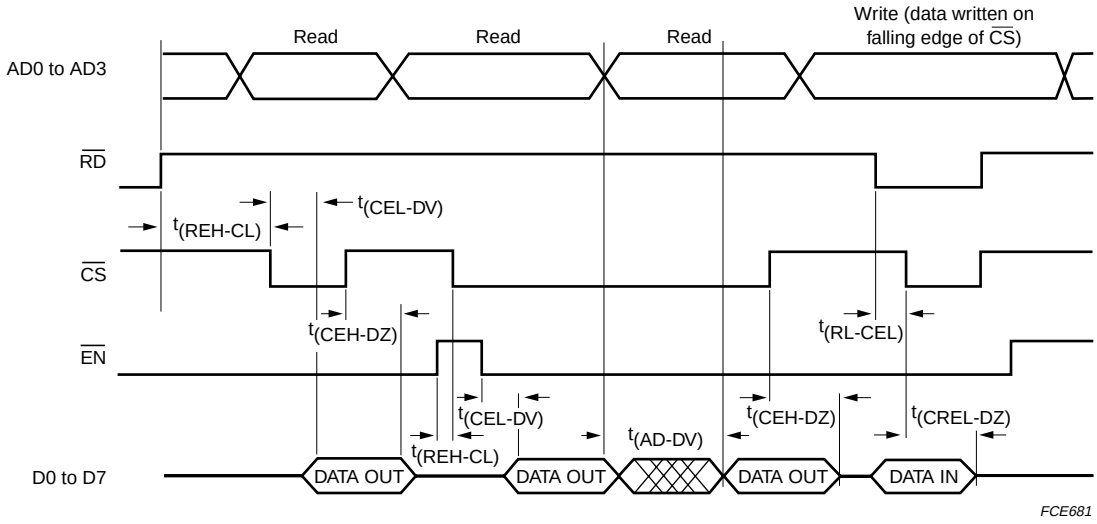


Fig.5 Control with non-multiplexed bus.

Control registers

The TDA8007B has 2 complete analog interfaces which can drive card 1 and card 2. The data to and from these 2 cards share the same ISO UART. The data to and from a third card (card 3), externally interfaced (with a TDA8002 or TDA8003 for example), may also share the same ISO UART.

Cards 1, 2 and 3 have dedicated registers for setting the parameters of the ISO UART; Programmable Divider Register (PDR), Guard Time Register (GTR), UART Configuration Register 1 (UCR1), UART Configuration Register 2 (UCR2) and Clock Configuration Register (CCR).

Cards 1 and 2 also have dedicated registers for controlling their power and clock configuration. The Power Control Register (PCR) for card 3, is controlled externally. The PCR is also used for writing or reading on the auxiliary card contacts C4 and C8.

Card 1, 2 or 3 can be selected via the Card Select Register (CSR). When one card is selected, the corresponding parameters are used by the ISO UART. The CSR also contains one bit for resetting the ISO UART (active LOW). This bit is reset after Power-on, and must be set to HIGH before starting with any one of the cards. It may be reset by software when necessary.

When the specific parameters of the cards have been programmed, the UART may be used with the following registers: UART Receive Register (URR), UART Transmit Register (UTR), UART Status Register (USR) and Mixed Status Register (MSR). In reception mode, a FIFO of 1 to 8 characters may be used, and is configured with the FIFO Control Register (FCR).

The Hardware Status Register (HSR) gives the status of the supply voltage, of the hardware protections and of the card movements.

HSR and USR give interrupts on pin $\overline{INT}$ when some of their bits have been changed.

The MSR does not give interrupts and may be used in the polling mode for some operations; for this use, some of the interrupt sources within the USR and HSR may be masked.

A 24-bit time-out counter may be started to give an interrupt after a number of ETUs programmed into registers TOR1, TOR2 and TOR3. This will help the microcontroller in processing different real-time tasks (ATR, WWT, BWT, etc.) mainly if the microcontrollers and cards clock are asynchronous.

This counter is configured with a register Time-Out counter Configuration (TOC). It may be used as a 24-bit or as a 16 + 8 bits. Each counter can be set to start counting once data has been written, or on detection of a start bit on the I/O, or as auto-reload.

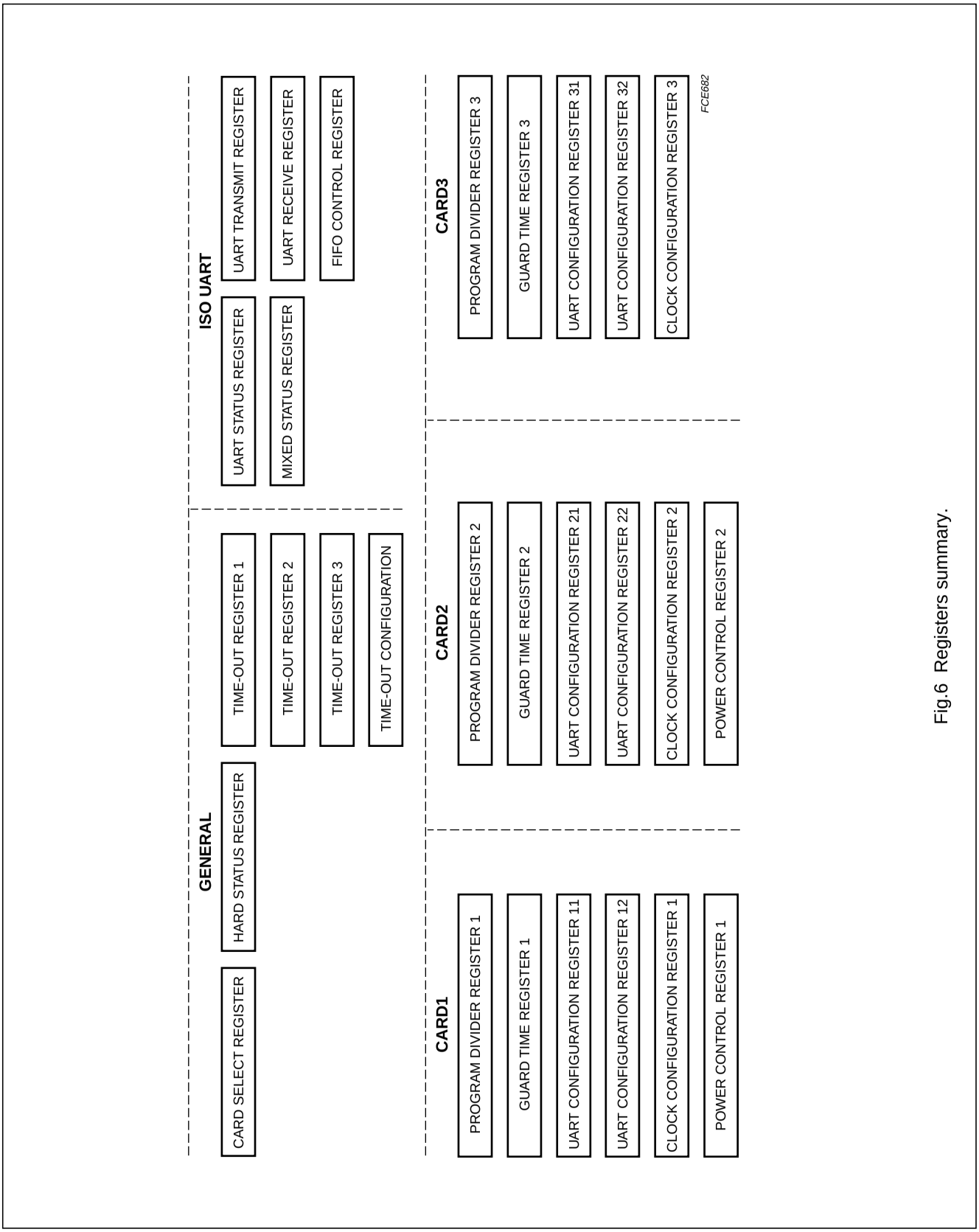


Fig.6 Registers summary.

GENERAL REGISTERS

The Card Select Register (see Table 1) is used for selecting the card on which the UART will act, and also to reset the ISO UART.

If SC1 = 1, then card 1 is selected; if SC2 = 1, then card 2 is selected, if SC3 = 1, then card 3 is selected. These bits must be set one at a time. After reset, card 1 is selected by default. The bit Reset ISO UART ($\overline{RIU}$) must be set to logic 1 by software before any action on the UART can take place. When reset, this bit resets all UART registers to their initial value.

It should be noted that access to card 3 is only possible once either card 1 or 2 has been activated.

The Hardware Status Register (see Table 2) gives the status of the chip after a hardware problem has been detected.

Presence Latch 1 (PRL1) and Presence Latch 2 (PRL2) are HIGH when a change has occurred on PR1 and PR2.

Supervisor Latch (SUPL) is HIGH when the supervisor has been activated.

Protection 1 (PRTL1) and Protection 2 (PRTL2) are HIGH when a default has been detected on card readers 1 and 2. (PRTL is the OR function of protection on V_{CC} and RST).

PTL is set if overheating has occurred.

INTAUXL is HIGH if the level on the INTAUX input has been changed.

When PRTL2, PRTL1, PRL2 or PRL1 or PTL is HIGH, then $\overline{INT}$ is LOW. The bits having caused the interrupt are cleared when the HSR has been read-out. The same occurs with bit INTAUXL if not disabled.

At power-on, or after a supply voltage dropout, SUPL is set and $\overline{INT}$ is LOW. $\overline{INT}$ will return HIGH at the end of the alarm pulse on pin RSTOUT. SUPL will be reset only after a status register read-out outside the ALARM pulse (see Fig.7).

In case of emergency deactivation (by PRTL1, PRTL2, SUPL, PRL2, PRL1 or PTL), the START bit is automatically reset by hardware.

The three registers TOR1, TOR2 and TOR3 form a programmable 24-bit ETU counter, or two independant counters (one 16-bit and one 8-bit).

The value to load in TOR1, 2 and 3 is the number of ETUs to count.

The TOC register is used for setting different configurations of the time-out counter as given in Table 7 (all other configurations are undefined).

Table 1 Card select register (write and read); address: 0
(all significant bits are cleared after reset, except for SC1 which is set)

CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
not used	not used	not used	not used	$\overline{RIU}$	SC3	SC2	SC1

Table 2 Hardware status register (read only); address: F
(all significant bits are cleared after reset, except for SUPL which is set within the RSTOUT pulse)

HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0
not used	PRTL2	PRTL1	SUPL	PRL2	PRL1	INTAUXL	PTL

Table 3 Time-out register 1 (write only); address: 9 (all bits are cleared after reset)

TO17	TO16	TO15	TO14	TO13	TO12	TO11	TO10
TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0

Table 4 Time-out register 2 (write only); address: A (all bits are cleared after reset)

TO27	TO26	TO25	TO24	TO23	TO22	TO21	TO20
TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8

Table 5 Time-out register 3 (write only); address: B (all bits are cleared after reset)

TO37	TO36	TO35	TO34	TO33	TO32	TO31	TO30
TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16

Table 6 Time-out configuration register (read and write); address: 8 (all bits are cleared after reset)

TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0
TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0

Table 7 Time-out counter configurations

TOC	OPERATING MODE
00	all counters are stopped
61	Counter 1 is stopped, and counters 3 and 2 form a 16-bit counter. Counting the value stored in TOR3 and TOR2 is started after 61 is written in the TOC. An interrupt is given, and bit TO3 is set within the USR when the terminal count is reached. The counter is stopped by writing 00 in the TOC.
65	Counter 1 is an 8-bit auto reload counter, and counters 3 and 2 form a 16-bit counter. Counter 1 starts counting the content of TOR1 on the first start bit (reception or transmission) detected on I/O after 65 is written in the TOC. When counter 1 reaches its terminal count, an interrupt is given, bit TO1 in the USR is set, and the counter automatically restarts the same count until it is stopped. It is not allowed to change the content of TOR1 during a count. In this mode, the accuracy of counter 1 is $\pm$0.5 ETU. Counters 3 and 2 are wired as a single 16-bit counter and starts counting the value TOR3 and TOR2 when 65 is written in the TOC. When the counter reaches its terminal count, an interrupt is given and bit TO3 is set within the USR. Both counters are stopped when 00 is written in the TOC.
68	Counters 3, 2 and 1 are wired as a single 24-bit counter. Counting the value stored in TOR3, TOR2 and TOR1 is started after 68 is written in the TOC. The counter is stopped by writing 00 in the TOC. It is not allowed to change the content of TOR3, TOR2 and TOR1 within a count.
7C	Counters 3, 2 and 1 are wired as a single 24-bit counter. Counting the value stored in TOR3, TOR2 and TOR1 on the first start bit detected on I/O (reception or transmission) after the value has been written. It is possible to change the content of TOR3, TOR2 and TOR1 during a count; the current count will not be affected and the new count value will be taken into account at the next start bit. The counter is stopped by writing 00 in the TOC. In this configuration TOR3, TOR2 and TOR1 must not be all zero.
E5	Same configuration as TOC = 65, except that counter 1 will be stopped at the end of the 12th ETU following the first start bit detected after E5 has been written in the TOC.

The time-out counter is very useful for processing the clock counting during ATR, the Work Waiting Time, or the waiting times defined in T = 1 protocol. It should be noted that the 200 and 400 CLK counter used during ATR is done by hardware when the start session is set; a specific hardware controls functionality BGT in T = 1 protocol, and a specific register is available for processing the extra guard time.

The possible use of the counters is as follows:

- ATR (cold reset):
  - Before activation; TOR1 = C0H, TOR2 = 6EH, TOR3 = 0 and TOC = 65. Once activated, timer 2 + 3 will count 40920 clock pulses before giving an interrupt.
  - On interrupt; TOR2 = 76H and TOC = 65. If a character is received from the card before the timeout, then counter 1 will be enabled. Counter 1 will give one interrupt every 192 ETUs, so the software will count 100 times to verify that the ATR is finished before 19200 ETUs. The UART will give an interrupt with bit Buffer Full (BF) at 10.5 ETUs after the start bit.
  - On interrupt; TOR3 = 25H, TOR2 = 80H and TOC = 65. Counter 1 keeps on counting 100×192 ETUs, while counter 2 and 3 counts 9600 ETUs. This sequence is repeated until the character before the last one of the ATR.
  - On interrupt TOR3 = 25H, TOR2 = 80H and TOC = E5. Timer 1 will be automatically stopped at the end of the last character of the ATR, allowing a count of 19200 ETUs.
  - On interrupt TOC = 00.
- Work Waiting Time (WWT) in T = 0 protocol;
  - Before sending the first command to the card TOR1, TOR2 and TOR3 should be loaded with the correct $960 \times WI \times D$ value and TOC = 7C
  - Timer 3, 2 and 1 will count the WWT between each start bit
- Character Waiting Time (CWT) and Block Waiting Time (BWT) in T = 1 protocol:
  - Before sending the first block to the card, TOR3, TOR2 and TOR1 should be loaded with the CWT and TOC = 7C
  - Timer 3 + 2 + 1 will count the CWT between each start bit
  - Before the end of the block, TOR3, TOR2 and TOR1 should be loaded with the BWT
  - Timer 3 + 2 + 1 will count the BWT from the last start bit of the sent block
  - After reception of the first character of the block from the card, TOR3, TOR2 and TOR1 should be loaded with the CWT
  - Timer 3 + 2 + 1 will count the CWT between each received start bit
  - And so on.
- Before and after CLOCK STOP (example, where ETU = 372 clock pulses):
  - After the last received character on I/O, TOR3 = 0, TOR2 = 6 and TOC = 61
  - Timer 3 + 2 will start counting 2232 clock pulses before giving an interrupt
  - On interrupt, the software may stop the clock to the card
  - When it is necessary to restart the clock, TOR3 = 0, TOR2 = 2, TOC = 61 and restart the clock
  - Timer 3 + 2 gives an interrupt at 744 clock pulses, and then the software can send the first command to the card.

ISO UART REGISTERS

When the microcontroller wants to transmit a character to the selected card, it writes the data in direct convention in the UART Transmit Register (see Table 8). The transmission:

- Starts at the end of writing (on the rising edge of $\overline{WR}$) if the previous character has been transmitted and if the extra guard time has expired; or
- Starts at the end of the extra guard time if this one has not expired; or
- Does not start if the transmission of the previous character is not completed.

In the case of a synchronous card (bit SAN within UCR2 is set), only D0 is relevant, and is copied on the I/O of the selected card. When the microcontroller wants to read data from the card it reads it from the UART Receive Register (see Table 9) in direct convention.

In case of a synchronous card, only D0 is relevant and is a copy of the state of the selected card I/O.

When needed, this register may be tied to a FIFO whose length ‘n’ is programmable between 1 and 8.

If n > 1, then no interrupt is given until the FIFO is full. The microcontroller may empty the FIFO at any time.

Error management in protocol:

- T = 0:

In the event of a parity error, the received byte is not stored in the FIFO, and the error counter is incremented. The error counter is programmable between 1 and 8. When the programmed number is reached, bit PE is set in the status register USR and $\overline{INT}$ goes LOW. The error counter must be reprogrammed to the desired value after its count has been reached.

- T = 1:

In the event of a parity error, the character is loaded in the FIFO, and bit PE is set whatever the programmed value in parity error counter.

When the FIFO is full, bit RBF in the status register USR is set. This bit is reset when at least one character has been read from the URR.

When the FIFO is empty, bit FE is set as long as no character has been received.

The Mixed Status Register (see Table 10) relates the status of pin INTAUX, the cards presence contacts PR1 and PR2, the BGT counter, the FIFO empty indication and the transmit/receive ready indicator TBE/RBF.

Bit INTAUX is set when the level on pin INTAUX is HIGH, it is reset when the level is LOW.

Bit BGT is linked with a 22 ETU counter, which is started at every start bit on the I/O. Bit BGT is set if the count is finished before the next start bit. This helps to verify that the card has not answered before 22 ETUs after the last transmitted character, or not transmitting a character before 22 ETUs after the last received character.

PR1 is HIGH when card 1 is present, PR2 is HIGH when card 2 is present.

FE is set when the reception FIFO is empty. It is reset when at least one character has been loaded in the FIFO.

Bit TBE/RBF (Transmit Buffer Empty/Receive Buffer Full) is set when:

- Changing from reception mode to transmission mode
- A character has been transmitted by the UART
- The reception FIFO is full.

Bit TBE/RBF is reset after Power-on or after one of the following:

- When bit $\overline{RIU}$ is reset
- When a character has been written to the UTR
- When at least one character has been read in the FIFO
- When changing from transmission mode to reception mode.

No bits within the MSR act upon $\overline{INT}$:

- The FIFO Control Register bits are given in Table 11, FL2, FL1 and FL0 determine the depth of the FIFO (000 = length 1, 111 = length 8).

PEC2, PEC1 and PEC0 determine the number of parity errors before setting bit PE in the USR and pulling $\overline{INT}$ LOW; 000 indicates that if only one parity error has occurred, bit PE is set; 111 indicates that bit PE will be set after 8 parity errors.

PEC2, PEC1 and PEC0 need to be reprogrammed to the desired value after bit PE has been set.

In protocol T = 0:

- If a correct character is received before the programmed error number is reached the error counter will be reset.
- If the programmed number of allowed parity errors is reached, bit PE in the USR will be set as long as the USR has not been read.

In protocol T = 1:

- The error counter has no action (bit PE is set at the first wrong received character).
- The UART Status Register (see Table 12) is used by the microcontroller to monitor the activity of the ISO UART and that of the time-out counter.

Transmission Buffer Empty (TBE) is HIGH when the UART is in transmission mode, and when the microcontroller may write the next character to transmit in the UTR. It is reset when the microcontroller has written data in the transmit register or when bit T/R within UCR1 has been reset either automatically or by software.

After detection of a parity error in transmission, it is necessary to wait 13 ETUs before rewriting the character which has been Not ACKnowledged (NAK) by the card.

Reception Buffer Full (RBF) is HIGH when the FIFO is full. The microcontroller may read some of the characters in the URR, which clears bit RBF.

TBE and RBF share the same bit within the USR (when in transmission mode, the relevant bit is TBE; when in reception mode, it is RBF).

Framing Error (FER) is HIGH when the I/O was not in the high-impedance state at 10.25 ETUs after a start bit. It is reset when the USR has been read-out.

Overrun (OVR) is HIGH if the UART has received a new character whilst the FIFO was full. In this case, at least one character has been lost.

In protocol T = 0: Parity Error (PE) is HIGH if the UART has detected a number of received characters with parity errors equal to the number written in PEC2, PEC1 and PEC0 or if a transmitted character has been NAKed by the card.

In protocol T = 0: a character received with a parity error is not stored in the FIFO (the card is supposed to repeat this character).

In protocol T = 1: a character with a parity error is stored in the FIFO and the parity error counter is not active.

Early Answer (EA) is HIGH if the first start bit on the I/O during ATR has been detected between 200 and 384 CLK pulses (all activities on the I/O during the 200 first CLK pulses with RST LOW or HIGH are not taken into account). These 2 features are reinitialized at each toggling of RST.

Bit TO1 is set when counter 1 has reached its terminal count.

Bit TO3 is set when counter 3 has reached its terminal count.

If any of the status bits FER, OVR, PE, EA, TO1 or TO3 are set then $\overline{INT}$ will go LOW. The bit having caused the interrupt is reset at the end of a read operation of the USR. If TBE/RBF is set, and if the mask bit DISTBE/RBF within USR2 is not set, then $\overline{INT}$ will also be LOW. TBE/RBF is reset when data has been written to the UTR, when data has been read from the URR, or when changing from transmission mode to reception mode.

Table 8 UART transmit register (write only); address: D (all bits are cleared after reset)

UT7	**UT6**	**UT5**	**UT4**	**UT3**	**UT2**	**UT1**	**UT0**
UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0

Table 9 UART receive register (read only); address: D (all bits are cleared after reset)

UR7	**UR6**	**UR5**	**UR4**	**UR3**	**UR2**	**UR1**	**UR0**
UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0

Table 10 Mixed status register (read only); address: C
(bits TBE, RBF and BGT are cleared after reset; bit FE is set after reset)

MS7	**MS6**	**MS5**	**MS4**	**MS3**	**MS2**	**MS1**	**MS0**
not used	FE	BGT	not used	PR2	PR1	INTAUX	TBE/RBF

Table 11 FIFO control register (write only); address: C (all relevant bits are cleared after reset)

FC7	**FC6**	**FC5**	**FC4**	**FC3**	**FC2**	**FC1**	**FC0**
not used	PEC2	PEC1	PEC0	not used	FL2	FL1	FL0

Table 12 UART status register (read only); address: E (all bits are cleared after reset)

US7	**US6**	**US5**	**US4**	**US3**	**US2**	**US1**	**US0**
TO3	not used	TO1	EA	PE	OVR	FER	TBE/RBF

CARD REGISTERS

When cards 1 2 or 3 are selected, then the following registers may be used for programming some specific parameters.

The Programmable Divider Register (see Table 13) is used for counting the cards clock cycles forming the ETU. It is an auto-reload 8-bit counter decounting from the programmed value down to 0.

Table 13 Programmable Divider Register (PDR1, 2 and 3) (read and write); address: 2 (all bits are cleared after reset)

PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The UART Configuration Register 2 bits are given in Table 14. If bit PSC is set to logic 1, then the prescaler value is 32. If bit PSC is set to logic 0, then the prescaler value is 31. One ETU will last a number of card clock cycles equal to prescaler x PDR. All baud rates specified in ISO 7816 norm are achievable with this configuration.

Table 14 UART configuration register 2 (UCR21, 22 and 23) (read and write); address: 3 (all relevant bits are cleared after reset)

UC27	UC26	UC25	UC24	UC23	UC22	UC21	UC20
not used	DISTBE/RBF	DISAUX	PDWN	SAN	$\overline{\text{AUTOCONV}}$	CKU	PSC

Table 15 Baud rates with a 3.58 MHz card clock frequency (31;12 means prescaler set to 31 and PDR set to 12)

D	F											
	0	1	2	3	4	5	6	9	10	11	12	13
1	31;12 9600	31;12 9600	31;18 6400	31;24 4800	31;36 3200	31;48 2400	31;60 1920	32;16	32;24	32;32	32;48	32;64
2	31;6 19200	31;6 19200	31;9 12800	31;12 9600	31;18 6400	31;24 4800	31;30 3840	32;8	32;12	32;16	32;24	32;32
3	31;3 38400	31;3 38400		31;6 19200	31;9 12800	31;12 9600	31;15 7680	32;4	32;6	32;8	32;12	32;16
4				31;3 38400		31;6 19200		32;2	32;3	32;4	32;6	32;8
5						31;3 38400		32;1		32;2	32;3	32;4
6										32;1		32;2
8	31;1 115200	31;1 115200		31;2 57600	31;3 38400	31;4 28800	31;5 23040		32;2		32;4	
9							31;3 38400					

For other baud rates than those given in Table 15, there is the possibility to set bit CKU (clock UART) to logic 1. In this case, the ETU will last half of the formula given above.

If bit $\overline{\text{AUTOCONV}}$ is set, then the convention is set by software using bit CONV in the UART Configuration Register. If it is reset, then the configuration is automatically detected on the first received character whilst the Start Session (SS) bit is set.

Synchronous/$\overline{\text{Asynchronous}}$ (SAN) is set by software if a synchronous card is expected. The UART is then bypassed, and only bit 0 in the URR and UTR is connected to the I/O. In this case the CLK is controlled by bit SC in the CCR.

When Power-down mode (PDWN) is set by software, the crystal oscillator is stopped. This mode allows low consumption in applications where it is required. During this mode, it is not possible to select another card other than the currently selected one. There are 5 ways of escaping from the Power-down mode:

1. Insert card 1 or card 2
2. Withdraw card 1 or card 2
3. Select the TDA8007B by resetting $\overline{\text{CS}}$ (this assumes that the TDA8007B had been deselected after setting Power-down mode)
4. INTAUXL has been set due to a change on pin INTAUX
5. If $\overline{\text{CS}}$ is permanently set to LOW, reset bit PDWN by software.

After any of these 5 events, the TDA8007B will leave the Power-down mode, and will pull $\overline{\text{INT}}$ LOW when it is ready to communicate with the system microcontroller. The system microcontroller may then read the status registers, and $\overline{\text{INT}}$ will return HIGH (if the system microcontroller has woken the TDA8007B by reselecting it, then no bits will be set in the status registers).

If the Disable AUX (DISAUX) interrupt bit in UCR2 is set, then a change on INTAUX will not generate an interrupt (but bit INTAUXL in the HSR will be set; it is therefore necessary to read the HSR before a DISAUX reset to avoid an interrupt by INTAUXL). To avoid an interrupt during a change of card, it is better to set the DISAUX bit in UCR2 for both cards.

If the Disable TBE/RBF (DISTBE/RBF) interrupt bit is set, then reception or transmission of a character will not generate an interrupt:

- This feature is useful for increasing communication speed with the card; in this case, a copy of the TBE/RBF bit within the MSR must be polled (and not the original) in order not to loose priority interrupts which can occur in the USR.
- The Guard Time Register (see Table 17) is used for storing the number of guard ETUs given by the card during ATR. In transmission mode, the UART will wait this number of ETUs before transmitting the character stored in the UTR. In T = 1 protocol, when GTR = FF means operation at 11 ETUs. In protocol T = 0, GTR = FF means operation at 12 ETUs.
- The UART Configuration Register (see Table 18) is used for setting the parameters of the ISO UART.

The Convention (CONV) bit is set if the convention is direct. CONV is either automatically written by hardware according to the convention detected during ATR, or by software if the bit $\overline{\text{AUTOCONV}}$ is set.

The SS bit is set before ATR for automatic convention detection and early answer detection (this bit must be reset by software after reception of a correct initial character).

The Last Character to Transmit (LCT) bit is set by software before writing the last character to be transmitted in the UTR. It allows automatic change to reception mode. It is reset by hardware at the end of a successful transmission.

The Transmit/Receive (T/R) bit is set by software for transmission mode. A change from logic 0 to logic 1 will set bit TBE in the USR. Bit T/R is automatically reset by hardware if the LCT bit has been used before transmitting the last character.

The Protocol (PROT) bit is set if the protocol type is asynchronous T = 1. If PROT = 0, the protocol is T = 0.

The Flow Control (FC) bit is set if flow control is used (not described in this specification).

If the Force Inverse Parity (FIP) bit is set to HIGH the UART will NAK a correctly received character, and will transmit characters with wrong parity bits.

Clock Configuration Register (see Table 19):

- For cards 1 and 2, the CCR defines the clock for the selected card.
- For cards 1, 2 and 3 it defines the clock to the ISO UART. It should be noted that if bit CKU in the prescaler register of the selected card is set, then the ISO UART is clocked at twice the frequency of the card, which allows baud rates not foreseen in ISO 7816 norm to be reached.

In case of an asynchronous card, the Clock Stop (CST) bit defines whether the clock to the card is stopped or not.

If CST is set, then CLK is stopped LOW if SHL = 0, and HIGH if SHL = 1.

If CST is reset, then CLK is determined by bits AC0, AC1 and AC2; see Table 16. All frequency changes are synchronous, thus ensuring that no spike or unwanted pulse widths occur during changes.

Table 16 CLK value for an asynchronous card

AC2	AC1	AC0	CLK
0	0	0	$\frac{1}{2}$XTAL
0	0	1	$\frac{1}{2}$XTAL
0	1	0	$\frac{1}{4}$XTAL
0	1	1	$\frac{1}{8}$XTAL
1	0	0	$\frac{1}{2}f_{int}$
1	0	1	$\frac{1}{2}f_{int}$
1	1	0	$\frac{1}{2}f_{int}$
1	1	1	$\frac{1}{2}f_{int}$

When switching from XTAL/n to $\frac{1}{2}f_{int}$ or vice verse, only bit AC2 must be changed (AC1 and AC0 must remain the same). When switching from XTAL/n or $\frac{1}{2}f_{int}$ to CLK STOP or vice verse, only bits CST and SHL must be changed.

When switching from XTAL/n to $\frac{1}{2}f_{int}$ or vice verse, a maximum delay of 200 µs can occur between the command and the effective frequency change on CLK (the fastest switching time is from $\frac{1}{2}$XTAL to $\frac{1}{2}f_{int}$ or vice verse, the best for duty cycle is from $\frac{1}{8}$XTAL to $\frac{1}{2}f_{int}$ or vice verse).

It is necessary to wait the maximum delay time before reactivating from Power-down mode.

In the event of a synchronous card, then the CLK contact is the copy of the value written in Synchronous Clock (SC). In reception mode, the data from the card is available to UR0 after a read operation of the URR; in transmission mode, the data is written on the I/O line of the card when the UTR has been written to and remains unchanged when another card is selected.

The Power Control Register (PCR), see Table 20:

- Starts or stops card sessions.
- Reads or writes on auxiliary card contacts C4 and C8.
- Is available only for cards 1 or 2.

If the microcontroller sets START to logic 1, then the selected card is activated (see Section “Activation sequence”). If the microcontroller resets START to logic 0, then the card is deactivated (see Section “Deactivation sequence”). START is automatically reset in case of emergency deactivation.

If 3 V/5 V is set to logic 1, then V_{CC} is 3 V. If 3 V/5 V is set to logic 0, then V_{CC} is 5 V.

When the card is activated, RST is the copy of the value written in RSTIN.

If 1.8 V is set, then V_{CC} = 1.8 V: It should be noted that no specification is guaranteed at this voltage.

When writing to the PCR, C4 will output the value written to PCR4, and C8 the value written to PCR5. When reading from the PCR, PCR4 will store the value on C4, and PCR5 the value on C8.

Table 17 Guard time register (GTR1, 2 and 3) (read and write); address: 5 (all bits are cleared after reset)

GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0
GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0

Table 18 UART configuration register 1 (UCR11, 12 and 13) (read and write); address: 6 (all relevant bits are cleared after reset)

UC7	UC6	UC5	UC4	UC3	UC2	UC1	UC0
not used	FIP	FC	PROT	T/R	LCT	SS	CONV

Table 19 Clock configuration register (CCR1, 2 and 3) (read and write); address: 1 (all bits are cleared after reset)

CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
not used	not used	SHL	CST	SC	AC2	AC1	AC0

Table 20 Power control register (PCR1 and 2) (read and write); address: 7 (all relevant bits are cleared after reset)

PCR7	PCR6	PCR5	PCR4	PCR3	PCR2	PCR1	PCR0
not used	not used	C8	C4	1V8	RSTIN	3V/5V	START

Table 21 Register summary

NAME	ADDR	R/W	7	6	5	4	3	2	1	0	VALUE AT RESET
CSR	00	R/W	not used	not used	not used	not used	$\overline{\text{RIU}}$	SC3	SC2	SC1	XXXX0000
HSR	0F	R	not used	PRTL2	PRTL1	SUPL	PRL2	PRL1	INTAUXL	PTL	X0010000
MSR	0C	R	not used	FE	BGT	not used	PR2	PR1	INTAUX	TBE/RF	X10XXXX0
TOR1	09	W	TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0	00000000
TOR2	0A	W	TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8	00000000
TOR3	0B	W	TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16	00000000
TOC	08	R/W	TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0	00000000
UTR	0D	W	UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0	00000000
URR	0D	R	UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0	00000000
FCR	0C	W	not used	PEC2	PEC1	PEC0	not used	FL2	FL1	FL0	X000X000
USR	0E	R	TO3	not used	TO1	EA	PE	OVR	FER	TBE/RBF	0X000000
PDR	02	R/W	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	00000000
UCR2	03	R/W	not used	DISTBE/RBF	DISAUX	PDWN	SAN	$\overline{\text{AUTOC}}$	CKU	PSC	X0000000
GTR	05	R/W	GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0	00000000
UCR1	06	R/W	not used	FIP	FC	PROT	T/R	LCT	SS	CONV	X0000000
CCR	01	R/W	not used	not used	SHL	CST	SC	AC2	AC1	AC0	00000000
PCR	07	R/W	not used	not used	C8	C4	1V8	RSTIN	3V/5V	START	XX110000

Supply

The circuit operates within a supply voltage range of 2.7 to 6 V. The supply pins are V_{DD}, V_{DDA}, GND and AGND. Pins V_{DDA} and AGND supply the analog drivers to the cards and have to be externally decoupled because of the large current spikes that the cards and the step-up converter can create. Pins V_{DD} and GND supply the rest of the chip. An integrated spike killer ensures that the contacts to the cards remain inactive during power-up or power-down. An internal voltage reference is generated which is used within the step-up converter, the voltage supervisor and the V_{CC} generators.

The voltage supervisor generates an alarm pulse, whose length is defined by an external capacitor tied to pin DELAY, when V_{DD} is too low to ensure proper operation (1 ms per 1 nF typical).

This pulse may be used as a reset pulse by the system microcontroller (pin RSTOUT, active HIGH). It is also used in order to either block any spurious noise on card contacts during the microcontrollers reset, or to force an automatic deactivation of the contacts in the event of supply dropout (see Sections “Activation sequence” and “Deactivation sequence”).

After Power-on, or after a voltage drop, bit SUPL is set within the Hardware Status Register (HSR) and remains set until HSR is read-out outside the alarm pulse. Pin $\overline{INT}$ is LOW for the duration that RSTOUT is active.

If needed, a complete reset of the chip may be performed by discharging the capacitor C_{DELAY}.

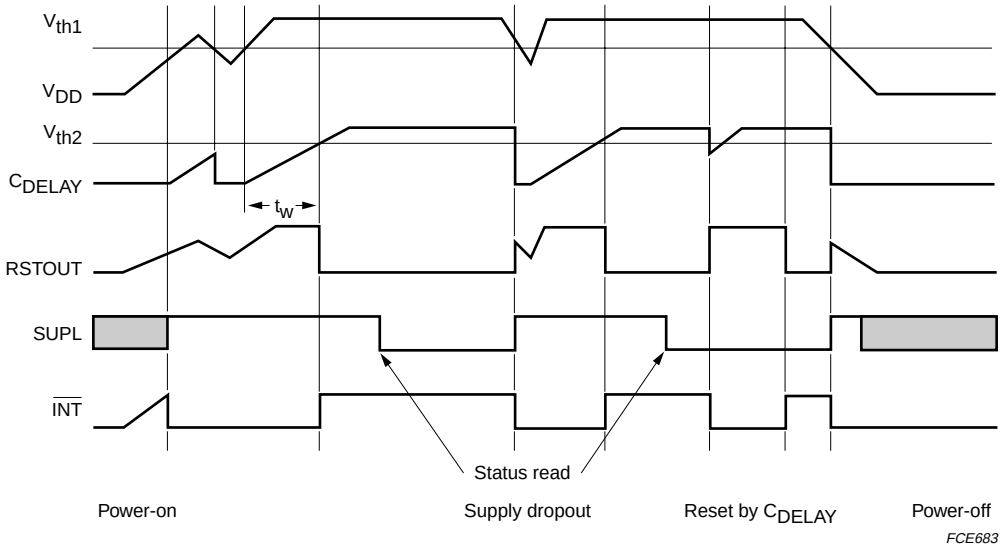


Fig.7 Voltage supervisor.

Step-up converter

Except for the V_{CC} generator and the other cards contacts buffers, the whole circuit is powered by V_{DD}, and V_{DDA}. If the supply voltage is 2.5 V, then a higher voltage is needed for the ISO contacts supply. When a card session is requested by the microcontroller, the sequencer first enables the step-up converter (a switched capacitors type) which is clocked by an internal oscillator at a frequency of approximately 2.5 MHz.

Suppose that V_{CC} is the maximum of V_{CC1} and V_{CC2}, then there are four possible situations:

1. V_{DD} = 3 V and V_{CC} = 3 V: in this case the step-up converter acts as a doubler with a regulation of approximately 4.0 V.
2. V_{DD} = 3 V and V_{CC} = 5 V: in this case the step-up converter acts as a tripler with a regulation of approximately 5.5 V.
3. V_{DD} = 5 V and V_{CC} = 3 V: in this case the step-up converter acts as a follower: V_{DD} is applied to V_{UP}.
4. V_{DD} = 5 V and V_{CC} = 5 V: in this case the step-up converter acts as a doubler with a regulation of approximately 5.5 V.

The recognition of the supply voltage is done by the TDA8007B at approximately 3.5 V.

The output voltage V_{UP} is fed to the V_{CC} generators. V_{CC} and GND are used as a reference for all other card contacts.

ISO 7816 security

The correct sequence during activation and deactivation of the cards is ensured by two specific sequencers, clocked by a division ratio of the internal oscillator.

Activation (START bit HIGH in PCR1 or PCR2) is only possible if the card is present (PRES active HIGH with an internal current source to GND) and if the supply voltage is correct (supervisor not active).

The presence of the cards is signalled to the microcontroller by the Hardware Status Register (HSR).

Bits PR1 or PR2 (in the USR) are set if card 1 or card 2 is present. PRL1 or PRL2 are set if PR1 or PR2 has toggled.

During a session, the sequencer performs an automatic emergency deactivation on one card in the event of card take-off, or short-circuit. Both cards are automatically deactivated in the event of a supply voltage drop, or overheating. The hardware status register is updated and the $\overline{INT}$ line falls, so that the system microcontroller is aware of what happened.

Activation sequence

When the cards are inactive, V_{CC}, CLK, RST, C4, C8 and I/O are LOW, with low-impedance with respect to GND. The step-up converter is stopped.

When everything is satisfactory (voltage supply, card present and no hardware problems), the system microcontroller may initiate an activation sequence on a present card.

After selecting the card and leaving the UART reset mode, and then configuring the necessary parameters for the counters and the UART, the START bit can be set within the PCR (t_0) (see Fig.8):

- The step-up converter is started (t_1); if one card was already active, then the step-up converter was already on and nothing more occurs at this step
- V_{CC} starts rising (t_2) from 0 to 5 V or 3 V with a controlled rise time of 0.17 V/µs (typ.)
- I/O rises to V_{CC} (t_3); C4 and C8 also rise if bits C4 and C8 within the PCR have been set to logic 1 (integrated 10 kΩ pull-up resistors to V_{CC})
- The CLK is sent to the card and RST is enabled (t_4).

After a number of CLK pulses that can be counted with the time-out counter, bit RSTIN may be set by software: RST will then rise to V_{CC}.

The sequencer is clocked by $\frac{1}{64}f_{int}$ which leads to a time interval of t = 25 µs (typ.). Thus $t_1 = 0$ to $\frac{1}{64}t$, $t_2 = t_1 + \frac{3}{2}t$, $t_3 = t_1 + \frac{7}{2}t$ and $t_4 = t_1 + 4t$.

Deactivation sequence

When the session is completed, the microcontroller resets START HIGH (t_{10}). The circuit then executes an automatic deactivation sequence (see Fig.9):

- The card is reset (RST falls LOW) (t_{11})
- The CLK is stopped (t_{12})
- I/O, C4 and C8 fall to 0 V (t_{13})
- V_{CC} falls to 0 V with typical 0.17 V/µs slew rate (t_{14})
- The step-up converter is stopped and CLK, RST, V_{CC} and I/O become low-impedance to GND (t_{15}) (if both cards are inactive).

$t_{11} = t_{10} + \frac{1}{64}t$, $t_{12} = t_{11} + \frac{1}{2}t$, $t_{13} = t_{11} + t$, $t_{14} = t_{11} + \frac{3}{2}t$ and $t_{15} = t_{11} + \frac{7}{2}t$.

t_{de} = time that V_{CC} needs to decrease to less than 0.4 V.

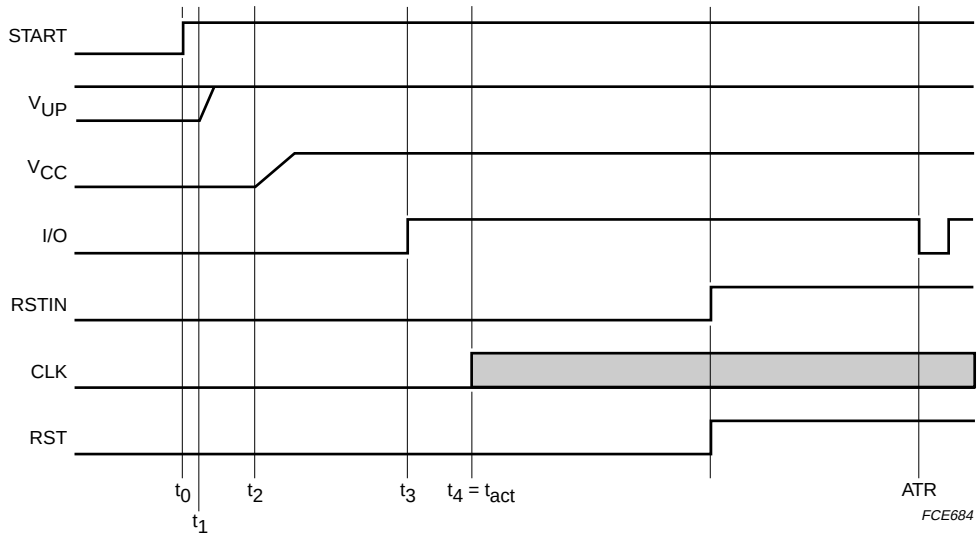


Fig.8 Activation sequence.

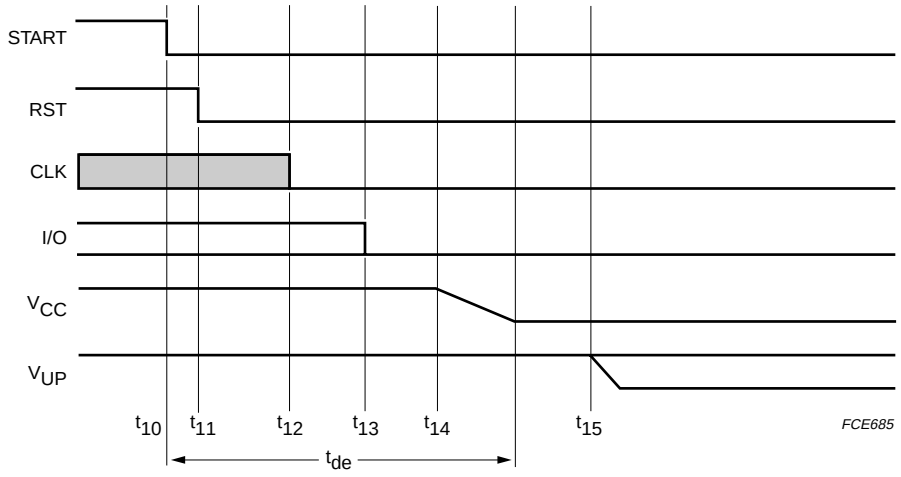


Fig.9 Deactivation sequence.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		–0.5	+6.5	V
V_{DD}	supply voltage		–0.5	+6.5	V
V_n	input voltage on all pins except S1, S2, S3, S4 and V_{UP}		–0.5	V_{DD} + 0.5	V
	input voltage on pins S1, S2, S3, S4 and VUP		–0.5	+7.5	V
I_{n1}	DC current into all pins except S1, S2, S3, S4 and V_{UP}		–5	+5	mA
I_{n3}	DC current from or to pins S1, S2, S3, S4 and V_{UP}		–200	+200	mA
P_{tot}	total power dissipation	T_{amb} = –20 to +85 °C	–	700	mW
T_{stg}	IC storage temperature		–55	+150	°C
T_j	junction temperature		–	125	°C
V_{es}	electrostatic discharge voltage				
	on pins I/O1, V_{CC1}, RST1, CLK1, GNDC1, PRES1, I/O2, V_{CC2}, RST2, CLK2, GNDC2 and PRES2		–6	+6	kV
	on pins C41, C42, C81 and C82		–5.5	+5.5	kV
	on pins D0 to D7		–1.8	+1.8	kV
	on other pins		–2	+2	kV

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	from junction to ambient	in free air	78	K/W

CHARACTERISTICS

V_{DD} = 3.3 V; V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.7	–	6.0	V
$I_{DD(pd)}$	supply current in Power-down mode	V_{DD} = 3.3 V; cards inactive; XTAL oscillator stopped	–	–	350	µA
		V_{DD} = 3.3 V; cards active at V_{CC} = 5 V; CLK stopped; XTAL oscillator stopped	–	–	3	mA
$I_{DD(sm)}$	supply current in Sleep mode	both cards powered, but with CLK stopped	–	–	5.5	mA
$I_{DD(om)}$	supply current in operating mode	I_{CC1} = 65 mA; I_{CC2} = 15 mA; f_{XTAL} = 20 MHz; f_{CLK} = 10 MHz; 5 V cards; V_{DD} = 2.7 V	–	–	315	mA
		I_{CC1} = 50 mA; I_{CC2} = 30 mA; f_{XTAL} = 20 MHz; f_{CLK} = 10 MHz; 3 V cards; V_{DD} = 2.7 V	–	–	215	mA
		I_{CC1} = 50 mA; I_{CC2} = 30 mA; f_{XTAL} = 20 MHz; f_{CLK} = 10 MHz; 3 V cards; V_{DD} = 5 V	–	–	100	mA
V_{th1}	threshold voltage on V_{DD} (falling)		2.25	–	2.50	V
V_{hys1}	hysteresis on V_{th1}		50	–	170	mV
V_{th2}	threshold voltage on pin DELAY		–	1.25	–	V
V_{DELAY}	voltage on pin DELAY		–	–	V_{DD} + 0.3	V
$I_{o(DELAY)}$	output current at pin DELAY	pin grounded (charge)	–	–2	–	µA
		V_{DELAY} = V_{DD} (discharge)	–	2	–	mA
C_{DELAY}	capacitance value		1	–	–	nF
$t_{W(ALARM)}$	ALARM pulse width	C_{DELAY} = 22 nF	–	10	–	ms
RSTOUT (open-drain active HIGH output)						
I_{OH}	HIGH-level output current	active LOW option; V_{OH} = 5 V	–	–	10	µA
V_{OL}	LOW-level output voltage	active LOW option; I_{OL} = 2 mA	–0.3	–	+0.4	V
I_{OL}	LOW-level output current	active HIGH option; V_{OL} = 0 V	–	–	–10	µA
V_{OH}	HIGH-level output voltage	active HIGH option; I_{OH} = –1 mA	0.8V_{DD}	–	V_{DD} + 0.3	V
Crystal oscillator						
f_{XTAL}	crystal frequency		4	–	25	MHz
f_{ext}	external frequency applied to pin XTAL1		0	–	25	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Step-up converter						
f_{int}	oscillation frequency		2	2.5	3.7	MHz
V_{VUP}	voltage on pin V_{UP}	at least one 5 V card	–	5.7	–	V
		both cards 3 V	–	4.1	–	V
$V_{det(dt)}$	detection voltage for doubler/tripler selection		3.4	3.5	3.6	V
Reset output to the cards (RST1 and RST2)						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	0	–	0.3	V
$I_{RST(inactive)}$	current from pin RST when inactive and pin grounded		0	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} =–200 μA	V_{CC} – 0.7	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	0.1	μs
t_f	fall time	C_L = 30 pF	–	–	0.1	μs
Clock output to the cards (CLK1 and CLK2)						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	0	–	0.3	V
$I_{CLK(inactive)}$	current from pin CLK when inactive and pin grounded		0	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 μA	V_{CC} – 0.5	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	8	ns
t_f	fall time	C_L = 30 pF	–	–	8	ns
f_{CLK}	clock frequency	1 MHz Idle configuration	1	–	1.85	MHz
		operational	0	–	10	MHz
δ	duty factor	C_L = 30 pF	45	–	55	%
SR	slew rate (rise and fall)	C_L = 30 pF	0.2	–	–	V/ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Card supply voltage (V_{CC1} and V_{CC2}) (2 ceramic multilayer capacitors with low ESR of minimum 100 nF should be used in order to meet these specifications)						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	0	–	0.3	V
$I_{VCC(inactive)}$	current from pin V_{CC} when inactive and pin grounded		–	–	–1	mA
V_{CC}	output voltage	active mode; I_{CC} < 65 mA; 5 V card	4.75	5	5.25	V
		active mode; I_{CC} < 50 mA; 3 V card	2.78	3	3.22	V
		active mode; current pulses of 40 nC with I < 200 mA; t < 400 ns; f < 20 MHz; 5 V card	4.6	–	5.4	V
		active mode; current pulses of 24 nC with I < 200 mA; t < 400 ns; f < 20 MHz; 3 V card	2.75	–	3.25	V
I_{CC}	output current	3 V card; from 0 to 3 V	–	–	–50	mA
		5 V card; from 0 to 5 V	–	–	–65	mA
SR	slew rate	up or down; maximum capacitance = 300 nF	0.05	0.16	0.22	V/µs
$I_{CC1} + I_{CC2}$	sum of both cards current		–	–	–80	mA
Data lines (I/O1 and I/O2) (I/O1 has an integrated 10 kΩ pull-up at V_{CC1} and I/O2 at V_{CC2})						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	–	–	0.3	V
$I_{o(inactive)}$	current from I/O when inactive and pin grounded		–	–	–1	mA
V_{OL}	LOW-level output voltage	I/O configured as an output; I_{OL} = 1 mA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I/O configured as an output; I_{OH} < –40 µA	$0.8V_{CC}$	–	V_{CC} + 0.25	V
V_{IL}	LOW-level input voltage	I/O configured as an input	–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage	I/O configured as an input	1.5	–	V_{CC}	V
I_{IL}	LOW-level input current on I/O	V_{IL} = 0	–	–	600	µA
$I_{LI(H)}$	input leakage current HIGH on I/O	$V_{IH} = V_{CC}$	–	–	20	µA
$t_{i(tr)}$, $t_{i(tf)}$	input transition times	C_L < = 30 pF	–	–	1	µs
$t_{o(tr)}$, $t_{o(tf)}$	output transition times	C_L < = 30 pF	–	–	0.1	µs
R_{pu}	internal pull-up resistance between I/O and V_{CC}		8	10	12	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Auxiliary cards contacts (pins C41, C81, C42 and C82) (pins C41 and C81 have an integrated 10 kΩ pull-up at V_{CC1}, pins C42 and C82 have an integrated 10 kΩ pull-up at V_{CC2})						
$V_{o(inactive)}$	output voltage inactive	no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	–	–	0.3	V
$I_{inactive}$	current from pins C4 or C8 when inactive and pin grounded		–	–	–1	mA
V_{OL}	LOW-level output voltage	C4 or C8 configured as an output; I_{OL} = 1 mA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I/O configured as an output; I_{OH} < –40 µA	$0.8V_{CC}$	–	V_{CC} + 0.25	V
V_{IL}	LOW-level input voltage	C4 or C8 configured as an input	–0.3	–	+0.8	V
V_{IH}	HIGH-level output voltage	C4 or C8 configured as an input	1.5	–	V_{CC}	V
I_{IL}	LOW-level input current on pins C4 or C8	V_{IL} = 0	–	–	600	µA
$I_{LI(H)}$	input leakage current HIGH on pins C4 or C8	$V_{IH} = V_{CC}$	–	–	20	µA
$t_{i(tr)}$, $t_{i(tf)}$	input transition times	C_L = 30 pF	–	–	1	µs
$t_{o(tr)}$, $t_{o(tf)}$	output transition times	C_L = 30 pF	–	–	0.1	µs
$t_{W(pu)}$	width of active pull-up pulse		–	200	–	ns
$R_{int(pu)}$	internal pull-up resistance between C4/C8 and V_{CC}		8	10	12	kΩ
$f_{(max)}$	maximum frequency on C4 or C8		–	–	1	MHz
Timing						
t_{act}	activation sequence duration		–	–	130	µs
t_{de}	deactivation sequence duration		–	–	150	µs
Protections and limitations						
$I_{CC(sd)}$	shutdown and limitation current at V_{CC}		–	–100	–	mA
$I_{I/O(lim)}$	limitation current on the I/O		–15	–	+15	mA
$I_{CLK(lim)}$	limitation current on pin CLK		–70	–	+70	mA
$I_{RST(sd)}$	shutdown and limitation current on RST		–20	–	+20	mA
T_{sd}	shutdown temperature		–	150	–	°C
Card presence inputs 1s (pins PRES1 and PRES2)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	–	V
$I_{IL(L)}$	input leakage current LOW	V_{IN} = 0	–20	–	+20	µA
$I_{IL(H)}$	input leakage current HIGH	$V_{IN} = V_{DD}$	–20	–	+20	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Bidirectional data bus (pins D0 to D7)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	–	V
$I_{IL(L)}$	input leakage current LOW		–20	–	+20	µA
$I_{IL(H)}$	input leakage current HIGH		–20	–	+20	µA
C_L	load capacitance		–	–	10	pF
V_{OL}	LOW-level output voltage	I_{OL} = 5 mA	–	–	$0.2V_{DD}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = –5 mA	$0.8V_{DD}$	–	–	V
$t_{o(tr)}$, $t_{o(tf)}$	output transition time	C_L = 50 pF	–	–	25	ns
Logic inputs (pins ALE, A0, A1, A2, A3, INTAUX, $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$)						
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
$I_{IL(L)}$	input leakage current LOW		–20	–	+20	µA
$I_{IL(H)}$	input leakage current HIGH		–20	–	+20	µA
C_L	load capacitance		–	–	10	pF
Auxiliary I/O (pin I/OAUX)						
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
$I_{IL(H)}$	input leakage current HIGH		–20	–	+20	µA
I_{IL}	LOW-level input current	V_{IL} = 0	–	–	–600	µA
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	–	–	300	mV
V_{OH}	HIGH-level output voltage	I_{OH} = 40 µA	$0.8V_{DD}$	–	V_{DD} +0.25	V
$R_{int(pu)}$	internal pull-up resistance between I/OAUX and V_{DD}		8	10	12	kΩ
$t_{i(tr)}$, $t_{i(tf)}$	input transition time	C_L = 30 pF	–	–	1	µs
$t_{o(tr)}$, $t_{o(tf)}$	output transition time	C_L = 30 pF	–	–	0.1	µs
$f_{I/OAUX(max)}$	maximum frequency on pin I/OAUX		–	–	1	MHz
Interrupt line $\overline{INT}$ (open-drain active LOW output)						
V_{OH}	LOW-level output voltage	I_{OH} = 2 mA	–	–	0.3	V
$I_{IL(H)}$	input leakage current HIGH		–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing for multiplexed bus; see Fig.4						
t_{XTAL1}	period on XTAL1		50	–	–	ns
$t_{W(ALE)}$	ALE pulse width		20	–	–	ns
t_{AVLL}	address valid to ALE LOW		10	–	–	ns
$t_{(AL-RWL)}$	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW		10	–	–	ns
$t_{W(RD)}$	$\overline{RD}$ pulse width for URR		$2t_{XTAL1}$	–	–	ns
	pulse width for other registers		10	–	–	ns
$t_{(RL-DV)}$	$\overline{RD}$ LOW to data out valid		–	–	50	ns
$t_{(RWH-AH)}$	$\overline{RD}$ or WR HIGH to ALE HIGH		10	–	–	ns
$t_{W(WR)}$	$\overline{WR}$ pulse width		10	–	–	ns
$t_{(DV-WL)}$	data in valid to $\overline{WR}$ LOW		10	–	–	ns
Timing for non-multiplexed bus; see Fig.5						
$t_{(REH-CL)}$	$\overline{RD}$ or $\overline{EN}$ HIGH to $\overline{CS}$ LOW		10	–	–	ns
$t_{(CEL-DV)}$	$\overline{CS}$ and $\overline{EN}$ LOW to data out valid	when reading from URR; $t_{(CEL-DV)}$ is minimum $2t_{XTAL1}$	–	–	50	ns
$t_{(CEH-DZ)}$	$\overline{CS}$ and $\overline{EN}$ HIGH to data high-impedance		–	–	10	ns
$t_{(AD-DV)}$	addresses stable to data out valid		–	–	10	ns
$t_{(RL-CEL)}$	R/$\overline{W}$ LOW to $\overline{CS}$ or $\overline{EN}$ LOW		10	–	–	ns
$t_{(CREL-DZ)}$	$\overline{CS}$ and R/$\overline{W}$ and $\overline{EN}$ LOW to data in high-impedance		–	–	–	ns
$t_{(DV-WL)}$	DATA valid to $\overline{WR}$ LOW		10	–	–	ns

APPLICATION INFORMATION:

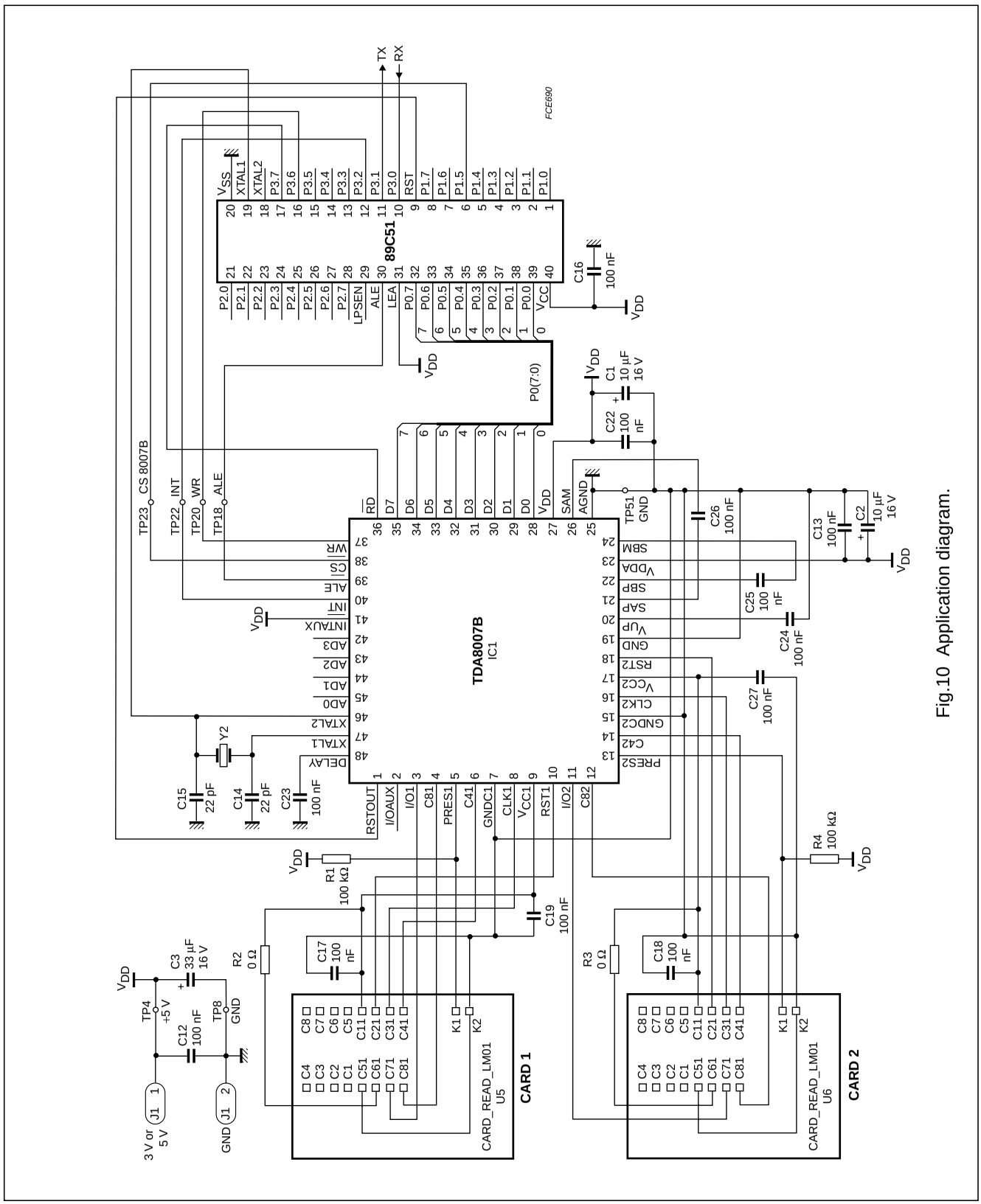
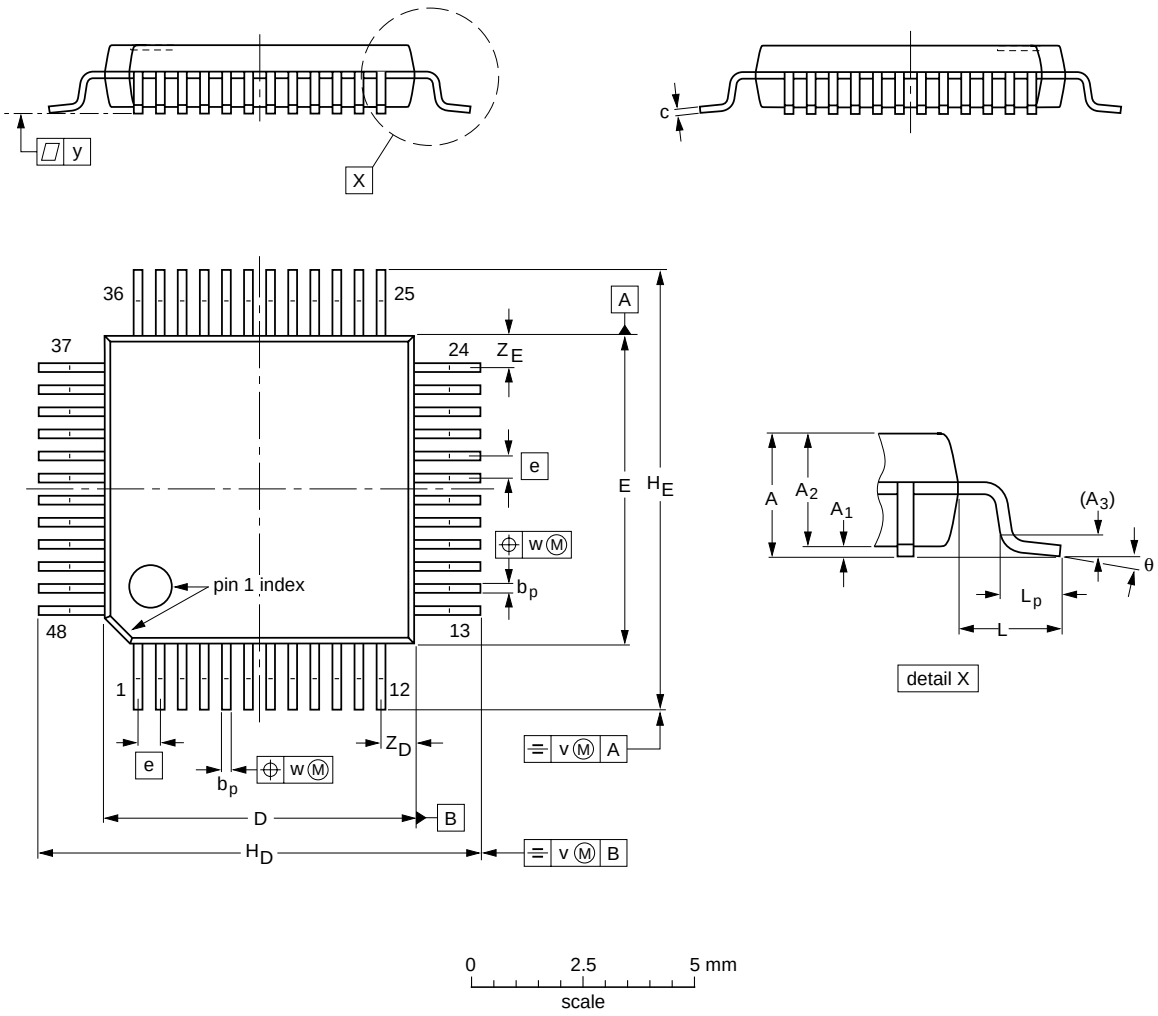


Fig.10 Application diagram.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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