

OptiMOS®-T2 Power-Transistor

Features

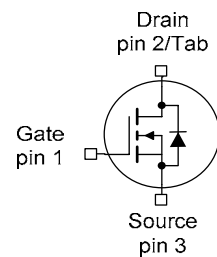
- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

Product Summary

| | | |
|------------------|-----|----|
| V_{DS} | 40 | V |
| $R_{DS(on),max}$ | 5.9 | mΩ |
| I_D | 75 | A |

PG-TO252-3-313


| Type | Package | Marking |
|---------------|----------------|---------|
| IPD75N04S4-06 | PG-TO252-3-313 | 4N0406 |


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|--|----------------|---|--------------|------|
| Continuous drain current | I_D | $T_C=25\text{ °C}, V_{GS}=10\text{V}$ | 75 | A |
| | | $T_C=100\text{ °C}, V_{GS}=10\text{V}^{2)}$ | 53 | |
| Pulsed drain current ¹⁾ | $I_{D,pulse}$ | $T_C=25\text{ °C}$ | 300 | |
| Avalanche energy, single pulse ¹⁾ | E_{AS} | $I_D=35\text{A}$ | 72 | mJ |
| Avalanche current, single pulse | I_{AS} | - | 75 | A |
| Gate source voltage | V_{GS} | - | ±20 | V |
| Power dissipation | P_{tot} | $T_C=25\text{ °C}$ | 58 | W |
| Operating and storage temperature | T_j, T_{stg} | - | -55 ... +175 | °C |
| IEC climatic category; DIN IEC 68-1 | - | - | 55/175/56 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|--|------------|--|--------|------|------|------|
| | | | min. | typ. | max. | |
| Thermal characteristics¹⁾ | | | | | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | - | 2.6 | K/W |
| Thermal resistance, junction - ambient, leaded | R_{thJA} | - | - | - | 62 | |
| SMD version, device on PCB | R_{thJA} | minimal footprint | - | - | 62 | |
| | | 6 cm ² cooling area ²⁾ | - | - | 40 | |

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

| | | | | | | |
|----------------------------------|---------------|--|-----|-------|-----|---------------|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}=0V, I_D=1\text{mA}$ | 40 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=26\mu\text{A}$ | 2.0 | 3.0 | 4.0 | |
| Zero gate voltage drain current | I_{DSS} | $V_{DS}=40V, V_{GS}=0V, T_j=25^\circ\text{C}$ | - | 0.015 | 1 | μA |
| | | $V_{DS}=18V, V_{GS}=0V, T_j=85^\circ\text{C}^{2)}$ | - | 1 | 20 | |
| Gate-source leakage current | I_{GSS} | $V_{GS}=20V, V_{DS}=0V$ | - | - | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}=10V, I_D=75A$ | - | 5.0 | 5.9 | m Ω |

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic characteristics¹⁾

| | | | | | | |
|------------------------------|--------------|--|---|------|------|----|
| Input capacitance | C_{iss} | $V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$ | - | 1960 | 2550 | pF |
| Output capacitance | C_{oss} | | - | 490 | 640 | |
| Reverse transfer capacitance | C_{rss} | | - | 15 | 35 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}=20\text{V}, V_{GS}=10\text{V},$ $I_D=75\text{A}, R_G=3.5\Omega$ | - | 7 | - | ns |
| Rise time | t_r | | - | 9 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 6 | - | |
| Fall time | t_f | | - | 8 | - | |

Gate Charge Characteristics¹⁾

| | | | | | | |
|-----------------------|---------------|---|---|------|------|----|
| Gate to source charge | Q_{gs} | $V_{DD}=32\text{V}, I_D=75\text{A},$ $V_{GS}=0\text{ to }10\text{V}$ | - | 11.7 | 15.2 | nC |
| Gate to drain charge | Q_{gd} | | - | 3.5 | 8.1 | |
| Gate charge total | Q_g | | - | 24.5 | 32 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 5.9 | - | V |

Reverse Diode

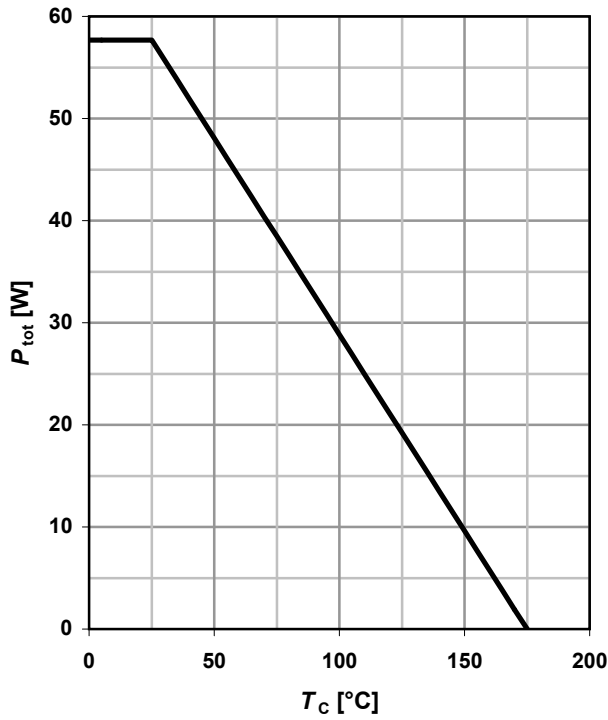
| | | | | | | |
|--|---------------|--|---|-----|-----|----|
| Diode continuous forward current ¹⁾ | I_S | $T_C=25^\circ\text{C}$ | - | - | 75 | A |
| Diode pulse current ¹⁾ | $I_{S,pulse}$ | | - | - | 300 | |
| Diode forward voltage | V_{SD} | $V_{GS}=0\text{V}, I_F=75\text{A},$ $T_j=25^\circ\text{C}$ | - | 0.9 | 1.3 | V |
| Reverse recovery time ¹⁾ | t_{rr} | $V_R=20\text{V}, I_F=50\text{A},$ $di_F/dt=100\text{A}/\mu\text{s}$ | - | 36 | - | ns |
| Reverse recovery charge ¹⁾ | Q_{rr} | | - | 31 | - | nC |

¹⁾ Defined by design. Not subject to production test.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

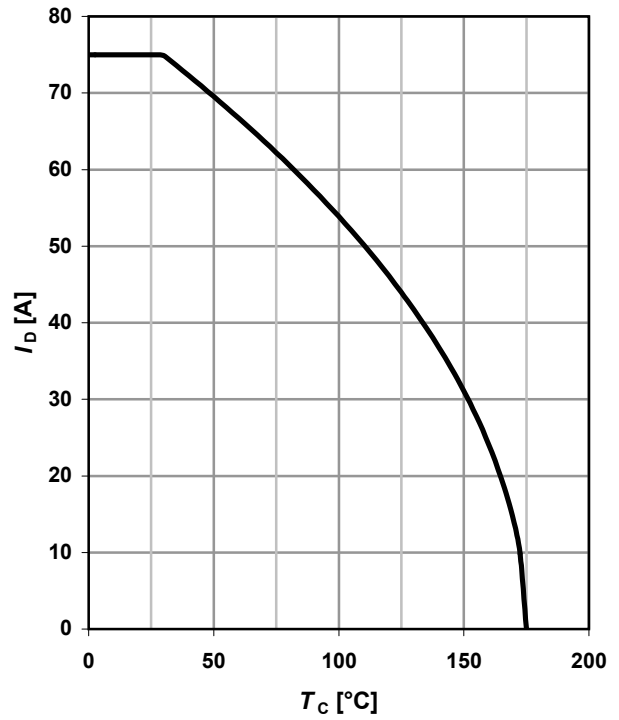
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \geq 6 V$



2 Drain current

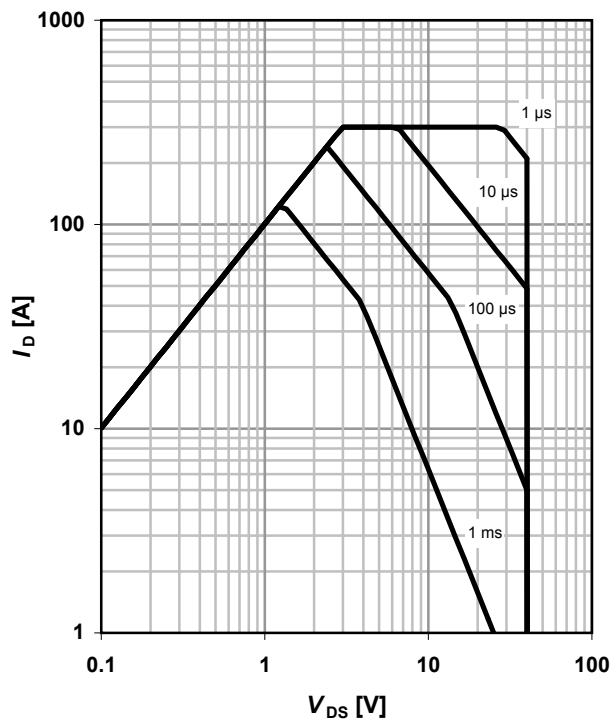
$I_D = f(T_C); V_{GS} \geq 6 V$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25^\circ C; D = 0$

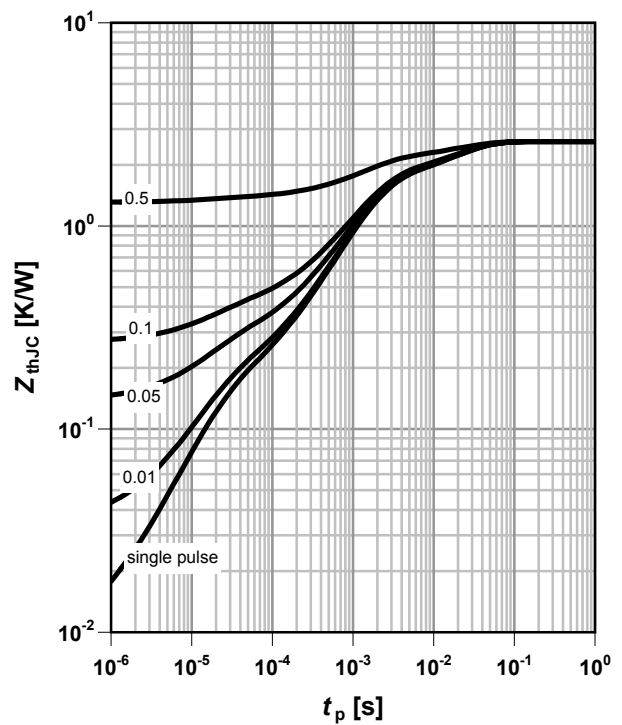
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

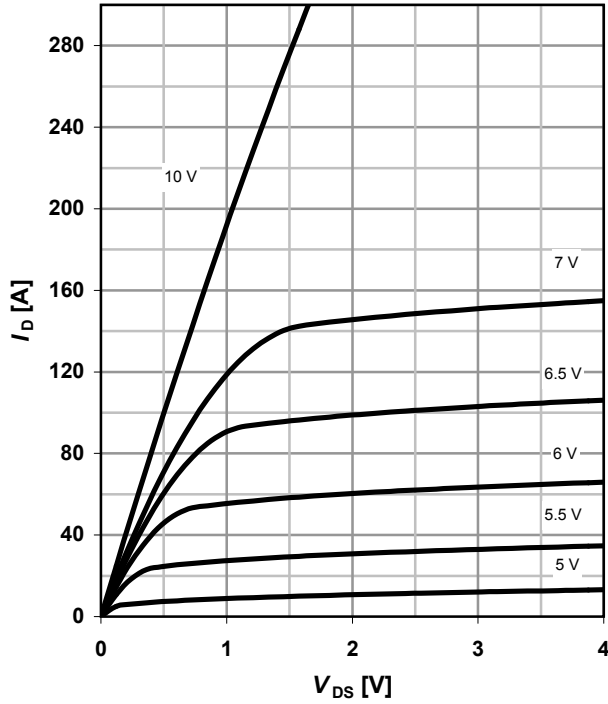
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

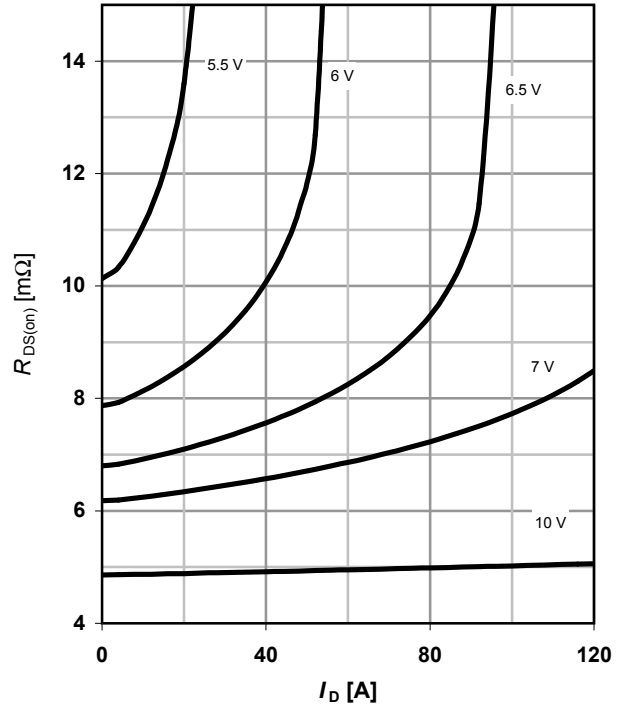
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

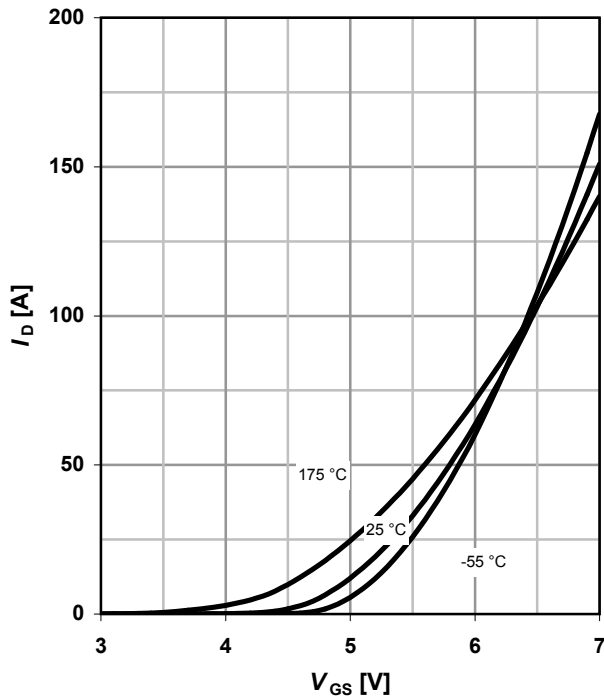
parameter: V_{GS}



7 Typ. transfer characteristics

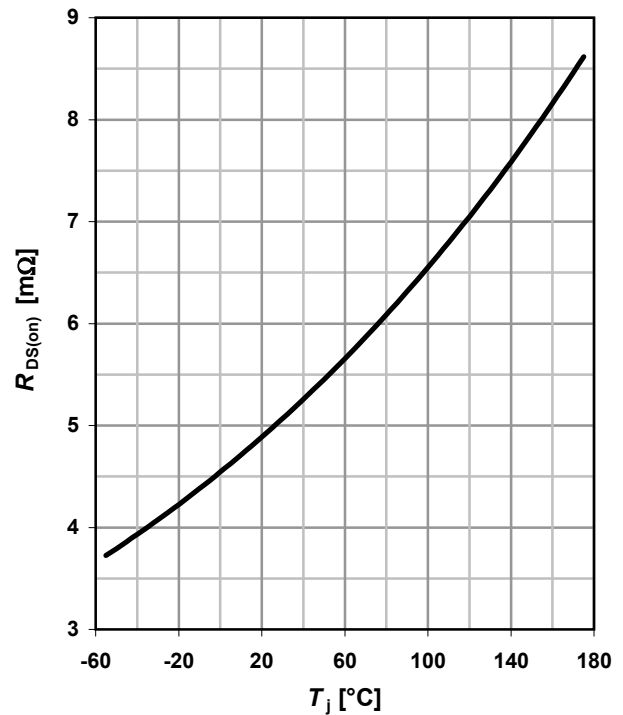
$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j



8 Typ. drain-source on-state resistance

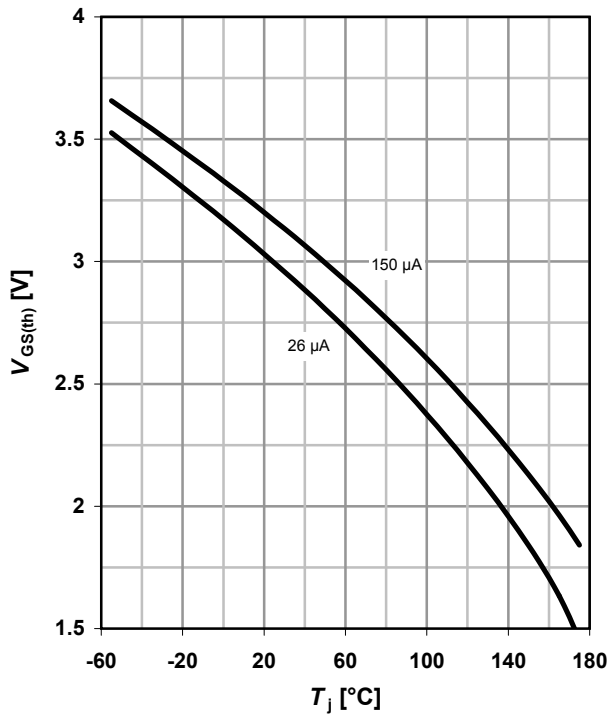
$R_{DS(on)} = f(T_j); I_D = 75\text{ A}; V_{GS} = 10\text{ V}$



9 Typ. gate threshold voltage

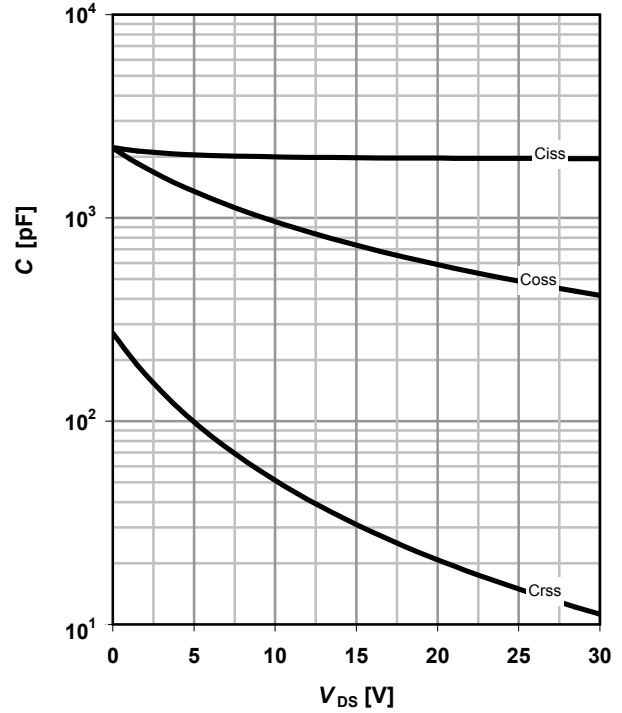
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

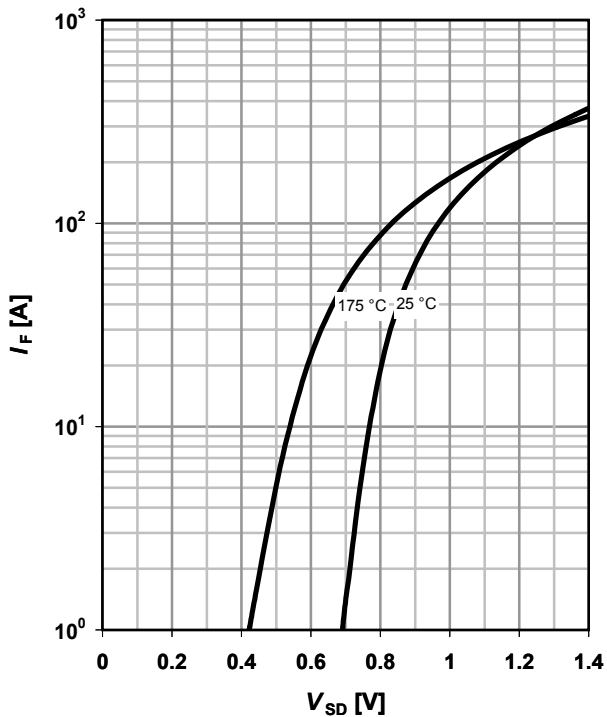
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

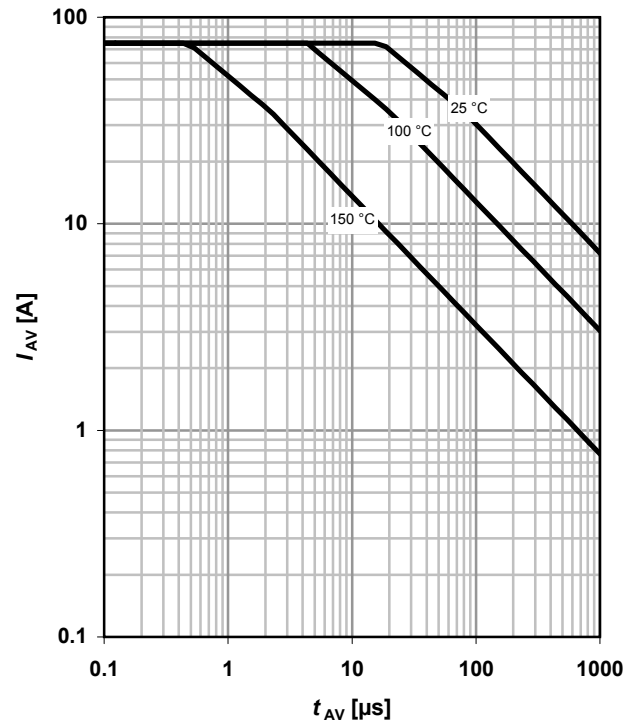
parameter: T_j



12 Avalanche characteristics

$I_{AS} = f(t_{AV})$

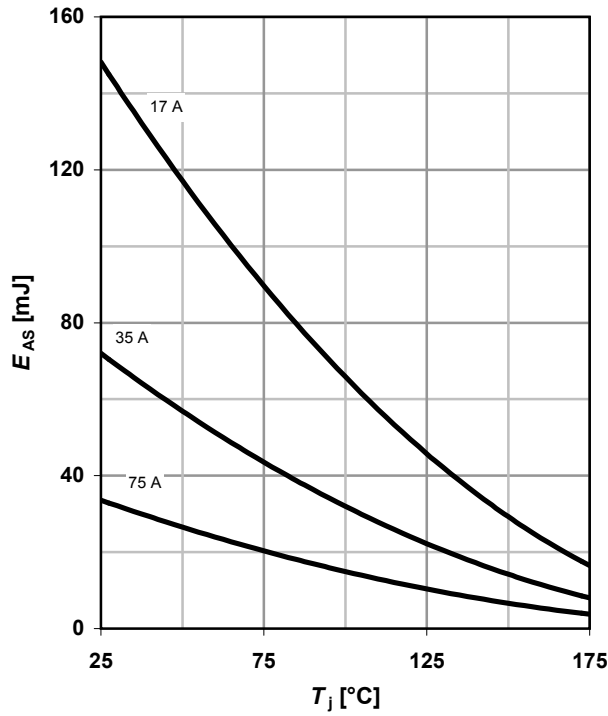
parameter: $T_{j(start)}$



13 Avalanche energy

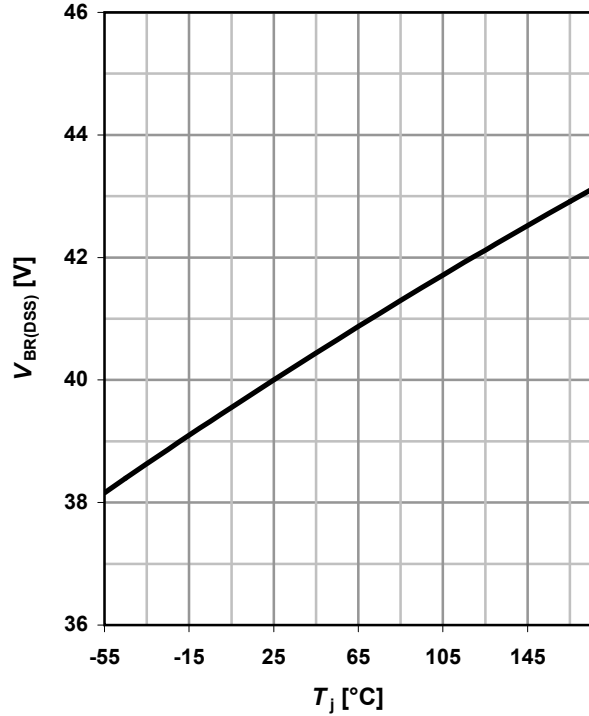
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

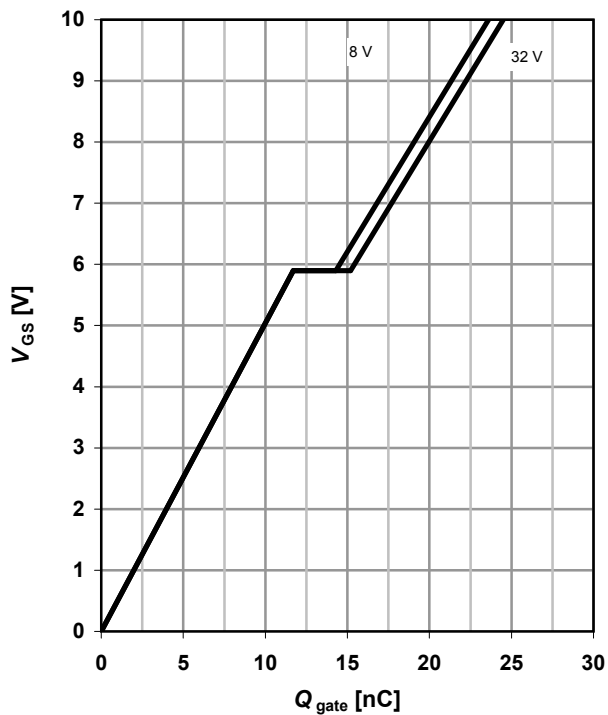
$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$



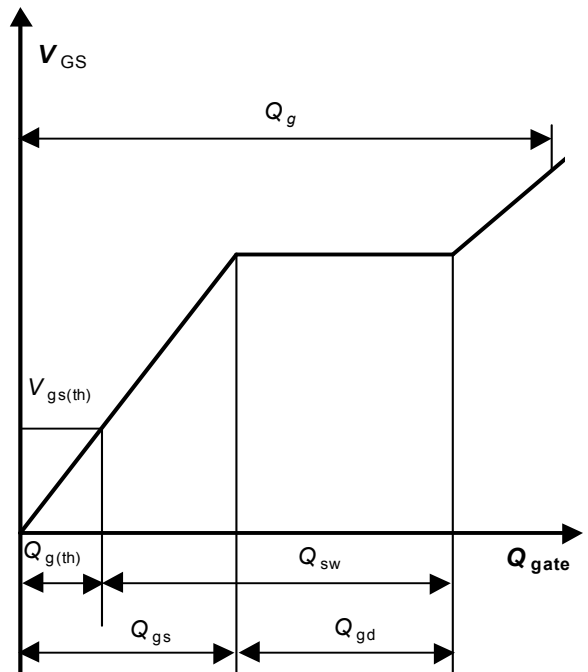
15 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = 75 \text{ A pulsed}$

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

| Version | Date | Changes |
|--------------|------------|-------------------------------|
| Revision 1.0 | 06.04.2010 | Final Data Sheet |
| Revision 1.1 | 15.07.2010 | Update of Gate Charge diagram |
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