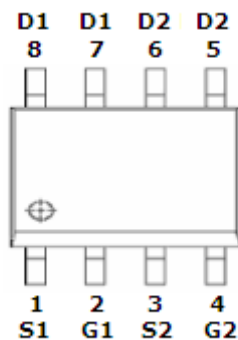


DESCRIPTION

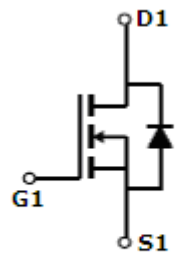
The STN9926 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

**PIN CONFIGURATION
SOP-8**

FEATURE

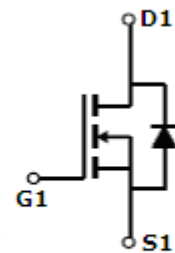
- 20V/5.0A, $R_{DS(ON)} = 50m\Omega$ @VGS = 4.5V
- 20V/4.0A, $R_{DS(ON)} = 65m\Omega$ @VGS = 2.5V
- 20V/2.8A, $R_{DS(ON)} = 90m\Omega$ @VGS = 1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

**PART MARKING
SOP-8**


S : Subcontractor Y : Year Code
A : Process Code



N-Channel



N-Channel

ORDERING INFORMATION

Part Number	Package	Part Marking
STN9926S8RG	SOP-8	STN9926
STN9926S8TG	SOP-8	STN9926

※ Process Code : A ~ Z ; a ~ z

※ STN9926S8RG S8 : SOP-8 ; R : Tape Reel ; G : Pb – Free

※ STN9926S8TG S8 : SOP-8 ; T : Tube ; G : Pb – Free



STN9926  Lead-free

Dual N Channel Enhancement Mode MOSFET
5A

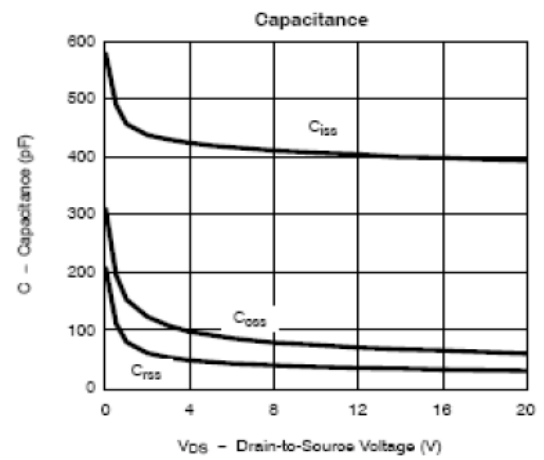
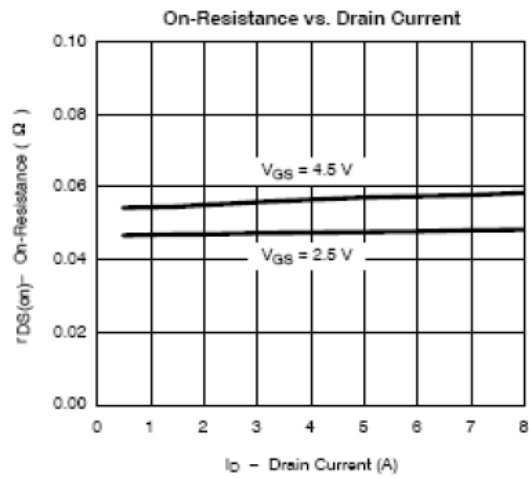
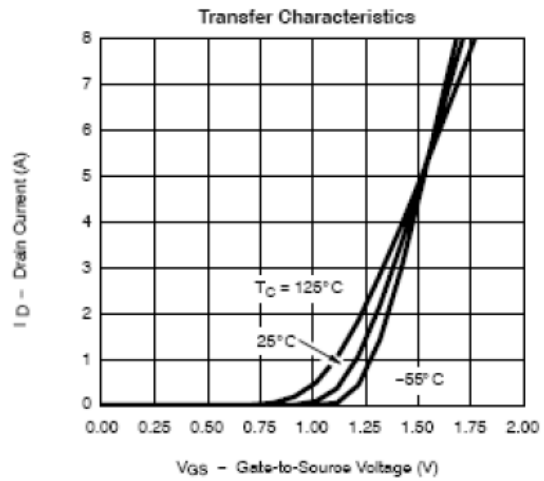
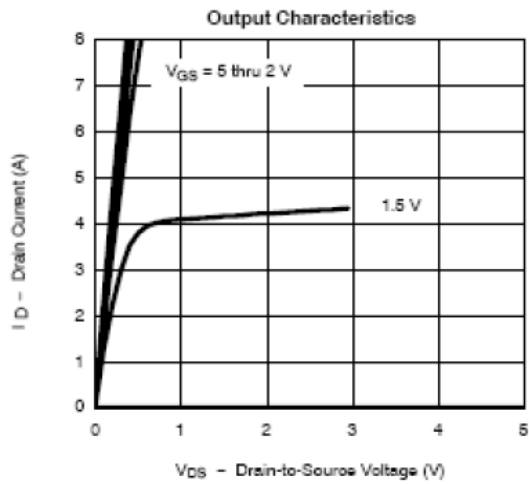
ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	20	V
Gate-Source Voltage		V _{GSS}	±12	V
Continuous Drain Current (T _J =150°C)	T _A =25°C	I _D	5.0	A
	T _A =70°C		4.0	
Pulsed Drain Current		I _{DM}	30	A
Continuous Source Current (Diode Conduction)		I _S	1.6	A
Power Dissipation	T _A =25°C	P _D	2.8	W
	T _A =70°C		1.8	
Operation Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	105	°C/W

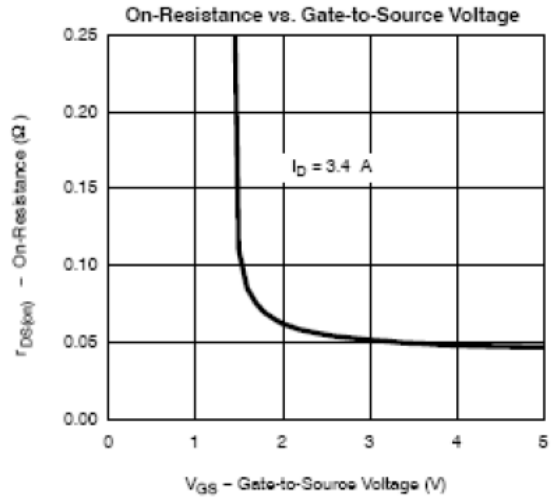
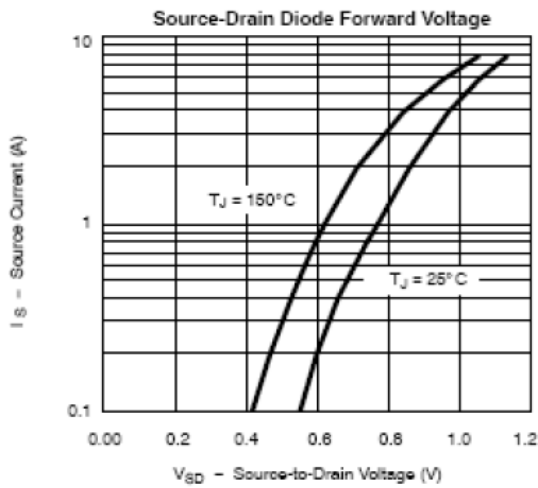
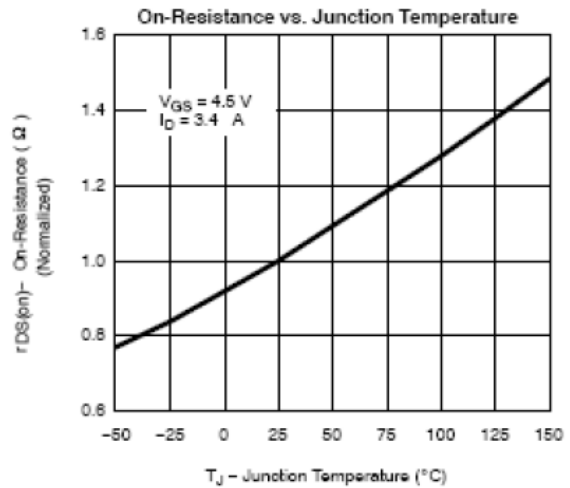
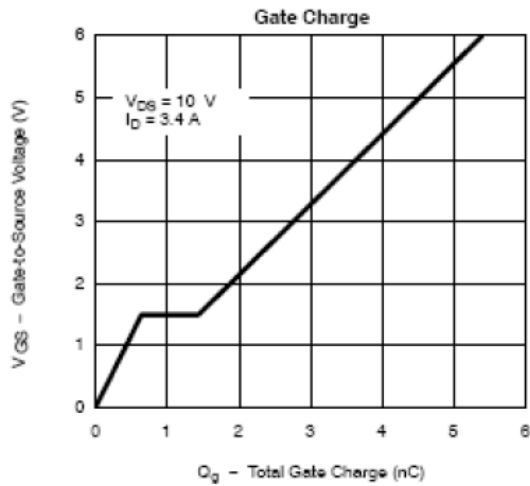
ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.4		1.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS} $T_J=55^\circ C$	$V_{DS}=20V, V_{GS}=0V$			1	uA
		$V_{DS}=20V, V_{GS}=0V$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\leq 5V, V_{GS}=4.5V$	6			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=5.0A$		0.004	0.050	Ω
		$V_{GS}=2.5V, I_D=4.0A$		0.055	0.065	
		$V_{GS}=1.8V, I_D=2.8A$		0.075	0.090	
Forward Tran Conductance	g_{fs}	$V_{DS}=5.0V, I_D=3.6A$		10		S
Diode Forward Voltage	V_{SD}	$I_S=1.6A, V_{GS}=0V$		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=6.0V, V_{GS}=4.5V$ $I_D=2.8A$		4.8	8.0	nC
Gate-Source Charge	Q_{gs}			1.0		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	$V_{DS}=6.0V, V_{GS}=0V$ $f=1MHz$		485		pF
Output Capacitance	C_{oss}			85		
Reverse Transfer Capacitance	C_{rss}			40		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=15V, R_L=15\Omega$ $I_D=1A, V_{GEN}=10V$ $R_G=6\Omega$		12	20	nS
				10	20	
Turn-Off Time	$t_{d(off)}$ t_f			30	36	
				15	17	

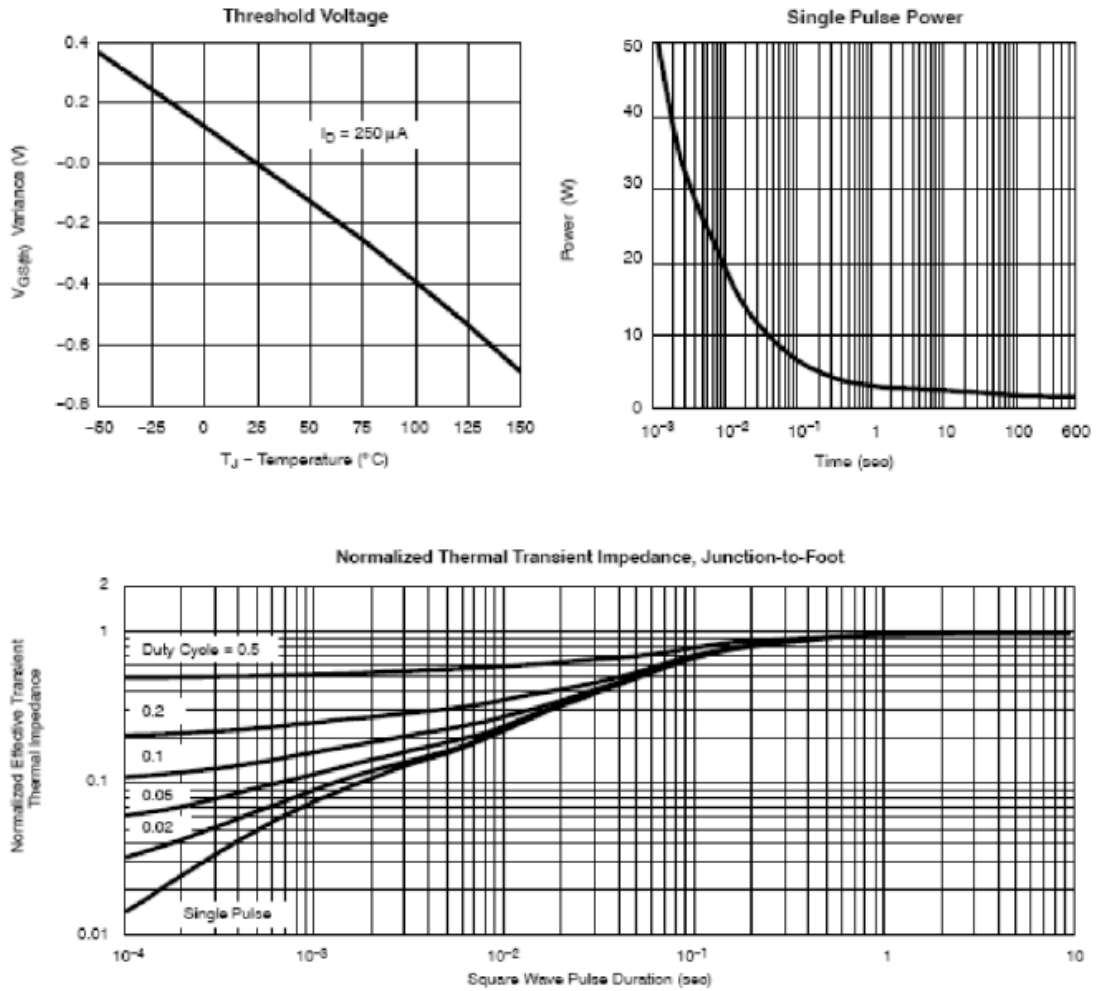
TYPICAL CHARACTERISTICS (25°C Unless Note)

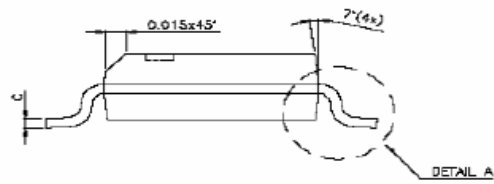
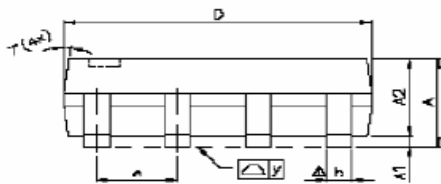
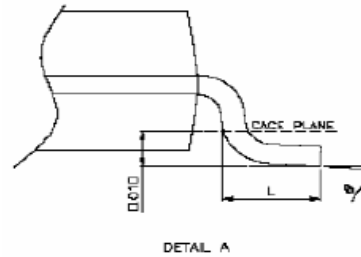
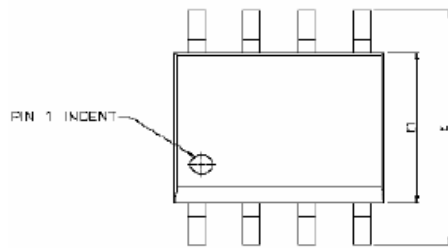


TYPICAL CHARACTERISTICS (25°C Unless Note)



TYPICAL CHARACTERISTICS (25°C Unless Note)



SOP-8 PACKAGE OUTLINE


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
\varnothing	0°	—	8°	0°	—	8°