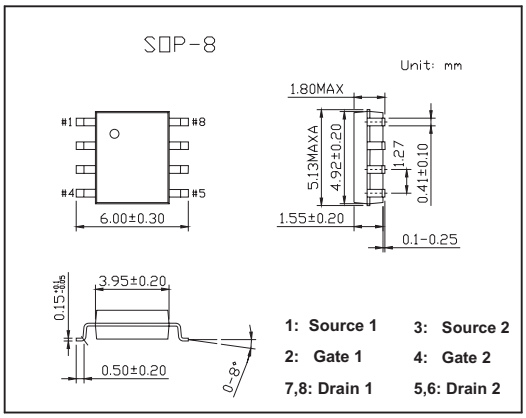
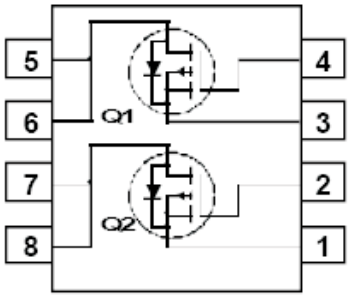
Dual 30V P-Channel PowerTrench MOSFET

KDS4953



■ Features

- -5 A, -30 V. $R_{DS(ON)}$ = 55mΩ @ V_{GS} = -10V
  $R_{DS(ON)}$ = 95mΩ @ V_{GS} =-4.5V
- Low gate charge(6nC typical)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability
- Fast switching speed



■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	-30	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current Continuous (Note 1a)	I_D	-5	A
Drain Current Pulsed		-20	A
Power Dissipation for Single Operation (Note 1a)	P_D	2	W
Power Dissipation for Single Operation (Note 1b)		1.6	
Power Dissipation for Single Operation (Note 1c)		1	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	℃
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78	℃/W
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40	℃/W

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■ Electrical Characteristics Ta = 25℃

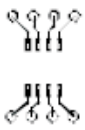
Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = -250 μA	-30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = -250 μA, Referenced to 25℃		-23		mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24 V, V_{GS} = 0 V			-1	μA
Gate-Body Leakage, Forward	I_{GSSF}	V_{GS} = -20V, V_{DS} = 0 V			100	nA
Gate-Body Leakage, Reverse	I_{GSSR}	V_{GS} = 20 V, V_{DS} = 0 V			-100	nA
Gate Threshold Voltage(Not 2)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 μA	-1	-1.7	-3	V
Gate Threshold Voltage Temperature Coefficient(Not 2)	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = -250 μA, Referenced to 25℃		4.5		mV/℃
Static Drain-Source On-Resistance(Not 2)	$R_{DS(on)}$	V_{GS} = -10 V, I_D =-5 A		46	55	mΩ
		V_{GS} = -4.5 V, I_D = -3.3 A		70	95	
		V_{GS} = -10 V, I_D =-5 A,T_J = 125℃		63	85	
On□State Drain Current	$I_{D(on)}$	V_{GS} = -10 V, V_{DS} = -5 V	-20			A
Forward Transconductance	g_{FS}	V_{DS} = -5 V, I_D = -5A		10		S
Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V,f = 1.0 MHz		528		pF
Output Capacitance	C_{oss}			132		pF
Reverse Transfer Capacitance	C_{rss}			70		pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -15 V, I_D = -1 A,V_{GS} = -10 V, R_{GEN} = 6 Ω (Note 2)		7	14	ns
Turn-On Rise Time	t_r			13	24	ns
Turn-Off Delay Time	$t_{d(off)}$			14	25	ns
Turn-Off Fall Time	t_f			9	17	ns
Total Gate Charge	Q_g	V_{DS} = -15 V, I_D =-5 A,V_{GS}=-5V(Note 2)		6	9	nC
Gate-Source Charge	Q_{gs}			2.2		nC
Gate-Drain Charge	Q_{gd}			2		nC
Maximum Continuous Drain□Source Diode Forward Current	I_S				-1.3	A
Drain□Source Diode Forward Voltage	V_{SD}	V_{GS}=0V,Is=-1.3A (Note 2)		-0.8	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper

b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%