VS2000 - Headtracking Multichannel USB Audio Headphone IC / USB DAC

Hardware Features

- Low-power operation
- Single input voltage: Internal voltage regulation for analog, digital, and I/O power
- Operates with a single 12 MHz clock
- Internal PLL clock multiplier
- USB Full Speed hardware
- I/O for user interface
- High-quality on-chip stereo DAC with no phase error between channels
- Stereo earphone driver capable of driving a 30 Ω load
- Lead-free RoHS-compliant package (Green)

Firmware Features

- 5.1-channel USB Audio Device
- Human Interface Device (HID) Buttons
  - Volume Decrement
  - Volume Increment
  - Pause
  - Play
  - Rewind
  - Fast Forward
- Volume controls also work without HID-aware host
- Four room effect levels selected with Effect Level Button
- Tracking On / Tracking Off / Bypass modes selected with Power Button
- Bass and treble controls through USB Audio Feature Unit
- Advanced controls through separate software
- SPI EEPROM boot for special applications
- UART for debugging and special applications

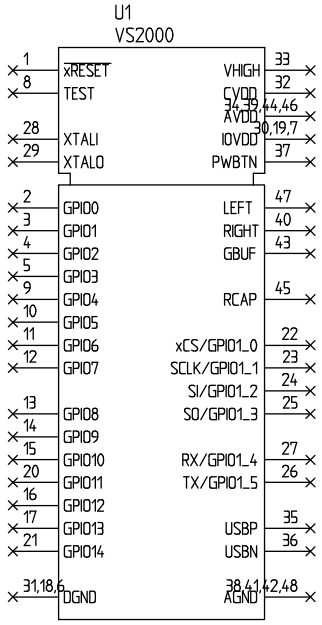
Description

VS2000 is a single-chip multichannel headtracking USB Audio IC with audio output to headphones. VS2000 contains a high-performance low-power DSP core VS_DSP[4], Full Speed USB port, general purpose I/O pins, SPI, UART, as well as a high-quality variable-sample-rate stereo DAC, and an earphone amplifier, and a common voltage buffer.

When connected to USB, VS2000 firmware controls an ultrasound transmitter and reads ultrasound receivers to track the movement of the listener's head. VS2000 then performs real-time spatial processing to the 5.1 audio channels to position each sound source correctly depending on the head movement.

An application without headtracking and just with 5.1 audio is also possible.

SPI EEPROM can be used to load code to customize the system.



Contents

List of Figures

1 Disclaimer

This is a *preliminary* datasheet. All properties and figures are subject to change.

2 Definitions

B Byte, 8 bits.

b Bit.

Ki "Kibi" = 2^{10} = 1024 (IEC 60027-2).

Mi "Mebi" = 2^{20} = 1048576 (IEC 60027-2).

VS_DSP VLSI Solution's DSP core.

W Word. In VS_DSP, instruction words are 32-bit and data words are 16-bit wide.

3 Characteristics & Specifications

3.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Regulator input voltage	VHIGH	-0.3	4.0	V
Injected Current on Any Pin			±50	mA
Voltage at Any Digital Input		-0.3	IOVDD+0.3[1]	V
Operating Temperature		-40	+85	°C
Storage Temperature		-65	+150	°C

[1] Must not exceed 3.6 V

3.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature		-40		+85	°C
Analog and Digital Ground [1]	AGND DGND		0.0		V
Regulator input voltage[3]	VHIGH	AVDD+0.3	5.0	5.25	V
Input Clock Frequency	XTALI		12[2]		MHz
Internal Clock Frequency	CLKI	12	48	48	MHz
Master Clock Duty Cycle		40	50	60	%

[1] Must be connected together as close the device as possible for latch-up immunity.
[2] To be able to use USB, XTALI must be 12 MHz.
[3] 4.0 V is required for compliant USB level.

3.3 Analog Characteristics of Audio Outputs

Unless otherwise noted: AVDD=2.8V, CVDD=2.5V, IOVDD=3.3V, TA=-40..+85°C, XTALI=12 MHz, Internal Clock Multiplier $4.0\times$. DAC tested with full-scale output sinewave, measurement bandwidth 20..20000 Hz, analog output load: LEFT to CBUF 30Ω, RIGHT to CBUF 30Ω.

Parameter	Symbol	Min	Typ	Max	Unit
DAC Resolution			18		bits
Total Harmonic Distortion	THD			0.1	%
Dynamic Range (DAC unmuted, A-weighted)	IDR		94		dB
S/N Ratio (full scale signal, no load)	SNR		90		dB
Interchannel Isolation (Cross Talk)		50	75		dB
Interchannel Isolation (Cross Talk), with GBUF			40		dB
Interchannel Gain Mismatch		-0.5		0.5	dB
Frequency Response		-0.05		0.05	dB
Full Scale Output Voltage (Peak-to-peak)		1.3	1.5	1.7	Vpp
Deviation from Linear Phase				5	°
Analog Output Load Resistance	AOLR		30[1]		Ω
Analog Output Load Capacitance				100[2]	pF
CBUF disconnect current (short-circuit protection)			200		mA

[1] AOLR may be lower than *Typical*, but distortion performance may be compromised. Also, there is a maximum current that the internal regulators can provide.

[2] CBUF must have external 10 Ω + 47 nF load, LEFT and RIGHT must have external 20 Ω + 10 nF load for stability.

3.4 Analog Characteristics of Regulators

Parameter	Symbol	Min	Typ	Max	Unit
Continuous current, IOVDD				50	mA
Continuous current, CVDD				50	mA
Continuous current, AVDD				100	mA
Dropout voltages, 30 mA			0.3		V
Line regulation, VHIGH_{min} ... VHIGH_{max}			10		mV
Load regulation, 1 mA ... 30 mA				100	mV
Absolute gain setting accuracy [1]		-150		+150	mV
Gain step setting accuracy		-10		+10	%

[1] Absolute level depends on RCAP voltage

3.5 Power Consumption

Parameter	Min	Typ	Max	Unit
Full operation in example application, V_{bus} = 5 V		75		mA

3.6 Digital Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage		0.7×IOVDD		IOVDD+0.3[1]	V
Low-Level Input Voltage		-0.2		0.3×IOVDD	V
High-Level Output Voltage at I_O = -2.0 mA		0.7×IOVDD			V
Low-Level Output Voltage at I_O = 2.0 mA				0.3×IOVDD	V
Input Leakage Current		-1.0		1.0	μA
Rise time of all output pins, load = 50 pF				50	ns

4 Packages and Pin Descriptions

4.1 Packages

LPQFP-48 is lead (Pb) free and also RoHS compliant package. RoHS is a short name of *Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment*.

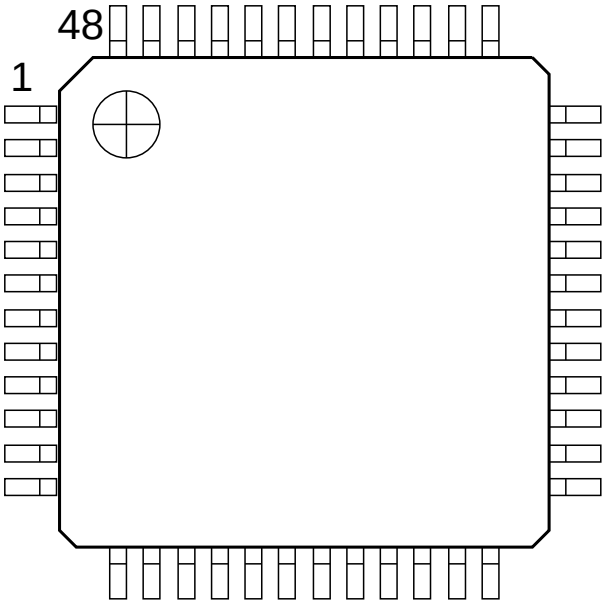


Figure 1: Pin Configuration, LQFP-48.

LQFP-48 package dimensions are at *http://www.vlsi.fi/* .

4.2 LQFP-48 Pin Descriptions

Pin Name	LQFP Pin	Pin Type	Function
XRESET	1	DI	Active low asynchronous reset, schmitt-trigger input
GPIO0_0	2	DIO	General-purpose IO Port 0, bit 0
GPIO0_1	3	DIO	General-purpose IO Port 0, bit 1
GPIO0_2	4	DIO	General-purpose IO Port 0, bit 2
GPIO0_3	5	DIO	General-purpose IO Port 0, bit 3
DGND0	6	DGND	Core & I/O ground
IOVDD1	7	IOPWR	I/O power supply
TEST	8	DI	Test mode input (active high), connect to DGND
GPIO0_4	9	DIO	General-purpose IO Port 0, bit 4
GPIO0_5	10	DIO	General-purpose IO Port 0, bit 5
GPIO0_6	11	DIO	General-purpose IO Port 0, bit 6
GPIO0_7	12	DIO	General-purpose IO Port 0, bit 7
GPIO0_8	13	DIO	General-purpose IO Port 0, bit 8
GPIO0_9	14	DIO	General-purpose IO Port 0, bit 9
GPIO0_10	15	DIO	General-purpose IO Port 0, bit 10
GPIO0_12	16	DIO	General-purpose IO Port 0, bit 12
GPIO0_13	17	DIO	General-purpose IO Port 0, bit 13
DGND1	18	DGND	Core & I/O ground
IOVDD2	19	IOPWR	I/O power supply
GPIO0_11	20	DIO	General-purpose IO Port 0, bit 11
GPIO0_14	21	DIO	General-purpose IO Port 0, bit 14
XCS / GPIO1_0	22	DIO	SPI XCS / General-Purpose I/O Port 1, bit 0
SCLK / GPIO1_1	23	DIO	SPI CLK / General-Purpose I/O Port 1, bit 1
SI / GPIO1_2	24	DIO	SPI MISO / General-Purpose I/O Port 1, bit 2
SO / GPIO1_3	25	DIO	SPI MOSI / General-Purpose I/O Port 1, bit 3
TX / GPIO1_4	26	DIO	UART TX / General-Purpose I/O Port 1, bit 4
RX / GPIO1_5	27	DIO	UART RX / General-Purpose I/O Port 1, bit 5
XTALI	28	AI	Crystal input
XTALO	29	AO	Crystal output
IOVDD	30	IOPWR	I/O power supply, Regulator output
DGND2	31	DGND	Core & I/O ground
CVDD	32	CPWR	Core power supply, Regulator output
VHIGH	33	PWR	Power supply, Regulator input
AVDD	34	APWR	Analog power supply, Regulator output
USBP	35	AIO	USB differential + in / out, controllable 1.5kΩ pull-up
USBN	36	AIO	USB differential - in / out
PWRBTN	37	AIO	Power button for Regulator startup (and Power Key)
AGND0	38	APWR	Analog ground
AVDD1	39	APWR	Analog power supply
RIGHT	40	AO	Right channel output
AGND1	41	APWR	Analog ground
AGND2	42	APWR	Analog ground
CBUF	43	AO	Common voltage buffer for headphones
AVDD2	44	APWR	Analog power supply
RCAP	45	AIO	Filtering capacitance for reference
AVDD3	46	APWR	Analog power supply
LEFT	47	AO	Left channel output
AGND3	48	APWR	Analog ground

Pin types:

Type	Description
DI	Digital input, CMOS Input Pad
DO	Digital output, CMOS Input Pad
DIO	Digital input/output
AI	Analog input
AO	Analog output

Type	Description
AIO	Analog input/output
APWR	Analog power supply pin
DGND	Core or I/O ground pin
CPWR	Core power supply pin
IOPWR	I/O power supply pin

5 VS2000 Functional Blocks

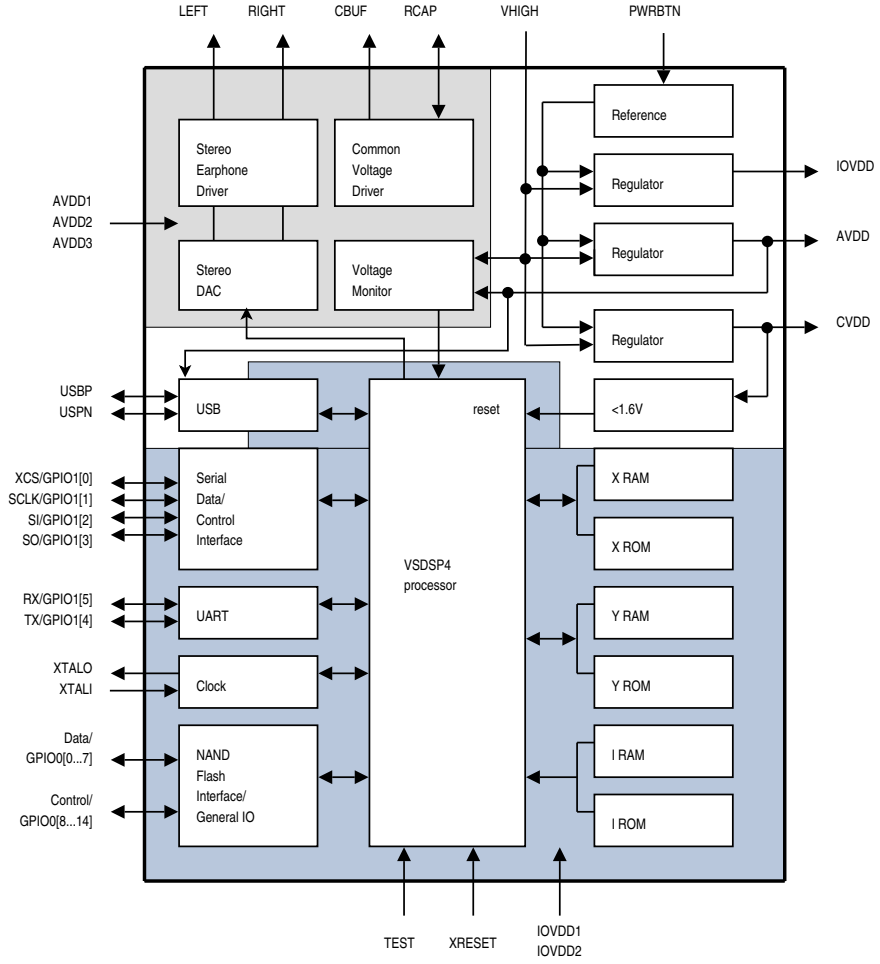


Figure 2: VS2000 Block Diagram

5.1 Regulator Section

The VHIGH pin in the regulator section is used as a common main power supply for voltage regulation. This input is connected to three internal regulators, which are activated when the PWRBTN pin is set high for about one millisecond, so that AVDD starts to rise and reaches about 1.5 V. After the PWRBTN has given this initial start current, the regulators reach their default voltages even if the PWRBTN is released. VHIGH must be sufficiently (about 0.3 V) above the highest regulated power (normally AVDD) so that regulation can be properly performed.

The PWRBTN state can also be read by software, so it can be used as one of the user interface buttons.

A power-on reset monitors the core voltage and asserts reset if CVDD drops below 1.6 V. It is also possible to force a reset by keeping PWRBTN pressed for longer than approximately 5.6 seconds. A watchdog counter and the XRESET pin can also generate a reset for the device.

Resets do not cause the regulators to shut down, but they restore the default regulator voltages. After boot the firmware and user software can change the voltages.

Return to power-off is possible only with active software control (VSDSP writes the regulator shutdown bit), or when VHIGH voltage is removed for a sufficiently long time. In the default firmware player the power button has to be pressed for 2 seconds to make the software powerdown the system and turn the regulators off.

5.2 Digital Section

Two of the regulators provide power supply for the digital section.

IOVDD is used for the level-shifters of the digital I/O and crystal oscillator. The IOVDD regulator output must be connected to IOVDD1 and IOVDD2 input pins, because they are not connected internally. Proper bypass capacitors should also be used. After reset the I/O voltage is 1.8 V, and firmware raises it to 3.3 V.

All other digital is powered from core voltage (CVDD). The core voltage is internally connected, and the CVDD pin should have a proper bypass capacitors.

Clock

The crystal amplifier uses a crystal connected to XTALI and XTALO. An external logic-level input clock can also be used. When VS2000 is used with USB, 12 MHz input clock must be used.

An internal phase-locked loop (PLL) generates the internal clock by multiplying the input clock by 1.0×, 1.5×, ..., 4.0×. In normal operating mode the clock is 4.0×12 MHz = 48 MHz. During USB suspend the PLL is off.

XRESET disables clock buffer and puts the digital section into powerdown mode.

VSDSP^4

VSDSP^4 is VLSI Solution's proprietary digital signal processor with a 32-bit instruction word, two 16-bit data buses, and both 16-bit and 32/40-bit arithmetic.

IROM, XROM, and YROM contain the firmware, including the default application. Most of the instruction RAM and some of the X and Y data RAM's can be used to customize and extend the functionality.

UART

An asynchronous serial port is used for debugging and special applications. The default speed is 115200 bps. RX and TX pins can also be used for general-purpose I/O when the UART is not required.

SPI

A synchronous serial port peripheral is used for SPI EEPROM boot, and can be used to access other SPI peripherals (for example LCD or SED) by using another chip select. The SPI is only used for boot if the XCS pin has a high level after reset (pull-up resistor attached). These pins can also be used for general-purpose I/O when the SPI is not required.

The firmware uses SPI pins SO and SCLK for ultrasound transmitter.

USB

The USB peripheral handles USB 1.1 Full Speed harware protocol. Low speed communication is not supported, but is correctly ignored. The USBP pin has a software-controllable 1.5kΩ pull-up.

A control endpoint (1 IN and 1 OUT) and upto 6 other endpoints (3 IN and 3 OUT) can be used simultaneously. Bulk, interrupt, and isochronous transfer modes are selectable for each endpoint. USB receive from USB host to device (OUT) uses a 2 KiB buffer, thus allowing very high transfer speeds. USB transmit from device to USB host (IN) also uses a 2 KiB buffer and allows all IN endpoints to be ready to transmit simultaneously. Double-buffering is also possible, but not usually required.

The firmware uses the USB peripheral to implement a 6-channel USB Audio Device and USB Human Interface Device.

5.3 Analog Section

The third regulator provides power for the analog section.

The analog section consists of digital to analog converters and earphone driver. This includes a buffered common voltage generator (CBUF, around 1.2 V) that can be used as a virtual ground for headphones.

The AVDD regulator output pin must be connected to AVDD1..AVDD3 pins with proper bypass capacitors, because they are not connected internally.

The USB pins use the internal AVDD voltage, and the firmware configures AVDD to 3.6 V when USB is attached.

Low AVDD voltage can be monitored by software. Currently the firmware does not take advantage of this feature.

CBUF contains a short-circuit protection. It disconnects the CBUF driver if pin is shorted to ground. In practise this only happens with external power regulation, because there is a limit to how much power the internal regulators can provide.

6 Firmware Operation

The firmware uses the following pins (see the example schematics in Section 7):

Pin	Description
VHIGH	VBUS with diode to VHIGH
PWRBTN	Power button starts regulator + VBUS-triggered (Mode Select)
USBN	external 1 MΩ pull-up
USBP	external 1 MΩ pull-up
GPIO0_0	external 1 MΩ pull-down resistor, Key 1 connects a 100 kΩ pull-up resistor (Vol-)
GPIO0_1	external 1 MΩ pull-down resistor, Key 2 connects a 100 kΩ pull-up resistor (Vol+)
GPIO0_2	external 1 MΩ pull-down resistor, Key 3 connects a 100 kΩ pull-up resistor (Pause)
GPIO0_3	external 1 MΩ pull-down resistor, Key 4 connects a 100 kΩ pull-up resistor (Play)
GPIO0_4	external 1 MΩ pull-down resistor, Key 5 connects a 100 kΩ pull-up resistor (Rewind)
GPIO0_5	external 1 MΩ pull-down resistor, Key 6 connects a 100 kΩ pull-up resistor (Fast Forward)
GPIO0_6	external 1 MΩ pull-down resistor, Key 7 connects a 100 kΩ pull-up resistor (Effect Level Select)
GPIO0_7	external 100 kΩ pull-up resistor
GPIO0_8	USB LED - Red
GPIO0_9	Effect Level LED - Green (PWM-controlled)
GPIO0_10	Tracking LED - Red
GPIO0_11	Tracking LED - Green
GPIO0_12	Headtracker input right
GPIO0_13	Headtracker input left
GPIO0_14	Audio LED, External power control, with 1 MΩ pull-down resistor
GPIO1_0 / XCS	external pull-up to enable SPI EEPROM boot
GPIO1_1 / SCLK	820 Hz headtracker transmit / SPI EEPROM SCLK
GPIO1_2 / SI	SPI EEPROM MISO
GPIO1_3 / SO	40 kHz headtracker transmit / SPI EEPROM MOSI
GPIO1_4 / TX	UART transmit
GPIO1_5 / RX	UART receive

Tracking LEDs indicate the operation mode:

Green On	Tracking On, RED On if tracking error is detected
Green Off, Red Off	Tracking Off, spatial processing active
Green Off, Red On	Bypass mode, no spatial processing, down-mixing only

USB LED is lit when setup packets are received, i.e. during device configuration, and when audio controls are changed.

Audio LED is lit when audio data is transferred and is turned off after a short timeout when audio transmission stops.

6.1 SPI Boot

The first boot method is SPI EEPROM. If GPIO1[0] is low after reset, SPI boot is skipped. If GPIO1[0] is high, it is assumed to have a pull-up resistor and SPI boot is tried.

First the first four bytes of the SPI EEPROM are read using 16-bit address. If the bytes are “VLSI”, a 16-bit EEPROM is assumed and the boot continues. If the last 3 bytes are read as “VLS”, a 24-bit EEPROM is assumed and boot continues in 24-bit mode. Both 16-bit and 24-bit EEPROM should have the “VLSI” string starting at address 0, and the rest of the boot data starting at address 4. If the identification is not found, SPI EEPROM boot is skipped.

Boot records are read from EEPROM until an execute record is reached. Unknown records are skipped using the data length field.

Byte	Description
0	type 0=I-mem 1=X-mem 2=Y-mem 3=execute
1,2	data len lo, hi – data length in bytes
3, 4	address lo, hi – record address
5..	data*

6.2 UART Boot/Monitor

When byte 0xef is sent to RX at 115200 bps, the firmware enters monitor mode and communicates with **vs3emu**. Memory contents can be displayed, executables can be loaded and run, or the firmware code can be restarted or continued.

The UART is also a convenient way to program or reprogram the SPI EEPROM.

6.3 Default Firmware Features

When USB cable insertion is detected by the firmware, USB handling code is started. The internal clock is configured to 4.0× 12 MHz = 48 MHz, the analog power is configured to 3.6 V, the core power to 2.5 V, the USB peripheral is initialized, and the USB pull-up resistor is enabled.

In addition to the power button, upto 7 keys are connected to GPIO0[6..0] so that they connect a 100 kΩ pull-up to the I/O when the button is pressed, and 1 MΩ pull-downs keep the lines low otherwise.

Some of the keys are used for different direct modes, the rest are available to PC through USB Human Interface Device.

6.3.1 USB Audio Device

VS2000 appears as an USB Composite Device with USB Audio Device and USB Human Interface Device. The USB Audio Device has 6 16-bit channels, and a feature unit that includes master volume, master mute, master bass, and master treble controls. These controls can be changed using system tools (in Windows using the volume control panel and advanced audio settings).

Headtracker transmit is only enabled when audio transmission is active.

6.3.2 USB Human Interface Device

The USB Human Interface Device (HID) transmits information about the state of the device buttons to the host machine. With proper software HID can also be used for reading and writing VS2000 memory, for example monitoring the headtracker state, and changing some advanced features.

Volume Decrement, Volume Increment

Volume can be turned up or down with 0.5 dB steps using the volume buttons. A short press changes the volume by 0.5 dB, a long press will change the volume by approximately 8 dB every second. Using the volume buttons is always possible, regardless of whether the host machine supports USB Human Interface Devices or not.

If the host machine supports USB Human Interface Devices, it can detect the press of volume buttons and set the volume using the USB Audio Device controls.

Pause, Play, Rewind, Fast Forward

These buttons are Human Interface Device buttons only. Their operation depends on the host machine, and the application that is active at the time.

Power Button

A press of the power button turns on the system. Insertion of the device to the USB port can also turn the unit on.

A long press (2 seconds) of the power button will turn off the device.

Short press of the power button switches the processing mode between Tracking On, Tracking Off, and Bypass.

In both tracking modes the full 3D processing is active. In the bypass-mode the 3D processing is replaced by a simple 6-channel to 2-channel matrixing operation.

The power button is not a Human Interface Device button.

Effect Level Button

The effect level button selects between four predefined levels of room response. The default levels are *off*, *low*, *medium*, and *high*. The default setting is the *medium* level.

The effect level button is not a Human Interface Device button.

7 Example Application

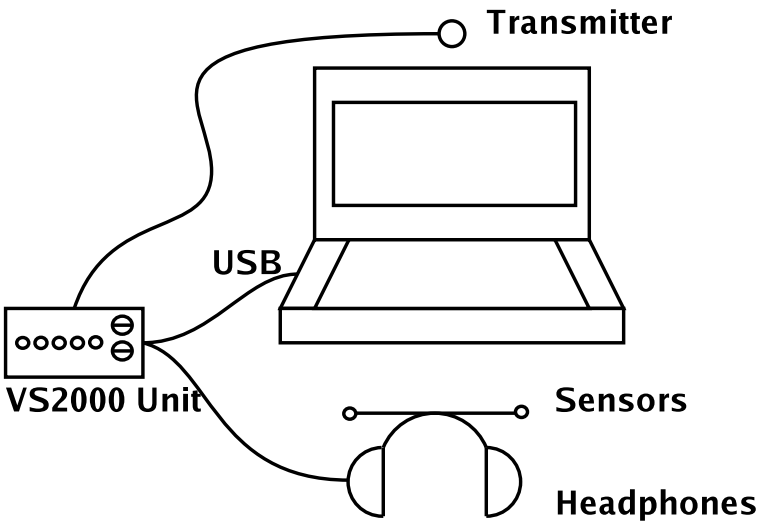


Figure 3: VS2000 Example Application

The example application consists of five parts.

1. VS2000 Unit - contains the VS2000 chip and other active electronics, buttons and LEDs.
2. Transmitter - ultrasound transmitter element, is powered and controlled by VS2000 Unit.
3. Sensors - ultrasound receivers, are read by VS2000 Unit.
4. USB - the audio source. USB also powers the system.
5. Headphones - for audio output.

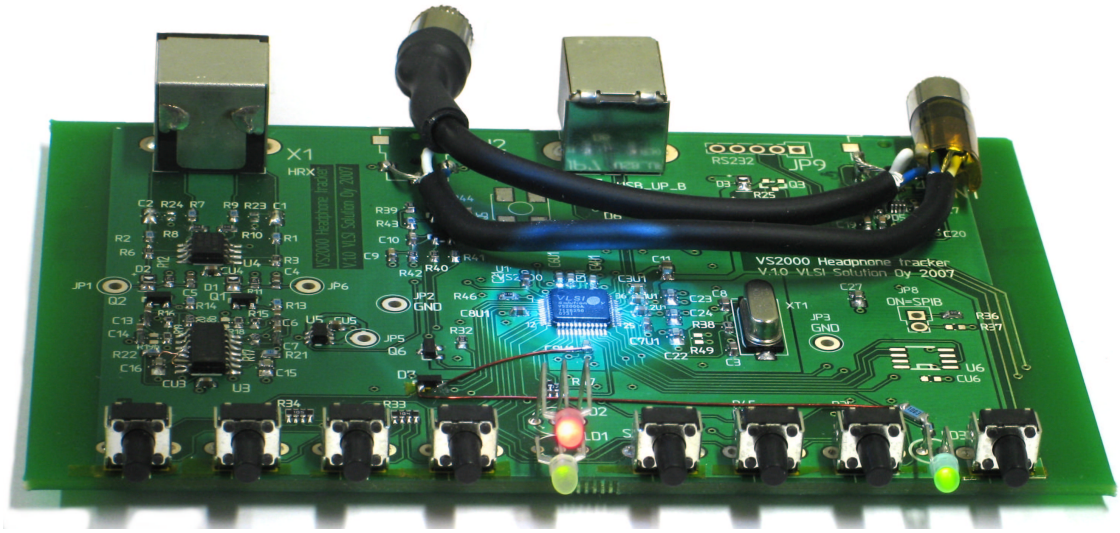
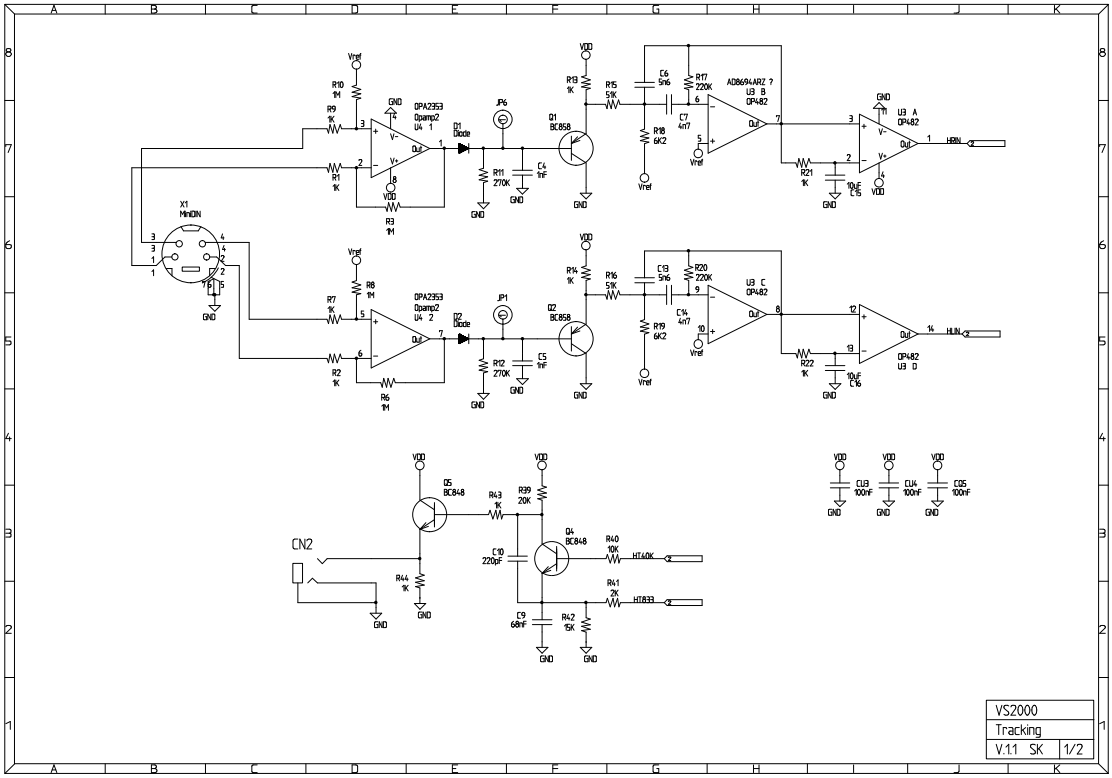


Figure 4: VS2000 Unit



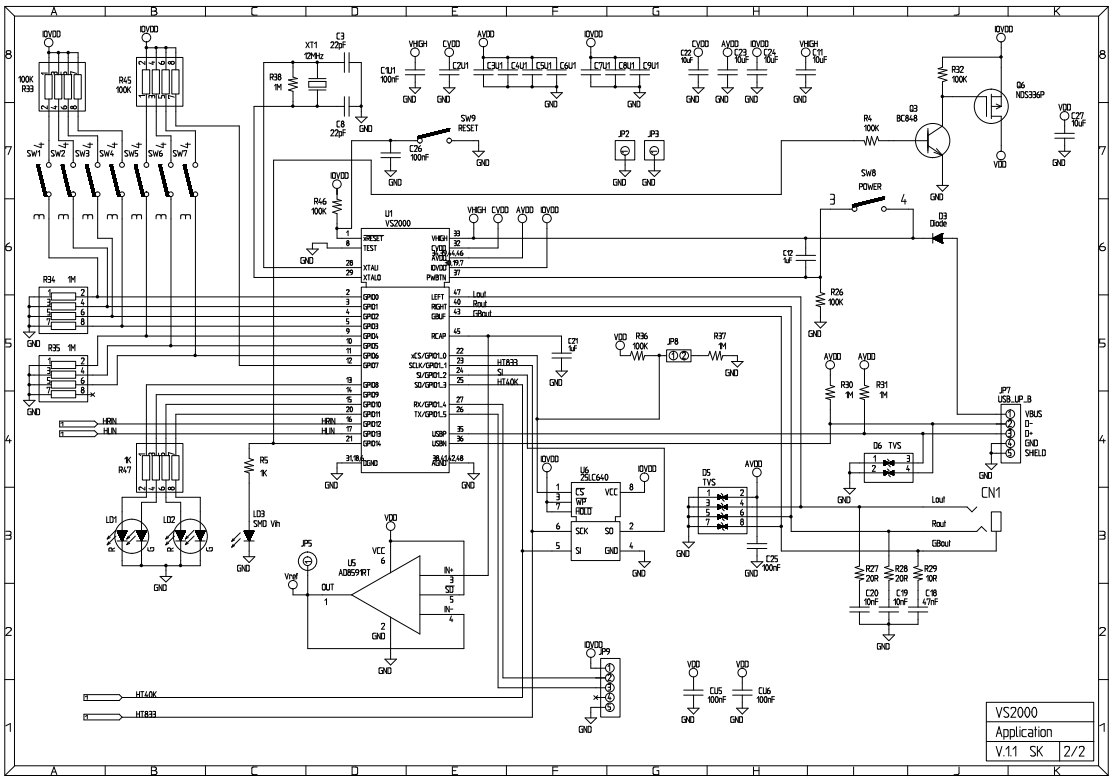


Figure 5: VS2000 Example Schematic

7.1 Usage Hints

Linux

Mplayer requires the following options to play the 6-channel audio instead of 2-channel: `-channels 6 -af channels=6:6:0:0:1:1:2:4:3:5:4:2:5:3`. The first option selects six channels, and the second option corrects the channel mapping. Mplayer does not determine the output channel mapping automatically.

Also an option like `-ao alsa:device=hw=1.0` may be needed to select the USB Audio Device in case the system has multiple audio devices.

MAC

The MAC system player seems to only play the two-channel mix of a DVD, and can not be configured for multi-channel sound, as far as we could determine.

Mplayer requires the following options to play the 6-channel audio instead of 2-channel: `-channels 6 -af channels=6:6:0:0:1:1:2:4:3:5:4:2:5:3`. The first option selects six channels, and the second option corrects the channel mapping. Mplayer does not determine the output channel mapping automatically.

Windows 2000Pro, XP, Vista

Windows MediaPlayer should play all the channels and it also processes the channel order information, thus plays the channels in the right order. Some old third-party DVD player applications only play 2-channel audio.

8 Document Version Changes

This chapter describes the most important changes to this document.

8.1 Version 0.3, 2007-09-05

- Example application picture and board photo added.
- First public release.

8.2 Version 0.2, 2007-08-31

- Headtracker left and right swapped.
- Example schematic and pictures updated.
- Usage hints chapter added.

8.3 Version 0.1, 2007-06-15

- First pre-release version.

9 Contact Information

VLSI Solution Oy
Entrance G, 2nd floor
Hermiankatu 8
FIN-33720 Tampere
FINLAND

Fax: +358-3-3140-8288
Phone: +358-3-3140-8200
Email: sales@vlsi.fi
URL: http://www.vlsi.fi/