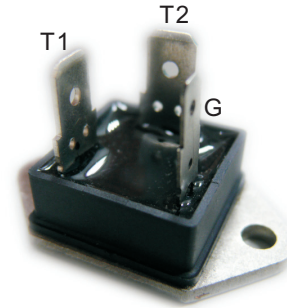


# TRIACs, 40A Sunbberless

## FEATURES

- High current triac
- Low thermal resistance with clip bonding
- Low thermal resistance insulation ceramic for insulated TO-3 package
- High commutation capability
- Packages are RoHS compliant



## APPLICATIONS

The snubberless concept offer suppression of RC network and it is suitable for applications such as on/off function in static relays, heating regulation, induction motor starting circuits, phase control operation in light dimmers, motor speed controllers, and silmilar.

Due to their clip assembly techinque, they provide a superior performance in surge current handling capabilities.

By using an internal ceramic pad, the M40T series provides voltage insulated tab (rated at 2500VRMS) complying with UL standards.

## MAIN FEATURES

SYMBOL	VALUE	UNIT
$I_{T(RMS)}$	40	A
$V_{DRM}/V_{RRM}$	600 to 1200	V
$I_{GT(Q1)}$	10 to 50	mA

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS		VALUE	UNIT
RMS on-state current (full sine wave)	$I_{T(RMS)}$	TO-3	$T_c = 90^\circ\text{C}$	40	A
Non repetitive surge peak on-state current (full cycle, $T_j$ initial = $25^\circ\text{C}$ )	$I_{TSM}$	F = 50 Hz	t = 20 ms	400	A
		F = 60 Hz	t = 16.7 ms	420	
$I^2t$ Value for fusing	$I^2t$	$t_p = 10$ ms		800	$\text{A}^2\text{s}$
Critical rate of rise of on-state current $I_G = 2xI_{GT}$ , $t_r \leq 100\text{ns}$	dI/dt	F = 100 Hz	$T_j = 125^\circ\text{C}$	50	A/ $\mu\text{s}$
Peak gate current	$I_{GM}$	$T_p = 20 \mu\text{s}$	$T_j = 125^\circ\text{C}$	4	A
Peak gate power dissipation ( $t_p = 20\mu\text{s}$ )	$P_{GM}$	$T_j = 125^\circ\text{C}$		10	W
Average gate power dissipation	$P_{G(AV)}$	$T_j = 125^\circ\text{C}$		1	
Storage temperature range	$T_{stg}$			- 40 to + 150	$^\circ\text{C}$
Operating junction temperature range	$T_j$			- 40 to + 125	

© ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$  unless otherwise specified)

SNUBBERLESS and Logic level (3 quadrants)					
SYMBOL	TEST CONDITIONS	QUADRANT		Limits	Unit
				BW	
$I_{GT}^{(1)}$	$V_D = 12\text{ V}, R_L = 33\Omega$	I - II - III	MAX.	50	mA
$V_{GT}$		I - II - III		1.3	
$V_{GD}$	$V_D = V_{DRM}, R_L = 3.3K\Omega$ $T_j = 125^\circ\text{C}$	I - II - III	MIN.	0.2	V
$I_H^{(2)}$	$I_T = 500\text{ mA}$		MAX.	60	mA
$I_L$	$I_G = 1.2 I_{GT}$	I - III	MAX.	80	mA
		II		100	
$dV/dt^{(2)}$	$V_D = 67\% V_{DRM}, \text{gate open}, T_j = 125^\circ\text{C}$		MIN.	1000	$V/\mu\text{s}$
$(dl/dt)_c^{(2)}$	Without snubber, $T_j = 125^\circ\text{C}$			20	A/ms

STATIC CHARACTERISTICS					
SYMBOL	TEST CONDITIONS			VALUE	UNIT
$V_{TM}^{(2)}$	$I_{TM} = 60\text{ A}, t_P = 380\text{ }\mu\text{s}$	$T_j = 25^\circ\text{C}$	MAX.	1.55	V
$V_{I0}^{(2)}$	Threshold voltage	$T_j = 125^\circ\text{C}$	MAX.	0.85	V
$R_d^{(2)}$	Dynamic resistance	$T_j = 125^\circ\text{C}$	MAX.	10	$m\Omega$
$I_{DRM}$ $I_{RRM}$	$V_D = V_{DRM}$ $V_R = V_{RRM}$	$T_j = 25^\circ\text{C}$	MAX.	10	$\mu\text{A}$
		$T_j = 125^\circ\text{C}$		5	mA

Note 1: Minimum  $I_{GT}$  is guaranteed at 5% of  $I_{GT}$  max.

Note 2: For both polarities of A2 referenced to A1.

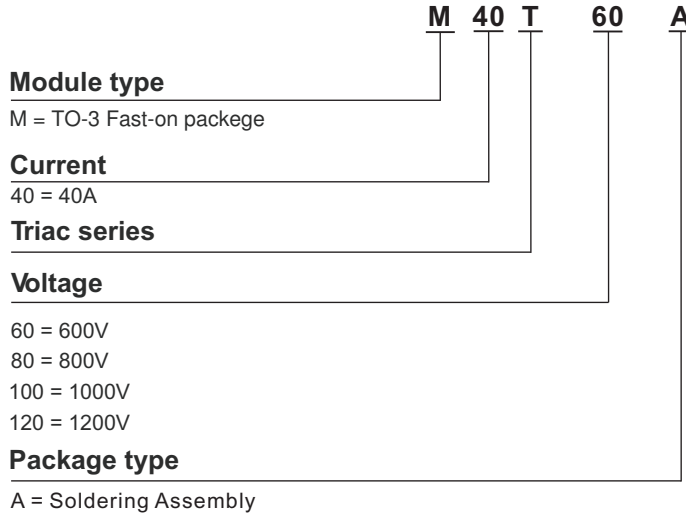
THERMAL RESISTANCE			
SYMBOL		VALUE	UNIT
$R_{th(j-c)}$	Junction to case (AC)	0.8	$^\circ\text{C/W}$
$R_{th(j-a)}$	Junction to ambient	50	

S = Copper surface under tab.

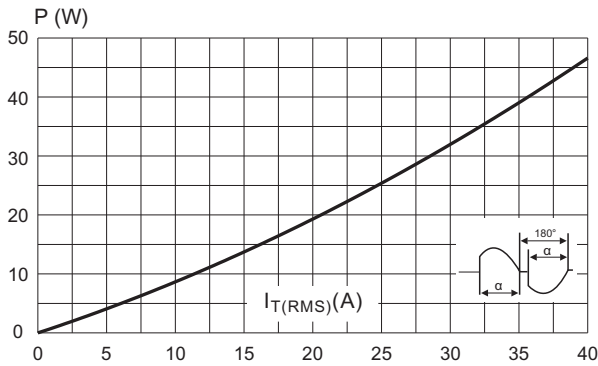
PRODUCT SELECTOR							
PART NUMBER	VOLTAGE (xx)				SENSITIVITY	TYPE	PACKAGE
	600 V	800 V	1000 V	1200 V			
M40TxxA	V	V	V	V	50 mA	Snubberless	TO-3

ORDERING INFORMATION					
ORDERING TYPE	MARKING	PACKAGE	WEIGHT	BASE Q'TY	DELIVERY MODE
M40TxxA	M40TxxA	TO-3	23g	50	BOX

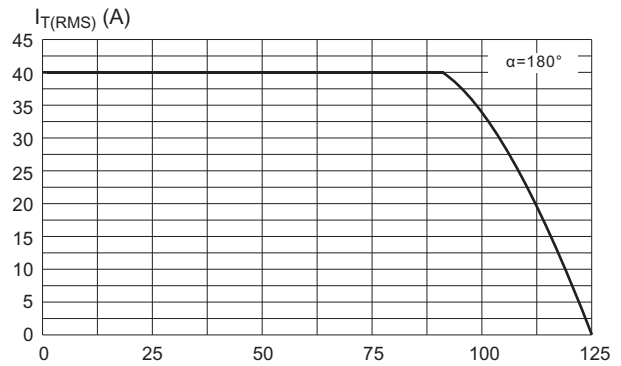
## ORDERING INFORMATION SCHEME



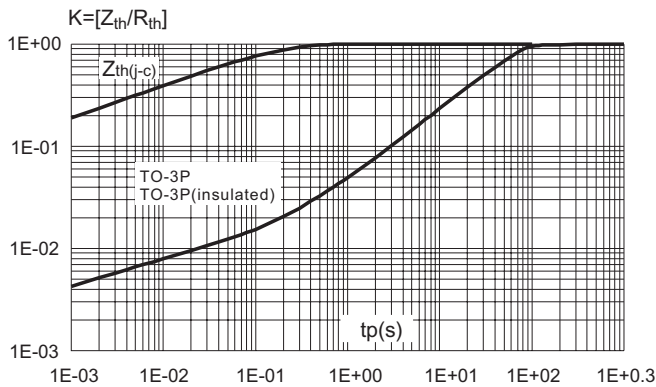
**Fig.1 Maximum power dissipation versus on-state rms current (full cycle)**



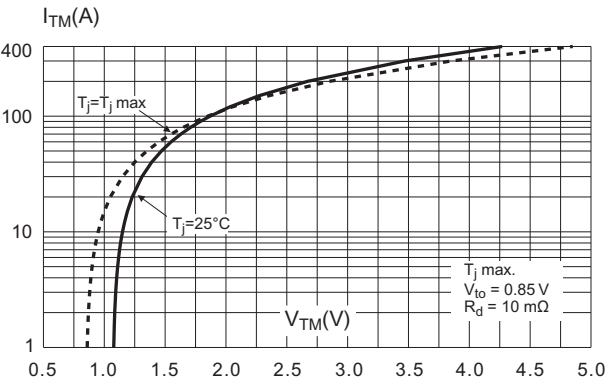
**Fig.2 On-state rms current versus case temperature (full cycle)**



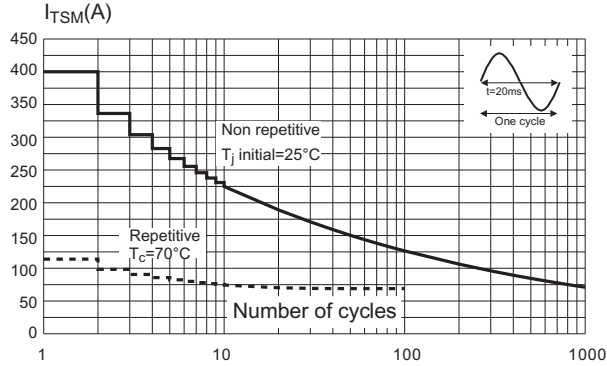
**Fig.3 Relative variation of thermal impedance versus pulse duration.**



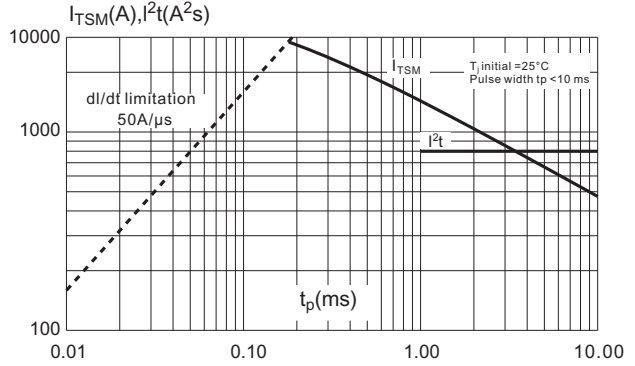
**Fig.4 On-state characteristics (maximum values).**



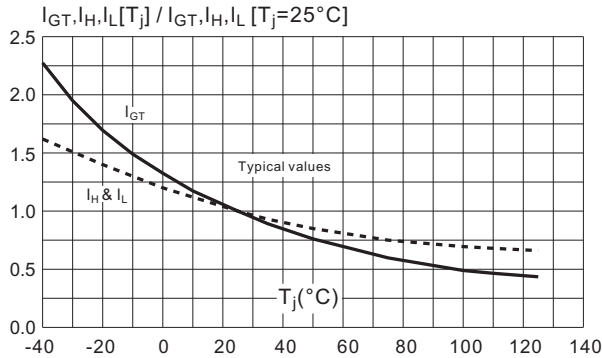
**Fig.5 Surge peak on-state current versus number of cycles.**



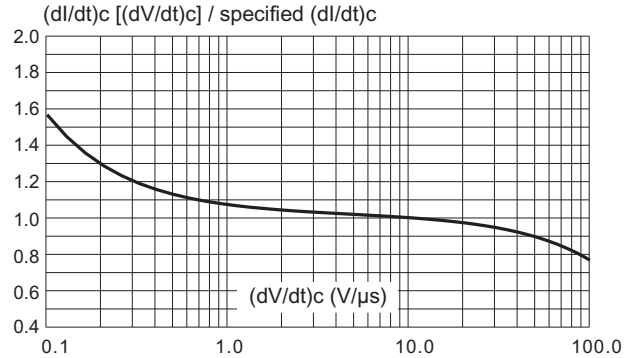
**Fig.6 Non-repetitive surge peak on-state current for a sinusoidal pulse and corresponding value of  $I^2t$ .**



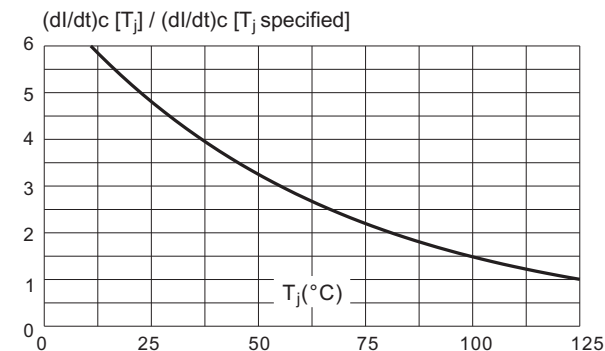
**Fig.7 Relative variation of gate trigger, holding and latching current versus junction temperature.**

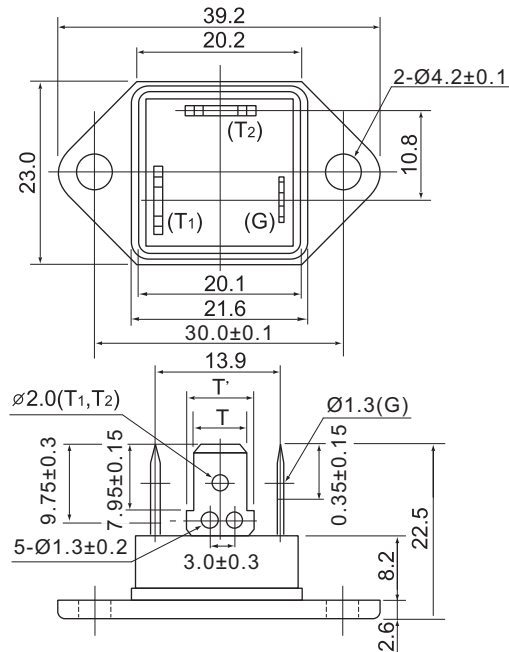


**Fig.8 Relative variation of critical rate of decrease of main current versus  $(dV/dt)_c$  (typical values).**



**Fig.9 Relative variation of critical rate of decrease of main current versus  $(dV/dt)_c$ .**





T<sub>1</sub>:TAB250(T=6.35, T'=8.25, t=0.8)  
 T<sub>2</sub>:TAB250(T=6.35, T'=8.25, t=0.8)  
 G:TAB187(T=4.75, T'=5.7, t=0.5)

All dimensions in millimeters