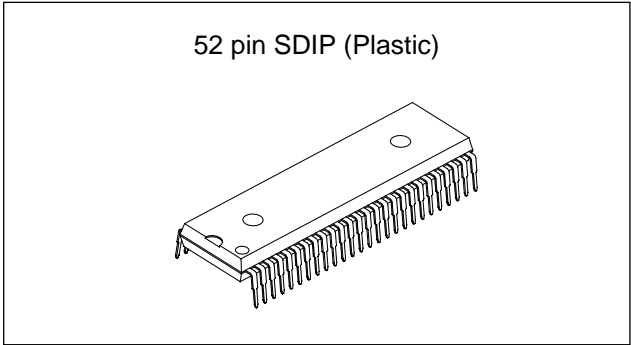


CMOS 8-bit Single Chip Microcomputer

Description

The CXP86609/86613/86617 are the CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, I²C bus interface, PWM output, remote control reception circuit, watchdog timer, 32kHz timer/counter besides the basic configurations of 8-bit CPU, ROM, RAM, I/O ports.

The CXP86609/86613/86617 also provide a sleep function that enables to lower the power consumption.



Structure

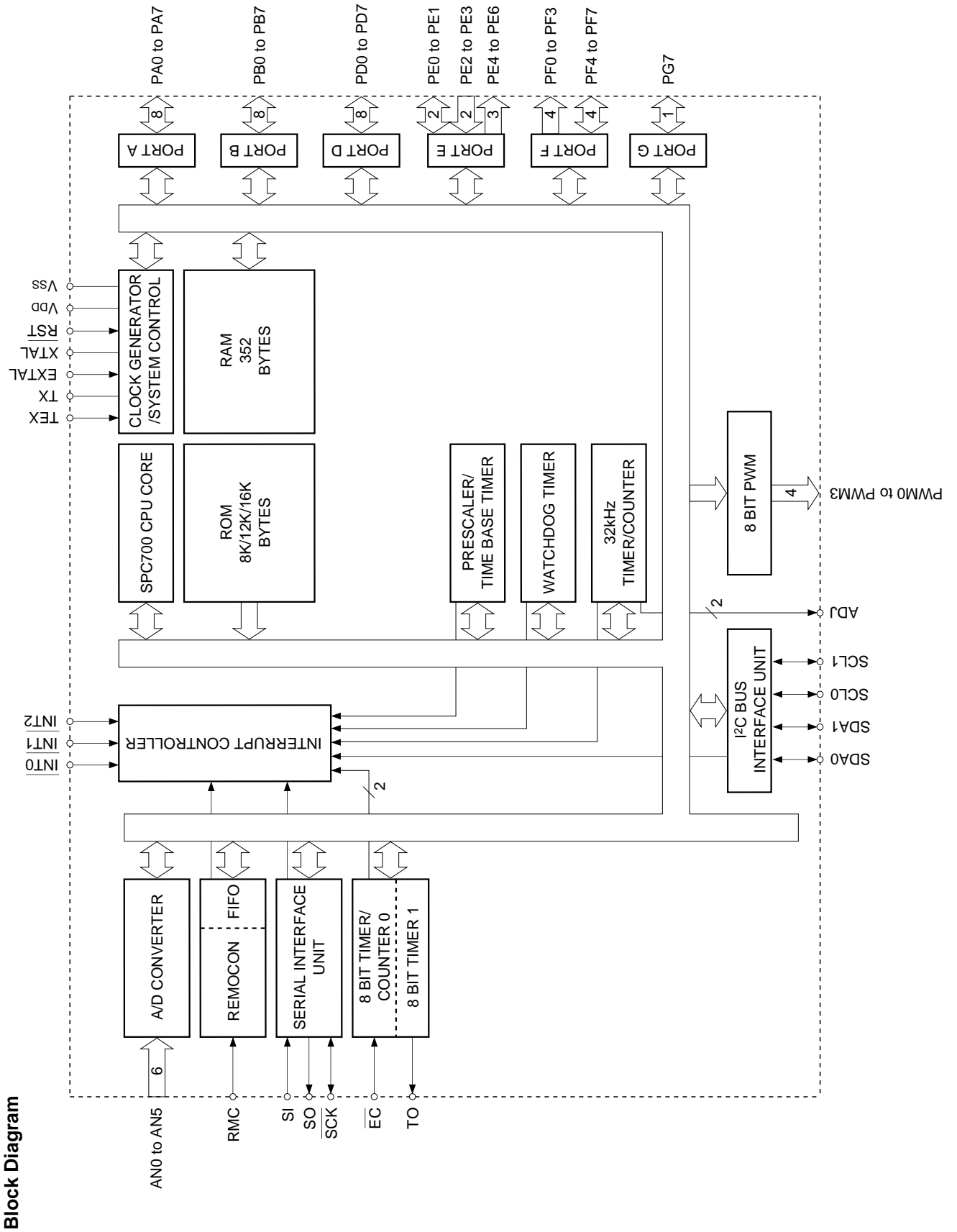
Silicon gate CMOS IC

Features

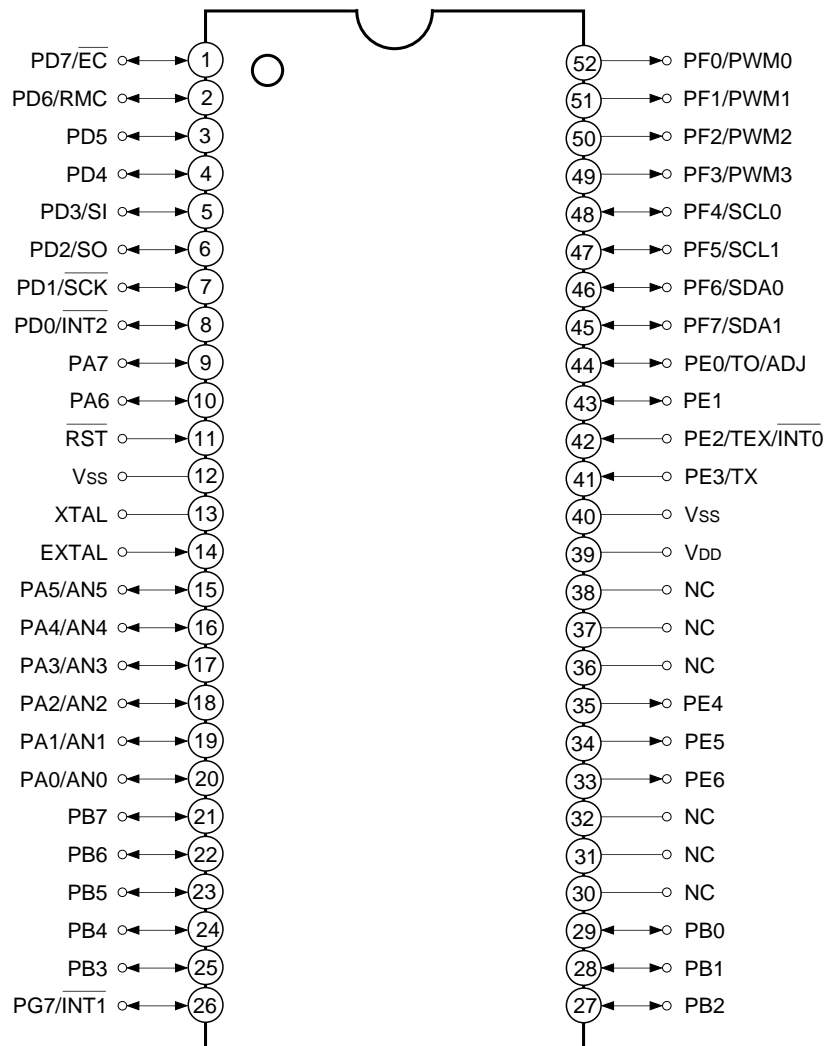
- A wide instruction set (213 instructions) which covers various types of data
 - 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle 250ns at 16MHz operation
 122µs at 32kHz operation
- Incorporated ROM 8K bytes (CXP86609)
 12K bytes (CXP86613)
 16K bytes (CXP86617)
- Incorporated RAM 352 bytes
- Peripheral functions
 - A/D converter 8 bits, 6 channels, successive approximation method
 (Conversion time of 3.25µs at 16MHz)
 - Serial interface 8-bit clock sync type, 1 channel
 - Timer 8-bit timer
 8-bit timer/counter
 19-bit time-base timer
 32kHz timer/counter
 - I²C bus interface
 - PWM output 8 bits, 4 channels
 - Remote control reception circuit 8-bit pulse measurement counter, 6-stage FIFO
 - Watchdog timer
- Interruption 11 factors, 11 vectors, multi-interruption possible
- Standby mode Sleep
- Package 52-pin plastic SDIP
- Piggyback/evaluator CXP86490 64-pin ceramic PSDIP

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Pin Assignment (Top View)



- Note)**
1. NC (Pins 30, 31, 32, 36 and 38) are left open.
 2. V_{SS} (Pins 12 and 40) are both connected to GND.
 3. Pin 37 is the NC pin. However, connect it to V_{DD} because it is the EXLC pin (input) for the piggyback/evaluator and OTP devices.

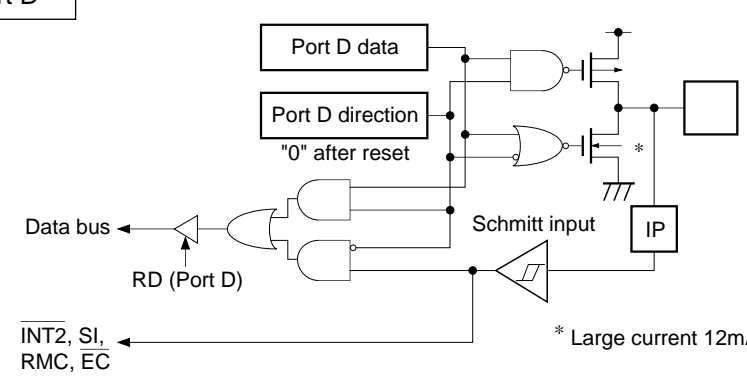
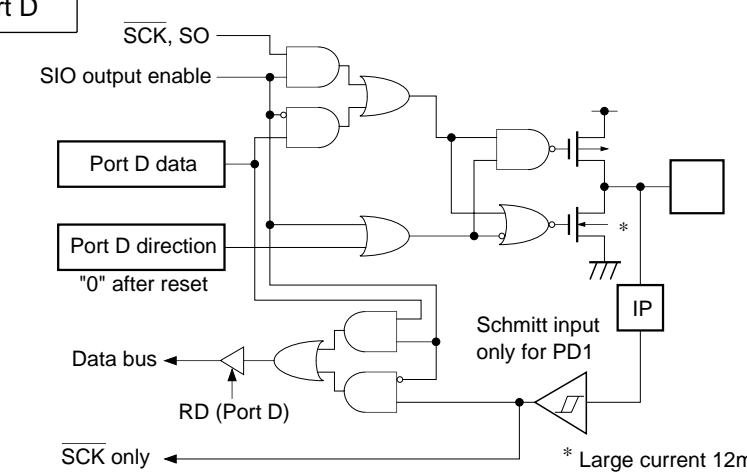
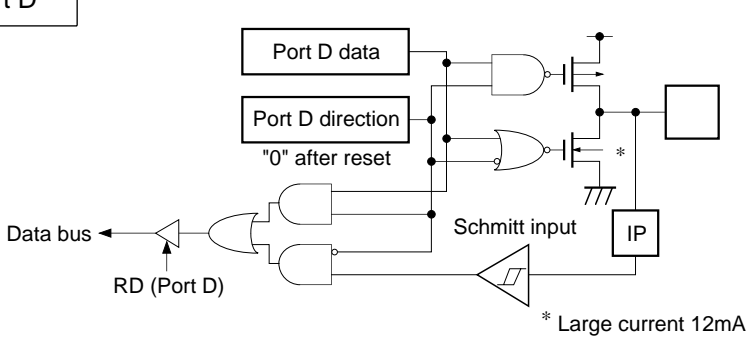
Pin Description

| Symbol | I/O | Description | | |
|-----------------------------------|-----------------------|--|--|--|
| PA0/AN0 to PA5/AN5 | I/O/ Analog input | (Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins) | Analog inputs to A/D converter. (6 pins) | |
| PA6 to PA7 | I/O | | | |
| PB0 to PB7 | I/O | (Port B) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins) | | |
| PD0/ $\overline{\text{INT2}}$ | I/O/Input | (Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sink current. (8 pins) | External interruption request input. Active at the falling edge. | |
| PD1/ $\overline{\text{SCK}}$ | I/O/I/O | | Serial clock I/O. | |
| PD2/SO | I/O/Output | | Serial data output. | |
| PD3/SI | I/O/Input | | Serial data input. | |
| PD4 to PD5 | I/O | | | |
| PD6/RMC | I/O/Input | | Remote control reception circuit input. | |
| PD7/ $\overline{\text{EC}}$ | I/O/Input | | External event input for timer/counter. | |
| PE0/TO/ADJ | I/O/Output/ Output | (Port E) Bits 0 and 1 are I/O port; I/O can be set in a unit of single. Bits 2 and 3 are input port. Bits 4, 5 and 6 are output port. (7 pins) | Rectangular wave output for 8-bit timer/counter. | |
| PE1 | I/O | | 32kHz oscillation frequency dividing output. | |
| PE2/TEX/ $\overline{\text{INT0}}$ | Input/Input/ Input | | Connects a crystal for 32kHz timer/counter clock oscillation. | External interruption request input. Active at the falling edge. |
| PE3/TX | Input/Output | | When used as an event counter, input to TEX pin and leave TX pin open. | |
| PE4 to PE6 | Output | | | |

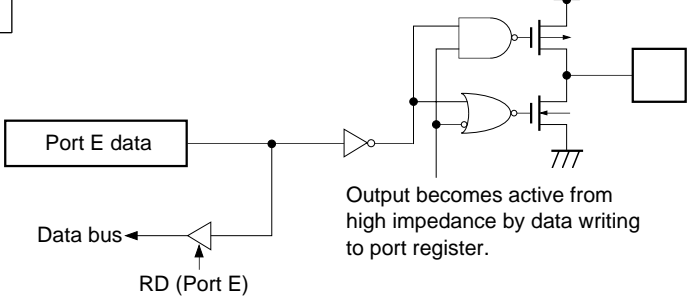
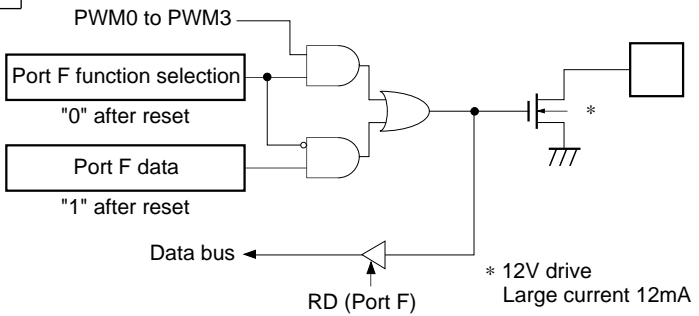
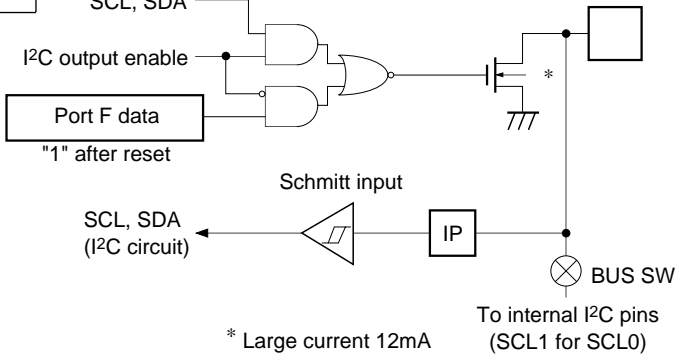
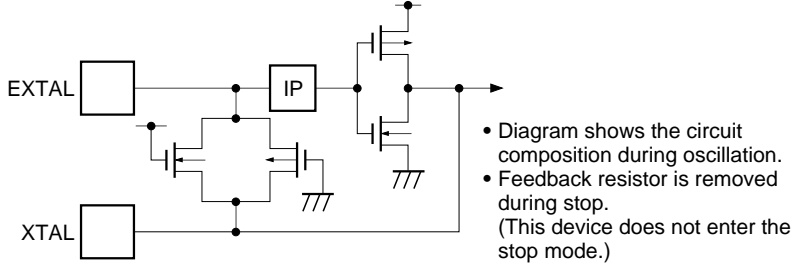
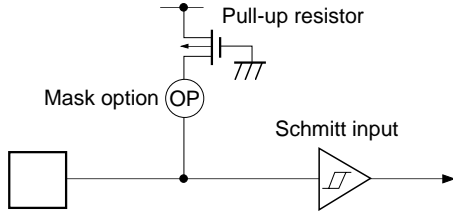
| Symbol | I/O | Description | |
|-------------------------------|---------------|--|--|
| PF0/PWM0 to PF3/PWM3 | Output/Output | (Port F) 8-bit output port and large current (12mA) | 8-bit PWM output. (4 pins) |
| PF4/SCL0 to PF5/SCL1 | Output/I/O | N-channel open drain output. Lower 4 bits are medium voltage drive (12V); | I ² C bus interface transfer clock I/O. (2 pins) |
| PF6/SDA0 to PF7/SDA1 | Output/I/O | upper 4 bits are 5V drive. (8 pins) | I ² C bus interface transfer data I/O. (2 pins) |
| PG7/ $\overline{\text{INT1}}$ | I/O/Input | (Port G) 1-bit I/O port. I/O can be set in a unit of single bits. (1 pin) | External interruption request input. Active at the falling edge. |
| EXTAL | Input | Connects a crystal for system clock oscillation. When a clock is supplied externally, input to EXTAL pin and input a reversed phase clock to XTAL pin. | |
| XTAL | Output | | |
| $\overline{\text{RST}}$ | Input | System reset; active at Low level. | |
| NC | | No connected. Connect this pin to V _{DD} under normal operation. | |
| V _{DD} | | Positive power supply. | |
| V _{SS} | | GND. Connect two V _{SS} pins to GND. | |

Input/Output Circuit Formats for Pins

| Pin | Circuit format | After reset |
|---|--|-------------|
| <p>PA0/AN0 to PA5/AN5</p> <p>6 pins</p> | <p>Port A</p> <p>Port A data</p> <p>Port A direction</p> <p>"0" after reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A function selection</p> <p>"0" after reset</p> <p>A/D converter</p> <p>Input multiplexer</p> <p>IP</p> <p>Input protection circuit</p> | <p>Hi-Z</p> |
| <p>PA6</p> <p>PA7</p> <p>2 pins</p> | <p>Port A</p> <p>Port A data</p> <p>Port A direction</p> <p>"0" after reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Schmitt input</p> <p>IP</p> | <p>Hi-Z</p> |
| <p>PB0 to PB7</p> <p>PG7/INT1</p> <p>9 pins</p> | <p>Port B</p> <p>Port G</p> <p>Ports B, G data</p> <p>Ports B, G direction</p> <p>"0" after reset</p> <p>Data bus</p> <p>RD (Ports B, G)</p> <p>Schmitt input only for PG7</p> <p>IP</p> <p>INT1</p> | <p>Hi-Z</p> |

| Pin | Circuit format | After reset |
|--|--|-------------|
| <p>PD0/$\overline{\text{INT2}}$ PD3/SI PD6/RMC PD7/$\overline{\text{EC}}$</p> <p>4 pins</p> | <p>Port D</p>  <p>* Large current 12mA</p> | <p>Hi-Z</p> |
| <p>PD1/$\overline{\text{SCK}}$ PD2/SO</p> <p>2 pins</p> | <p>Port D</p>  <p>* Large current 12mA</p> | <p>Hi-Z</p> |
| <p>PD4 PD5</p> <p>2 pins</p> | <p>Port D</p>  <p>* Large current 12mA</p> | <p>Hi-Z</p> |

| Pin | Circuit format | After reset |
|---|--|---|
| <p>PE0/TO/ADJ</p> <p>1 pin</p> | <p>Port E</p> <p>Internal reset signal</p> <p>Port E data "1" after reset TO *1 ADJ16K *1 ADJ2K *1</p> <p>MPX</p> <p>00 01 10 11</p> <p>Port E function selection (upper) Port E function selection (lower) "00" after reset</p> <p>Port E direction "1" after reset</p> <p>Data bus</p> <p>RD (Port E)</p> <p>*1 ADJ signals are frequency dividing outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.</p> <p>*2 Pull-up transistor approx. 150kΩ</p> | <p>High level (with the resistor of pull-up transistor ON when reset)</p> |
| <p>PE1</p> <p>1 pin</p> | <p>Port E</p> <p>Port E data "1" after reset</p> <p>Port E direction "1" after reset</p> <p>Data bus</p> <p>RD (Port E)</p> | <p>High level</p> |
| <p>PE2/TEX/$\overline{\text{INT0}}$ PE3/TX</p> <p>2 pins</p> | <p>Port E</p> <p>32kHz oscillation circuit control</p> <p>"1" after reset Schmitt input</p> <p>$\overline{\text{INT0}}$</p> <p>Data bus</p> <p>RD (Port E)</p> <p>Data bus</p> <p>RD (Port E)</p> <p>Schmitt input</p> <p>Clock input</p> <p>PE2/ TEX/ $\overline{\text{INT0}}$</p> <p>PE3/ TX</p> | <p>Oscillation stop Port input</p> |

| Pin | Circuit format | After reset |
|--|--|-------------------------------|
| <p>PE4 PE5 PE6</p> <p>3 pins</p> | <p>Port E</p>  <p>Port E data</p> <p>Data bus</p> <p>RD (Port E)</p> <p>Output becomes active from high impedance by data writing to port register.</p> | <p>Hi-Z</p> |
| <p>PF0/PWM0 to PF3/PWM3</p> <p>4 pins</p> | <p>Port F</p> <p>PWM0 to PWM3</p> <p>Port F function selection "0" after reset</p> <p>Port F data "1" after reset</p>  <p>Data bus</p> <p>RD (Port F)</p> <p>* 12V drive Large current 12mA</p> | <p>Hi-Z</p> |
| <p>PF4/SCL0 PF5/SCL1 PF6/SDA0 PF7/SDA1</p> <p>4 pins</p> | <p>Port F</p> <p>SCL, SDA</p> <p>I²C output enable</p> <p>Port F data "1" after reset</p>  <p>SCL, SDA (I²C circuit)</p> <p>Schmitt input</p> <p>IP</p> <p>BUS SW</p> <p>To internal I²C pins (SCL1 for SCL0)</p> <p>* Large current 12mA</p> | <p>Hi-Z</p> |
| <p>EXTAL XTAL</p> <p>2 pins</p> |  <p>EXTAL</p> <p>XTAL</p> <p>IP</p> <ul style="list-style-type: none"> • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop. (This device does not enter the stop mode.) | <p>Oscillation</p> |
| <p>$\overline{\text{RST}}$</p> <p>1 pin</p> |  <p>Pull-up resistor</p> <p>Mask option OP</p> <p>Schmitt input</p> | <p>Low level (when reset)</p> |

Absolute Maximum Ratings

(V_{SS} = 0V reference)

| Item | Symbol | Ratings | Unit | Remarks |
|---------------------------------|-------------------|----------------|------|--|
| Supply voltage | V _{DD} | -0.3 to +7.0 | V | |
| Input voltage | V _{IN} | -0.3 to +7.0*1 | V | |
| Output voltage | V _{OUT} | -0.3 to +7.0*1 | V | |
| Medium drive output voltage | V _{OUTP} | -0.3 to +15.0 | V | |
| High level output current | I _{OH} | -5 | mA | |
| High level total output current | ∑I _{OH} | -50 | mA | Total of all output pins |
| Low level output current | I _{OL} | 15 | mA | Ports excluding large current output (value per pin) |
| | I _{OLC} | 20 | mA | Large current output ports (value per pin*2) |
| Low level total output current | ∑I _{OL} | 130 | mA | Total of all output pins |
| Operating temperature | T _{opr} | -20 to +75 | °C | |
| Storage temperature | T _{stg} | -55 to +150 | °C | |
| Allowable power dissipation | P _D | 375 | mW | SDIP-52P-01 |

*1 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*2 The large current output port is Port D (PD) and Port F (PF).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

| Item | Symbol | Min. | Max. | Unit | Remarks |
|--------------------------|-------------------|-----------------------|-----------------------|------|--|
| Supply voltage | V _{DD} | 4.5 | 5.5 | V | Guaranteed operation range for 1/2 and 1/4 frequency dividing clocks |
| | | 3.5 | 5.5 | V | Guaranteed operation range for 1/16 frequency dividing clock or sleep mode |
| | | 2.7 | 5.5 | V | Guaranteed operation range for TEX |
| | | — | — | V | Guaranteed data hold range for stop*1 |
| High level input voltage | V _{IH} | 0.7V _{DD} | V _{DD} | V | *2 |
| | V _{IHS} | 0.8V _{DD} | V _{DD} | V | *3 |
| | V _{IHEX} | V _{DD} - 0.4 | V _{DD} + 0.3 | V | EXTAL pin*4, TEX pin*5 |
| Low level input voltage | V _{IL} | 0 | 0.3V _{DD} | V | *2 |
| | V _{ILS} | 0 | 0.2V _{DD} | V | *3 |
| | V _{ILEX} | -0.3 | 0.4 | V | EXTAL pin*4, TEX pin*5 |
| Operating temperature | T _{opr} | -20 | +75 | °C | |

*1 This device does not enter the stop mode.

*2 PA0 to PA5, PB0 to PB7, PD2, PE0, PE1, PE3, SCL0, SCL1, SDA0, SDA1 pins

*3 PA6, PA7, INT2, SCK, SI, PD4, PD5, RMC, EC, INT0, INT1, RST pins

*4 Specifies only during external clock input.

*5 Specifies only during external event count input.

Electrical Characteristics

DC characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

| Item | Symbol | Pins | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|--|------------------------|------|------|------|
| High level output voltage | VOH | PA, PB, PD, PE0 to PE1, PE4 to PE6, PG7 | VDD = 4.5V, IOH = -0.5mA | 4.0 | | | V |
| | | | VDD = 4.5V, IOH = -1.2mA | 3.5 | | | V |
| Low level output voltage | VOL | PA, PB, PD, PE0 to PE1, PE4 to PE6, PF0 to PF3, PG7 | VDD = 4.5V, IOL = 1.8mA | | | 0.4 | V |
| | | | VDD = 4.5V, IOL = 3.6mA | | | 0.6 | V |
| | | PD, PF | VDD = 4.5V, IOL = 12.0mA | | | 1.5 | V |
| | | PF4 to PF7 (SCL0, SCL1, SDA0, SDA1) | VDD = 4.5V, IOL = 3.0mA | | | 0.4 | V |
| | | | VDD = 4.5V, IOL = 4.0mA | | | 0.6 | V |
| Input current | IiHE | EXTAL | VDD = 5.5V, VIH = 5.5V | 0.5 | | 40 | μA |
| | IiLE | | | VDD = 5.5V, VIL = 0.4V | -0.5 | | -40 |
| | IiHT | TEX | VDD = 5.5V, VIH = 5.5V | 0.1 | | 10 | μA |
| | IiLT | | | VDD = 5.5V, VIL = 0.4V | -0.1 | | -10 |
| | IiLR | RST*1 | VDD = 5.5V, VIL = 0.4V | -1.5 | | -400 | μA |
| I/O leakage current | IIZ | PA, PB, PD, PE, PG7, RST*1 | VDD = 5.5V, VI = 0, 5.5V | | | ±10 | μA |
| Open drain I/O leakage current (in N-ch Tr off state) | ILOH | PF0 to PF3 | VDD = 5.5V, VOH = 12.0V | | | 50 | μA |
| | | PF4 to PF7 | VDD = 5.5V, VOH = 5.5V | | | 10 | μA |
| I ² C bus switch connection impedance (in output Tr off state) | RBS | SCL0: SCL1 SDA0: SDA1 | VDD = 4.5V VSCL0 = VSCL1 = 2.25V VSDA0 = VSDA1 = 2.25V | | | 120 | Ω |
| Supply current*2 | IDD1 | VDD | 1/2 frequency dividing clock operation | | 18 | 28 | mA |
| | | | VDD = 5.5V, 16MHz crystal oscillation (C1 = C2 = 15pF) | | | | |
| | IDD2 | | VDD = 3.3V, 32MHz crystal oscillation (C1 = C2 = 47pF) | | 30 | 80 | μA |
| | IDDS1 | | Sleep mode | | 1.2 | 2.1 | mA |
| | | | VDD = 5.5V, 16MHz crystal oscillation (C1 = C2 = 15pF) | | | | |
| IDDS2 | VDD = 3.3V, 32MHz crystal oscillation (C1 = C2 = 47pF) | | 12 | 35 | μA | | |
| IDDS3 | Stop mode*3 VDD = 5.5V, termination of 16MHz and 32MHz oscillation | | — | — | — | μA | |

| Item | Symbol | Pins | Conditions | Min. | Typ. | Max. | Unit |
|-------------------|-----------------|--|---------------------------------------|------|------|------|------|
| Input capacitance | C _{IN} | PA, PB, PD, PE0 to PE3, PF4 to PF7, PG7, EXTAL, TEX, $\overline{\text{RST}}$ | Clock 1MHz 0V for no measured pins | | 10 | 20 | pF |

*1 For $\overline{\text{RST}}$ pin, specifies the input current when pull-up resistor is selected, and specifies the leakage current when non-resistor is selected.

*2 When all output pins are left open.

*3 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

| Item | Symbol | Pins | Conditions | Min. | Typ. | Max. | Unit |
|---|--------------------------------------|-----------------|--|----------------------|--------|------|------|
| System clock frequency | fc | XTAL EXTAL | Fig. 1, Fig. 2 | 8 | | 16 | MHz |
| System clock input pulse width | t _{XL} , t _{XH} | EXTAL | Fig. 1, Fig. 2 External clock drive | 28 | | | ns |
| System clock input rise and fall times | t _{CR} , t _{CF} | EXTAL | Fig. 1, Fig. 2 External clock drive | | | 200 | ns |
| Event count input clock pulse width | t _{EH} , t _{EL} | \overline{EC} | Fig. 3 | 4t _{sys} *1 | | | ns |
| Event count input clock rise and fall times | t _{ER} , t _{EF} | \overline{EC} | Fig. 3 | | | 20 | ms |
| System clock frequency | fc | TEX TX | VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied conditions) | | 32.768 | | kHz |
| Event count input clock input pulse width | t _{TL} , t _{TH} | TEX | Fig. 3 | 10 | | | μs |
| Event count input clock rise and fall times | t _{TR} , t _{TF} | TEX | Fig. 3 | | | 20 | ms |

*1 Indicates three values according to the contents of the clock control register (CLC: 00 FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

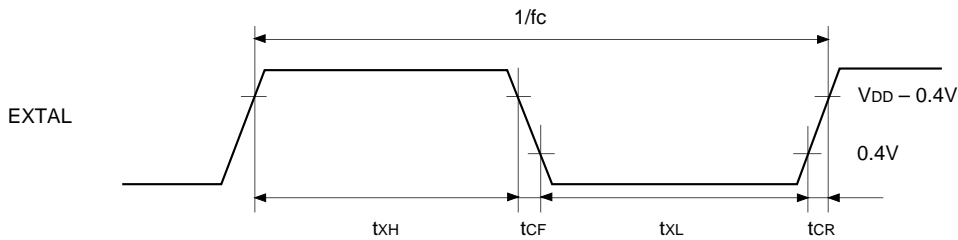


Fig. 1. Clock timing

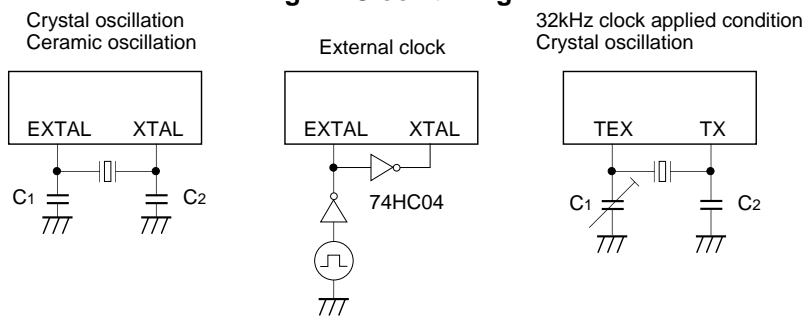


Fig.2. Clock applied conditions

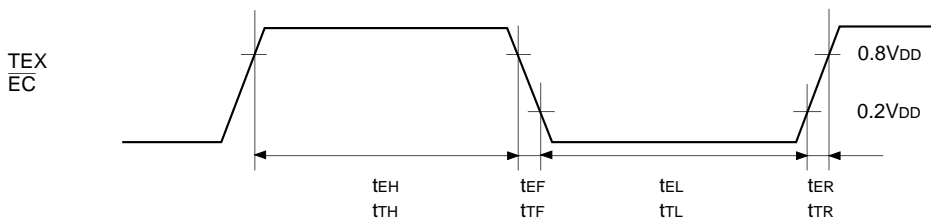


Fig. 3. Event count clock timing

(2) Serial transfer

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

| Item | Symbol | Pins | Conditions | Min. | Max. | Unit |
|---|------------------|-------------------------|-------------------------------------|-----------------|------|------|
| $\overline{\text{SCK}}$ cycle time | t_{KCY} | $\overline{\text{SCK}}$ | Input mode | 1000 | | ns |
| | | | Output mode | $8000/f_c$ | | ns |
| $\overline{\text{SCK}}$ High and Low level width | t_{KH} | $\overline{\text{SCK}}$ | $\overline{\text{SCK}}$ input mode | 400 | | ns |
| | t_{KL} | | $\overline{\text{SCK}}$ output mode | $4000/f_c - 50$ | | ns |
| SI input setup time (for $\overline{\text{SCK}} \uparrow$) | t_{SIK} | SI | $\overline{\text{SCK}}$ input mode | 100 | | ns |
| | | | $\overline{\text{SCK}}$ output mode | 200 | | ns |
| SI hold time (for $\overline{\text{SCK}} \uparrow$) | t_{KSI} | SI | $\overline{\text{SCK}}$ input mode | 200 | | ns |
| | | | $\overline{\text{SCK}}$ output mode | 100 | | ns |
| $\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time | t_{KSO} | SO | $\overline{\text{SCK}}$ input mode | | 200 | ns |
| | | | $\overline{\text{SCK}}$ output mode | | 100 | ns |

Note) The load of $\overline{\text{SCK}}$ output mode and SO output delay time is $50\text{ pF} + 1\text{TTL}$.

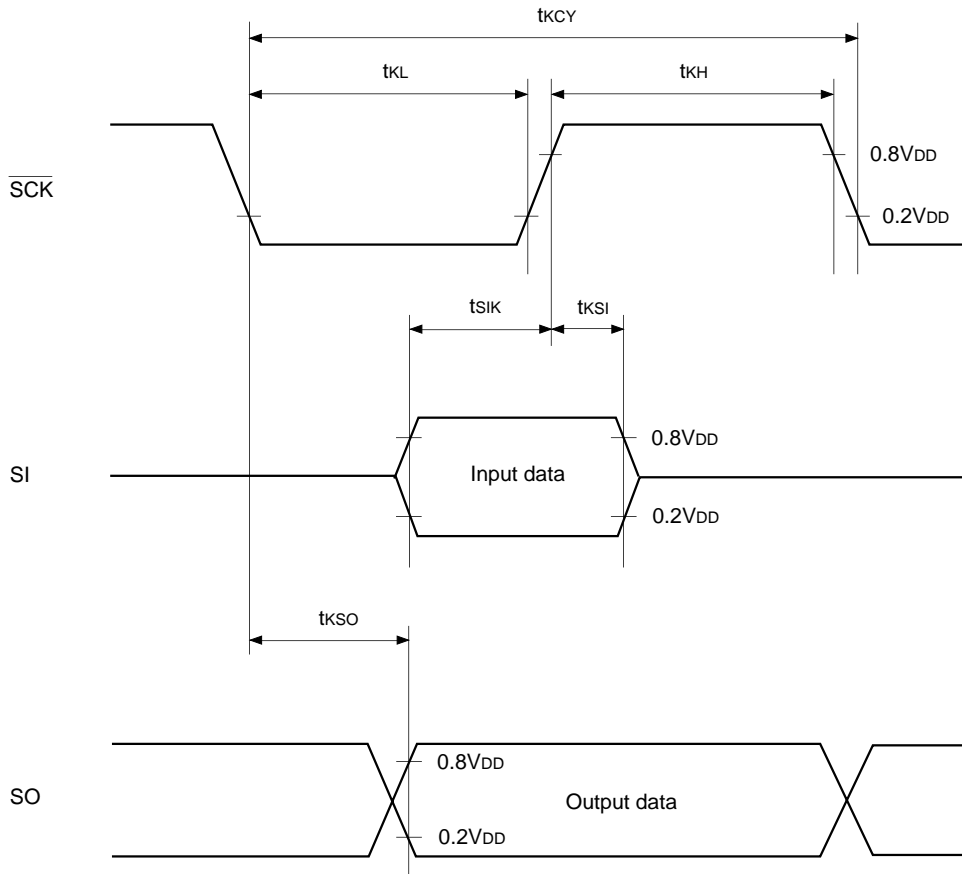
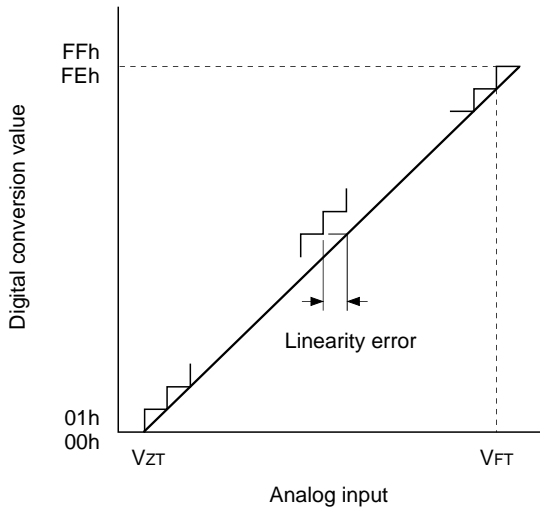


Fig. 4. Serial transfer timing

(3) A/D converter characteristics

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

| Item | Symbol | Pins | Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|---------------|------------|--|-------------------|------|----------|---------------|
| Resolution | | | | | | 8 | Bits |
| Linearity error | | | $T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = 0\text{V}$ | | | ± 3 | LSB |
| Zero transition voltage | V_{ZT}^{*1} | | | -10 | 10 | 70 | mV |
| Full-scale transition voltage | V_{FT}^{*2} | | | 4910 | 4970 | 5030 | mV |
| Conversion time | t_{CONV} | | | $26/f_{ADC}^{*3}$ | | | μs |
| Sampling time | t_{SAMP} | | | $6/f_{ADC}^{*3}$ | | | μs |
| Analog input voltage | V_{IAN} | AN0 to AN5 | | 0 | | V_{DD} | V |



*1 V_{ZT} : Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 V_{FT} : Value at which the digital conversion value changes from FEh to FFh and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F6h):

$$f_{ADC} = f_c \text{ (CKS = "0")}, f_c/2 \text{ (CKS = "1")}$$

Fig. 5. Definitions of A/D converter terms

(4) Interruption, reset input ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

| Item | Symbol | Pins | Conditions | Min. | Max. | Unit |
|---|----------------------|--|------------|----------|------|---------------|
| External interruption High, Low level width | t_{IH} t_{IL} | $\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ | | 1 | | μs |
| Reset input Low level width | t_{RSL} | $\overline{\text{RST}}$ | | $32/f_c$ | | μs |

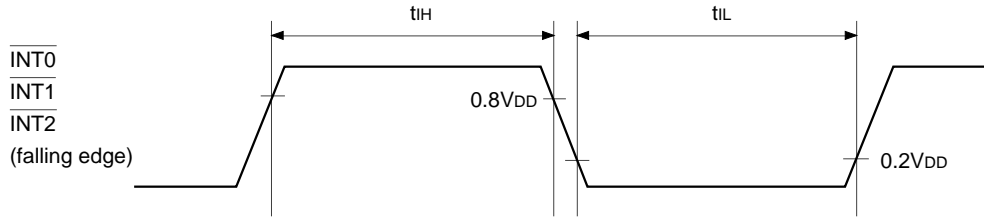


Fig. 6. Interruption input timing

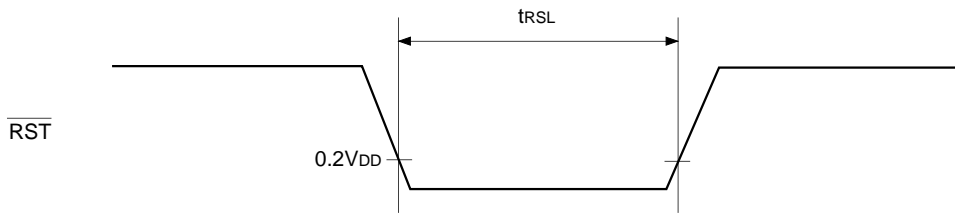


Fig. 7. $\overline{\text{RST}}$ input timing

(5) I²C bus timing

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

| Item | Symbol | Pins | Conditions | Min. | Max. | Unit |
|--|----------------------|----------|------------|------|------|------|
| SCL clock frequency | f _{SCL} | SCL | | 0 | 100 | kHz |
| Bus-free time before starting transfer | t _{BUF} | SDA, SCL | | 4.7 | | μs |
| Hold time for starting transfer | t _{HD; STA} | SDA, SCL | | 4.0 | | μs |
| Clock Low level width | t _{LOW} | SCL | | 4.7 | | μs |
| Clock High level width | t _{HIGH} | SCL | | 4.0 | | μs |
| Setup time for repeated transfers | t _{SU; STA} | SDA, SCL | | 4.7 | | μs |
| Data hold time | t _{HD; DAT} | SDA, SCL | | 0*1 | | μs |
| Data setup time | t _{SU; DAT} | SDA, SCL | | 250 | | ns |
| SDA, SCL rise time | t _R | SDA, SCL | | | 1 | μs |
| SDA, SCL fall time | t _F | SDA, SCL | | | 300 | ns |
| Setup time for transfer completion | t _{SU; STO} | SDA, SCL | | 4.7 | | μs |

*1 The data hold time should be 300ns or more because the SCL rise time (300ns Max.) is not included in it.

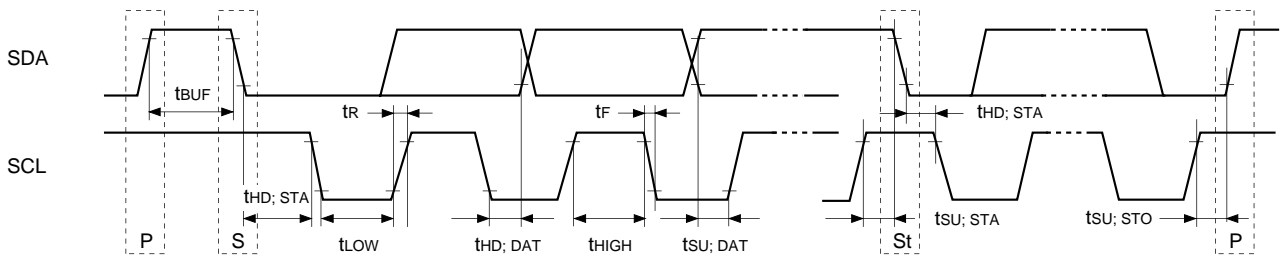


Fig. 8. I²C bus transfer timing

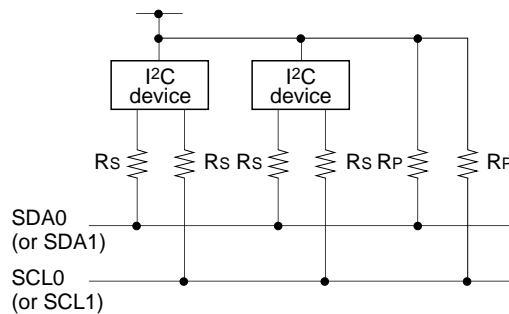


Fig. 9. I²C device recommended circuit

- A pull-up resistor (Rp) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce the spike noise caused by CRT flashover.

Appendix

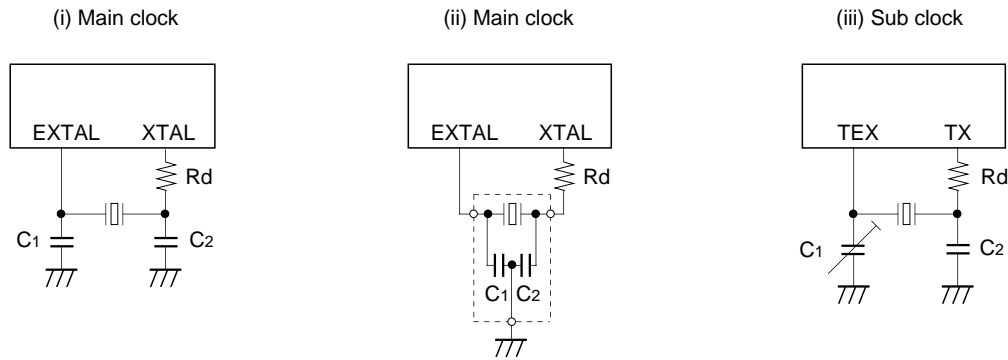


Fig. 10. Recommended oscillation circuit

| Manufacture | Model | fc (MHz) | C1 (pF) | C2 (pF) | Rd (Ω) | Circuit example |
|--------------------------|-----------------|-----------|---------|---------|-------------------|-----------------|
| MURATA MFG CO., LTD. | CSA10.0MTZ | 10.0 | 30 | 30 | 0* ¹ | (i) |
| | CSA12.0MTZ | 12.0 | | | | |
| | CSA16.00MXZ040 | 16.0 | 5 | 5 | | |
| | CST10.0MTW* | 10.0 | 30 | 30 | | (ii) |
| | CST12.0MTW* | 12.0 | | | | |
| | CST16.00MXW0C1* | 16.0 | | | | |
| RIVER ELETEC CORPORATION | HC-49/U03 | 8.0 | 18 | 18 | 330* ¹ | (i) |
| | | 12.0 | 12 | 12 | | |
| | | 16.0 | 10 | 10 | | |
| KINSEKI LTD. | HC-49/U (-S) | 8.0 | 10 | 10 | 0* ¹ | |
| | | 12.0 | 5 | 5 | | |
| | | 16.0 | Open | Open | | |
| | P3 | 32.768kHz | 30 | 33 | 120k | (iii) |

*Models with an asterisk have the built-in ground capacitance (C1, C2).

*¹ The series resistor for XTAL can reduce the effect of the noise caused by the electrostatic discharge.

Mask Option Table

| Item | Content | |
|----------------------------|--------------|----------|
| Reset pin pull-up resistor | Non-existent | Existent |

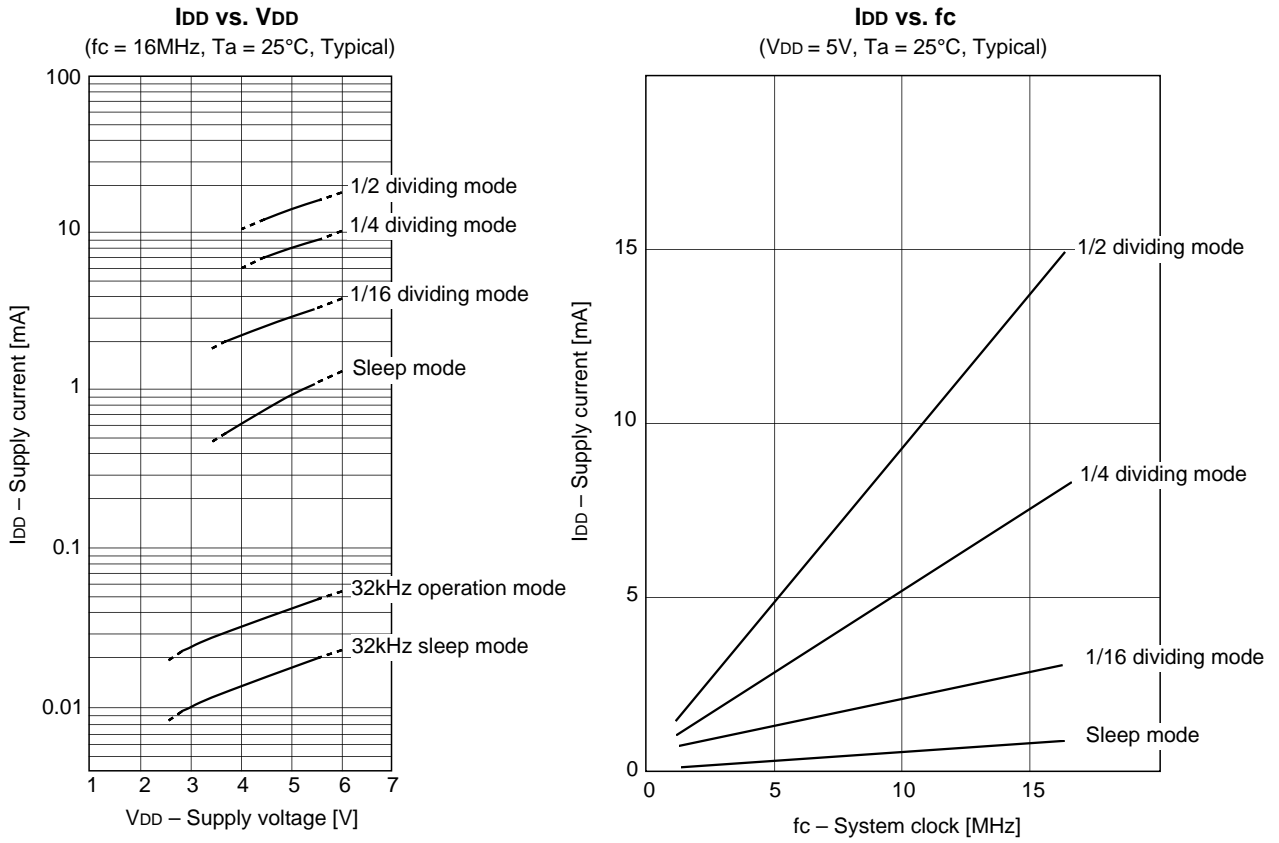
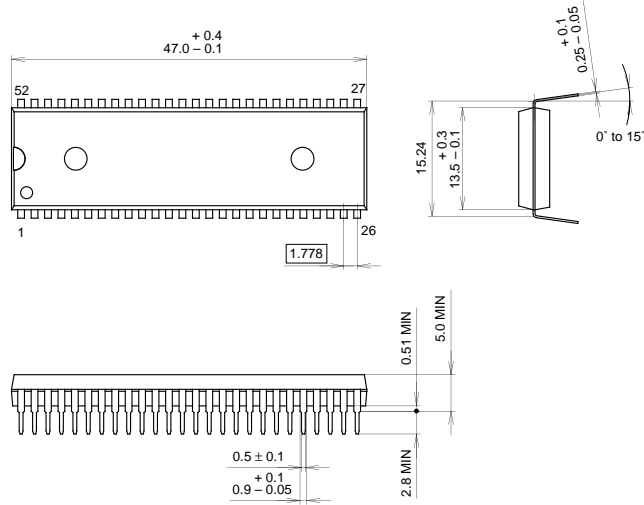


Fig. 11. Characteristic curves

Package Outline

Unit: mm

52PIN SDIP (PLASTIC)

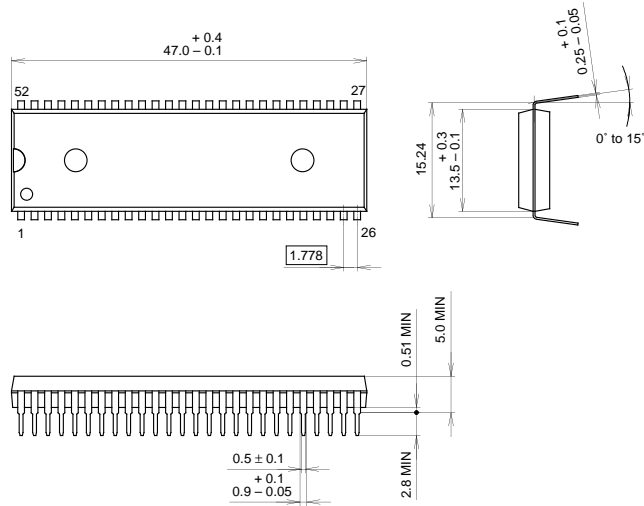


PACKAGE STRUCTURE

| | |
|------------|--------------------------|
| SONY CODE | SDIP-52P-01 |
| EIAJ CODE | P-SDIP52-13.5x47.0-1.778 |
| JEDEC CODE | _____ |

| | |
|------------------|----------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | COPPER ALLOY |
| PACKAGE MASS | 5.6g |

52PIN SDIP (PLASTIC)



PACKAGE STRUCTURE

| | |
|------------|--------------------------|
| SONY CODE | SDIP-52P-01 |
| EIAJ CODE | P-SDIP52-13.5x47.0-1.778 |
| JEDEC CODE | _____ |

| | |
|------------------|----------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | COPPER ALLOY |
| PACKAGE MASS | 5.6g |

LEAD PLATING SPECIFICATIONS

| ITEM | SPEC. |
|--------------------|-----------------|
| LEAD MATERIAL | COPPER ALLOY |
| SOLDER COMPOSITION | Sn-Bi Bi:1-4wt% |
| PLATING THICKNESS | 5-18µm |