

## GP4501

### N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

N-CH BV <sub>DSS</sub>	30V
R <sub>DS(ON)</sub>	28mΩ
I <sub>D</sub>	7A
P-CH BV <sub>DSS</sub>	-30V
R <sub>DS(ON)</sub>	50mΩ
I <sub>D</sub>	-5.3A

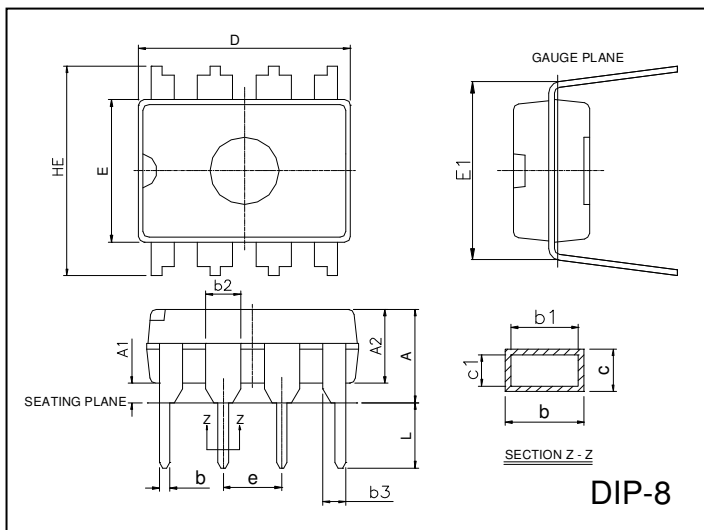
### Description

The GP4501 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

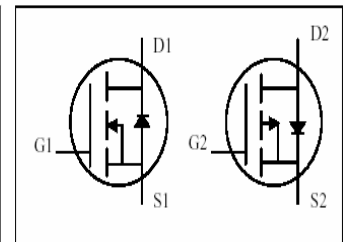
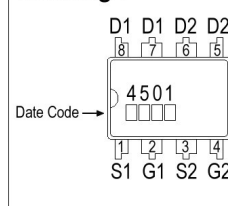
### Features

- \*Simple Drive Requirement
- \*Lower On-resistance
- \*Fast Switching

### Package Dimensions



### Marking :



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	-	0.5334	c1	0.203	0.279
A1	0.381	-	D	9.017	10.16
A2	2.921	4.953	E	6.096	7.112
b	0.356	0.559	E1	7.620	8.255
b1	0.356	0.508	e	2.540 BSC	
b2	1.143	1.778	HE	-	10.92
b3	0.762	1.143	L	2.921	3.810
c	0.203	0.356			

### Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		N-channel	P-channel	
Drain-Source Voltage	V <sub>DS</sub>	30	-30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	±16	V
Continuous Drain Current <sup>3</sup>	I <sub>D</sub> @TA=25°C	7	-5.3	A
Continuous Drain Current <sup>3</sup>	I <sub>D</sub> @TA=70°C	5.8	-4.7	A
Pulsed Drain Current <sup>1</sup>	I <sub>DM</sub>	20	-20	A
Total Power Dissipation	P <sub>D</sub> @TA=25°C	2.0		W
Linear Derating Factor		0.016		W/°C
Operating Junction and Storage Temperature Range	T <sub>j</sub> , T <sub>stg</sub>	-55 ~ +150		°C

### Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-ambient <sup>3</sup> Max.	R <sub>thj-a</sub>	62.5	°C/W

**N-Channel Electrical Characteristics (T<sub>j</sub> = 25°C unless otherwise specified)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	30	-	-	V	V <sub>GS</sub> =0, I <sub>D</sub> =250uA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_j$	-	0.02	-	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
Gate Threshold Voltage	V <sub>GS(th)</sub>	1.0	-	3.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA
Forward Transconductance	g <sub>fs</sub>	-	13	-	S	V <sub>DS</sub> =10V, I <sub>D</sub> =7A
Gate-Source Leakage Current	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> = ±20V
Drain-Source Leakage Current(T <sub>j</sub> =25°C)	I <sub>DSS</sub>	-	-	1	uA	V <sub>DS</sub> =30V, V <sub>GS</sub> =0
Drain-Source Leakage Current(T <sub>j</sub> =70°C)		-	-	25	uA	V <sub>DS</sub> =24V, V <sub>GS</sub> =0
Static Drain-Source On-Resistance <sup>2</sup>	R <sub>DS(ON)</sub>	-	-	28	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> =7A
		-	-	42		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A
Total Gate Charge <sup>2</sup>	Q <sub>g</sub>	-	8.4	-	nC	I <sub>D</sub> =7A V <sub>DS</sub> =24V V <sub>GS</sub> =4.5V
Gate-Source Charge	Q <sub>gs</sub>	-	2.1	-		
Gate-Drain ("Miller") Charge	Q <sub>gd</sub>	-	4.7	-		
Turn-on Delay Time <sup>2</sup>	T <sub>d(on)</sub>	-	6	-	ns	V <sub>DS</sub> =15V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>G</sub> =3.3Ω R <sub>D</sub> =15Ω
Rise Time	T <sub>r</sub>	-	5.2	-		
Turn-off Delay Time	T <sub>d(off)</sub>	-	18.8	-		
Fall Time	T <sub>f</sub>	-	4.4	-		
Input Capacitance	C <sub>iss</sub>	-	645	-	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =25V f=1.0MHz
Output Capacitance	C <sub>oss</sub>	-	150	-		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	95	-		

**Source-Drain Diode**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage <sup>2</sup>	V <sub>SD</sub>	-	-	1.2	V	I <sub>S</sub> =7A, V <sub>GS</sub> =0V, T <sub>j</sub> =25°C
Continuous Source Current (Body Diode)	I <sub>S</sub>	-	-	1.67	A	V <sub>D</sub> =V <sub>G</sub> =0V, V <sub>S</sub> =1.2V

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width ≤ 300us, duty cycle ≤ 2%.

3. Mounted on 1 in<sup>2</sup> copper pad of FR4 board; 90°C/W when mounted on Min. copper pad.

**P-Channel Electrical Characteristics (T<sub>j</sub> = 25°C unless otherwise specified)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-30	-	-	V	V <sub>GS</sub> =0, I <sub>D</sub> =-250uA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_j$	-	-0.028	-	V/°C	Reference to 25°C, I <sub>D</sub> =-1mA
Gate Threshold Voltage	V <sub>GS(th)</sub>	-1.0	-	-3.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA
Forward Transconductance	g <sub>fs</sub>	-	8.5	-	S	V <sub>DS</sub> =-10V, I <sub>D</sub> =-5.3A
Gate-Source Leakage Current	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> = ±16V
Drain-Source Leakage Current(T <sub>j</sub> =25°C)	I <sub>DSS</sub>	-	-	-1	uA	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0
Drain-Source Leakage Current(T <sub>j</sub> =70°C)		-	-	-25	uA	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0
Static Drain-Source On-Resistance <sup>2</sup>	R <sub>DS(ON)</sub>	-	-	50	mΩ	V <sub>GS</sub> =-10V, I <sub>D</sub> =-5.3A
		-	-	90		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4.2A
Total Gate Charge <sup>2</sup>	Q <sub>g</sub>	-	20	-	nC	I <sub>D</sub> =-5.3A V <sub>DS</sub> =-15V V <sub>GS</sub> =-10V
Gate-Source Charge	Q <sub>gs</sub>	-	3.5	-		
Gate-Drain ("Miller") Charge	Q <sub>gd</sub>	-	2	-		
Turn-on Delay Time <sup>2</sup>	T <sub>d(on)</sub>	-	12	-	ns	V <sub>DS</sub> =-15V I <sub>D</sub> =-1A V <sub>GS</sub> =-10V R <sub>G</sub> =6Ω R <sub>D</sub> =15Ω
Rise Time	T <sub>r</sub>	-	20	-		
Turn-off Delay Time	T <sub>d(off)</sub>	-	45	-		
Fall Time	T <sub>f</sub>	-	27	-		
Input Capacitance	C <sub>iss</sub>	-	790	-	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =-15V f=1.0MHz
Output Capacitance	C <sub>oss</sub>	-	440	-		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	120	-		

**Source-Drain Diode**

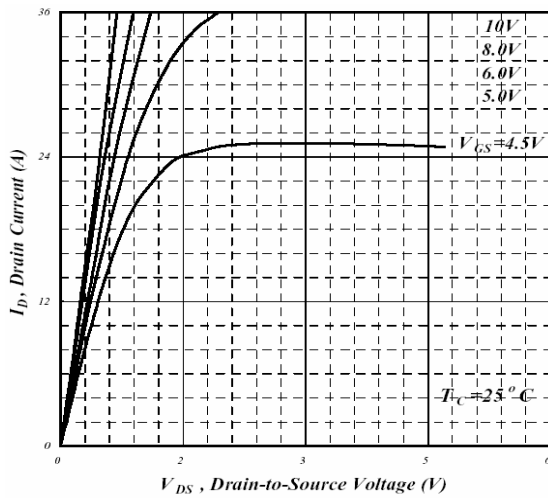
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage <sup>2</sup>	V <sub>SD</sub>	-	-	-1.2	V	I <sub>S</sub> =-2.6A, V <sub>GS</sub> =0V, T <sub>j</sub> =25°C
Continuous Source Current (Body Diode)	I <sub>S</sub>	-	-	-1.67	A	V <sub>D</sub> =V <sub>G</sub> =0V, V <sub>S</sub> =-1.2V

Notes: 1. Pulse width limited by Max. junction temperature.

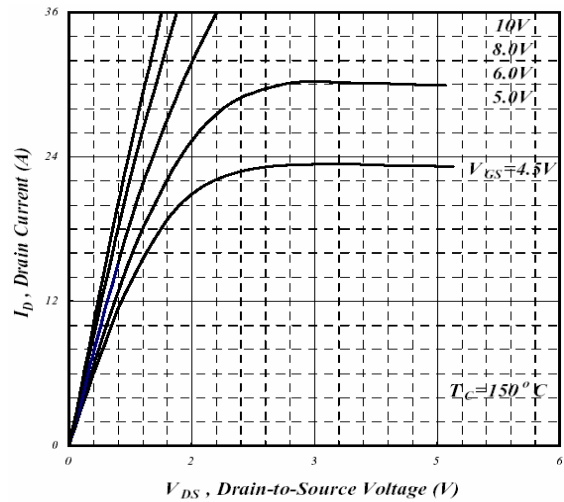
2. Pulse width ≤ 300us, duty cycle ≤ 2%.

3. Mounted on 1 in<sup>2</sup> copper pad of FR4 board; 90°C/W when mounted on Min. copper pad.

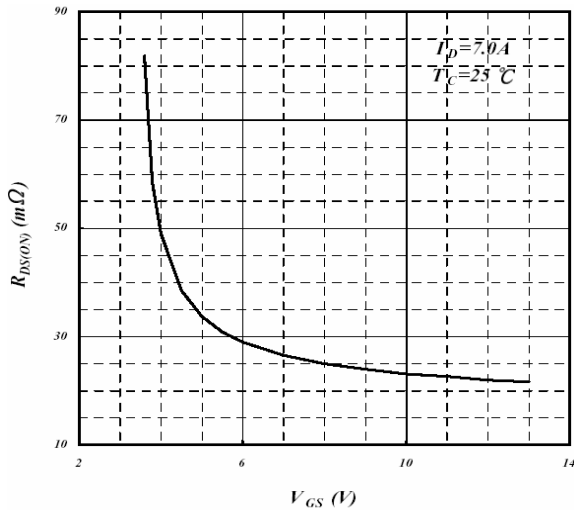
## Characteristics Curve N-Channel



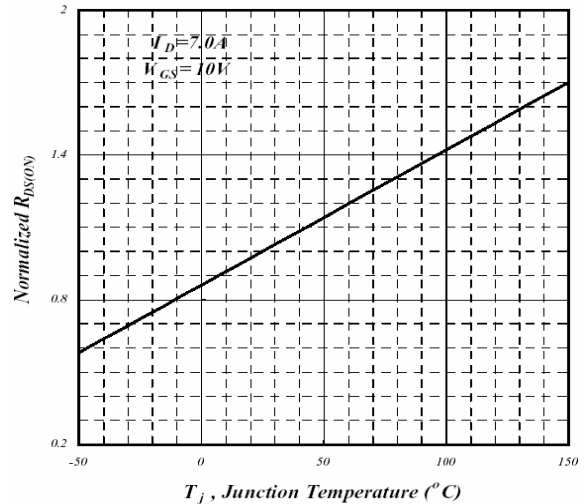
**Fig 1. Typical Output Characteristics**



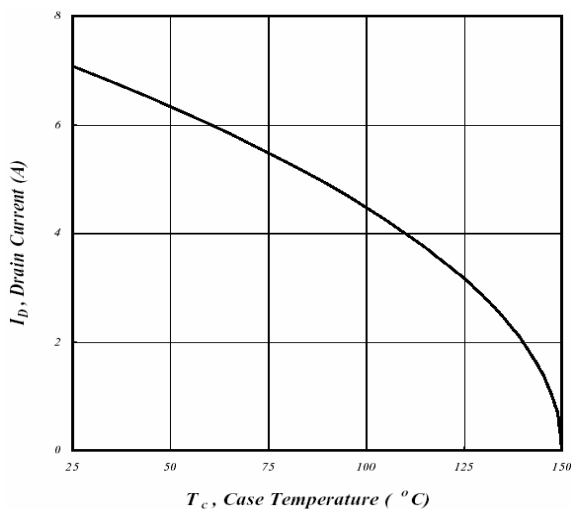
**Fig 2. Typical Output Characteristics**



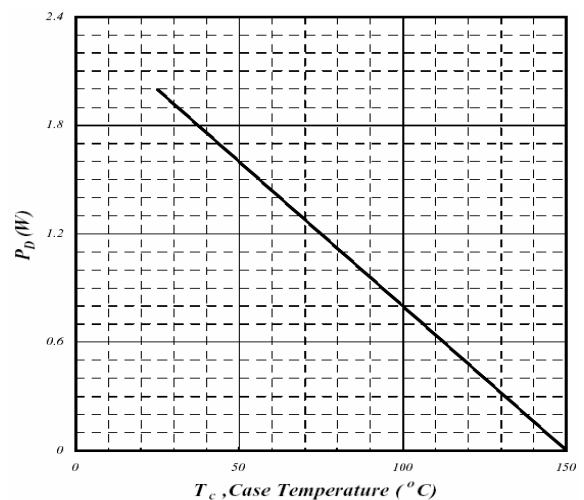
**Fig 3. On-Resistance v.s. Gate Voltage**



**Fig 4. Normalized On-Resistance v.s. Junction Temperature**

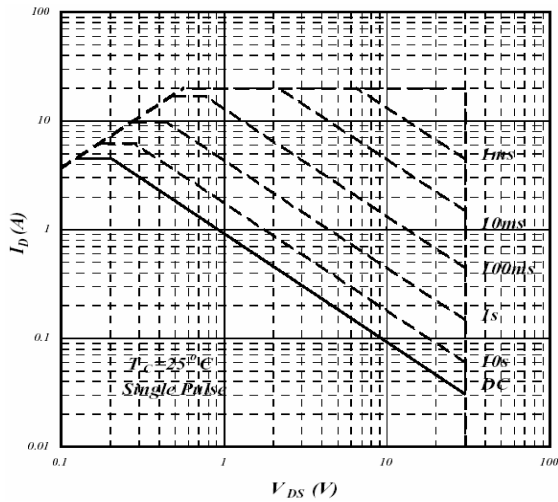


**Fig 5. Maximum Drain Current v.s. Case Temperature**

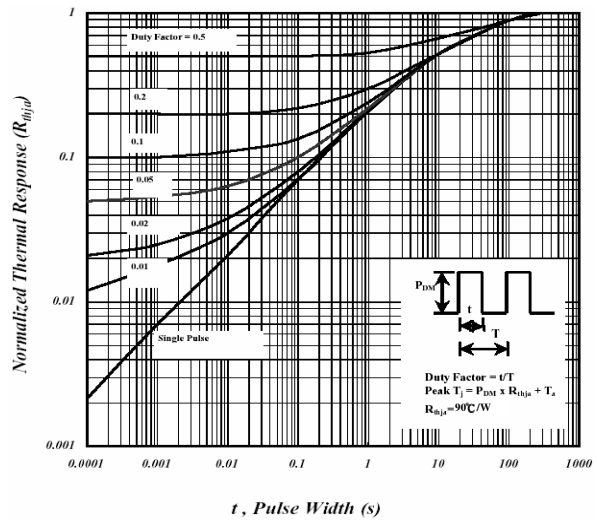


**Fig 6. Type Power Dissipation**

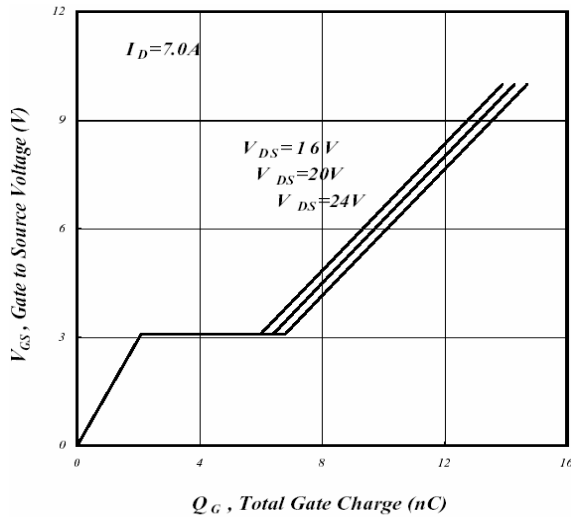
## N-Channel



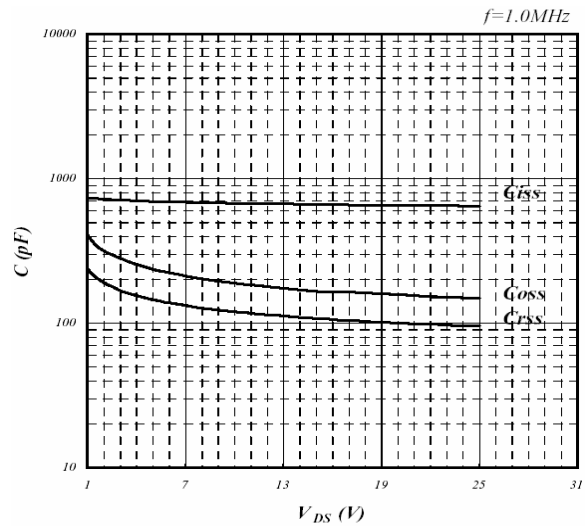
**Fig 7. Maximum Safe Operating Area**



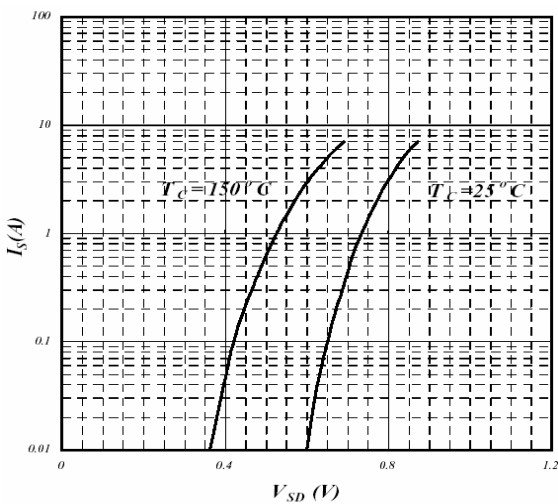
**Fig 8. Effective Transient Thermal Impedance**



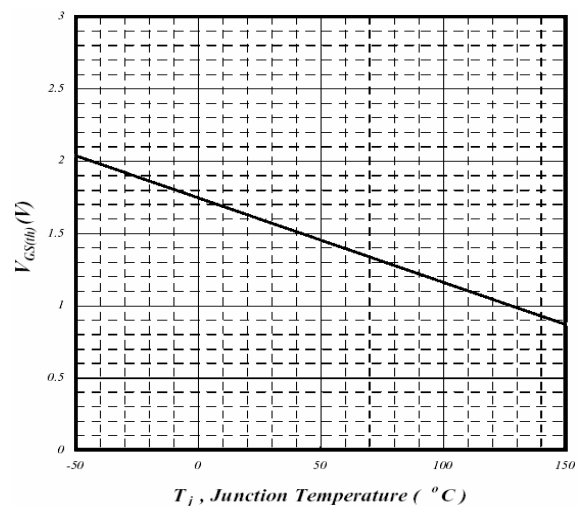
**Fig 9. Gate Charge Characteristics**



**Fig 10. Typical Capacitance Characteristics**

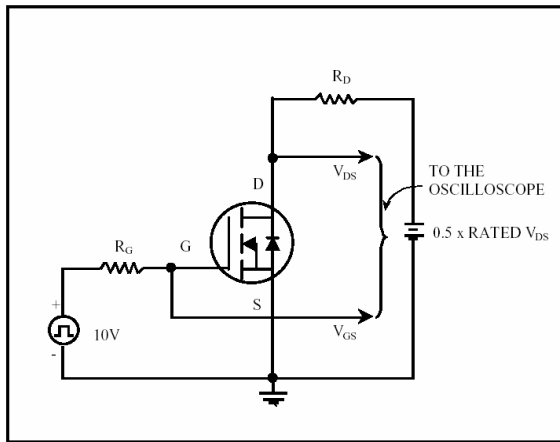


**Fig 11. Forward Characteristics of Reverse Diode**

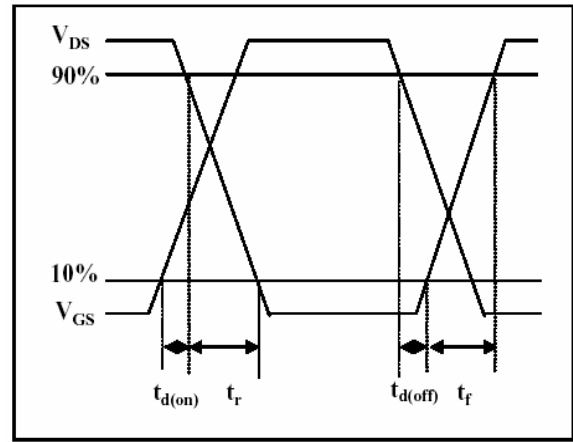


**Fig 12. Gate Threshold Voltage v.s. Junction Temperature**

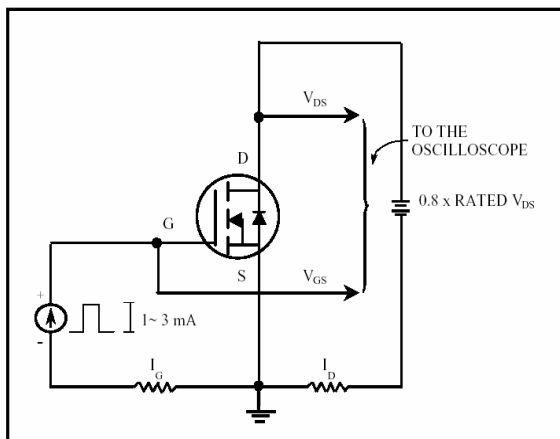
## N-Channel



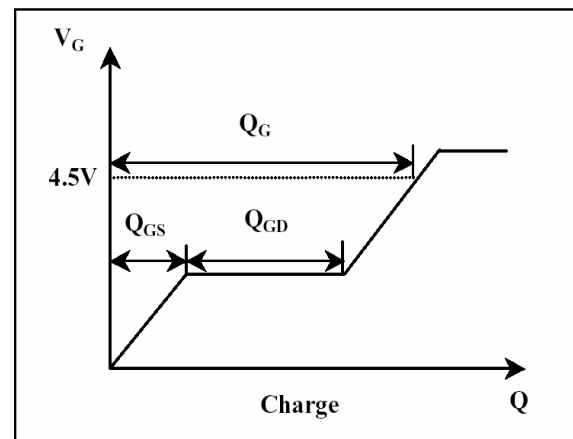
**Fig 13. Switching Time Circuit**



**Fig 14. Switching Time Waveform**

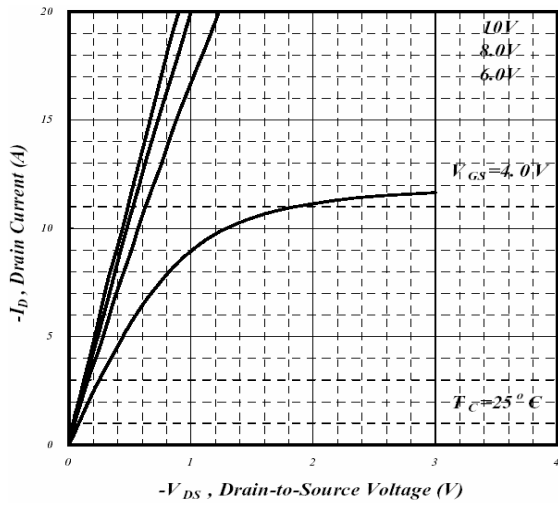


**Fig 15. Gate Charge Circuit**

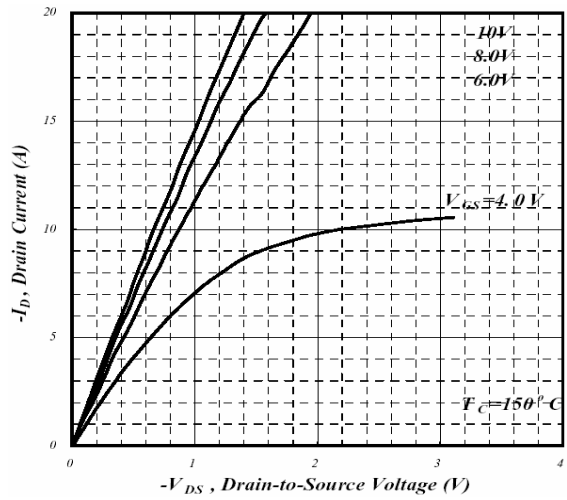


**Fig 16. Gate Charge Waveform**

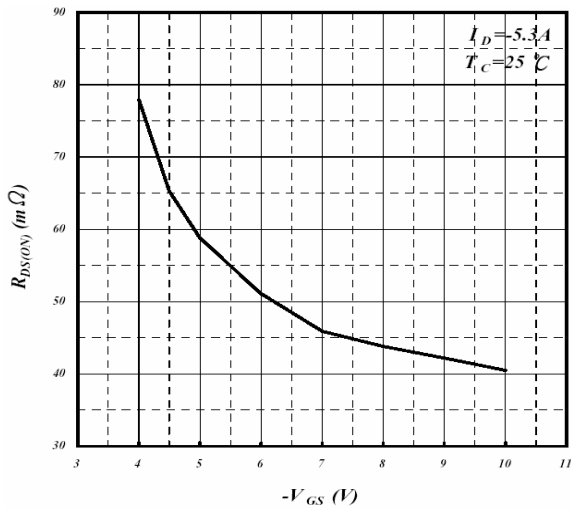
## P-Channel



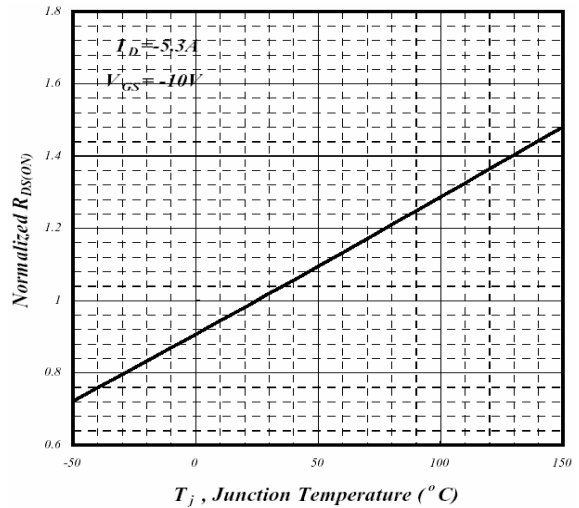
**Fig 1. Typical Output Characteristics**



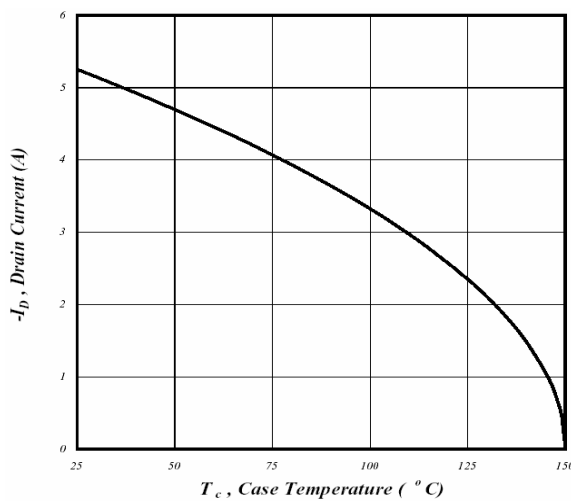
**Fig 2. Typical Output Characteristics**



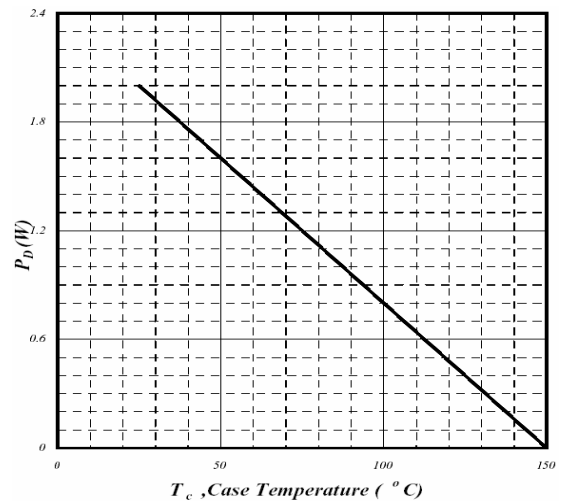
**Fig 3. On-Resistance v.s. Gate Voltage**



**Fig 4. Normalized On-Resistance v.s. Junction Temperature**

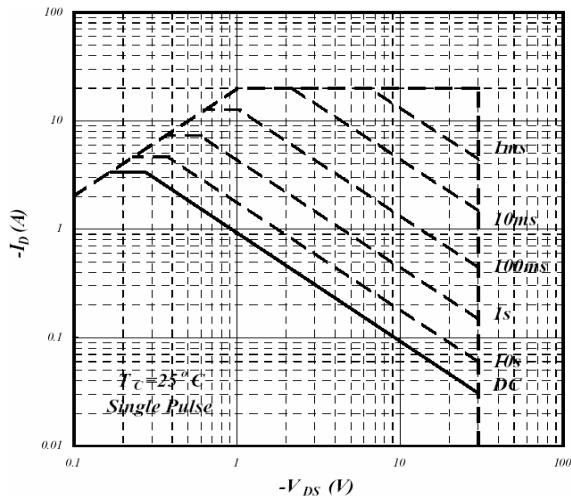


**Fig 5. Maximum Drain Current v.s. Case Temperature**

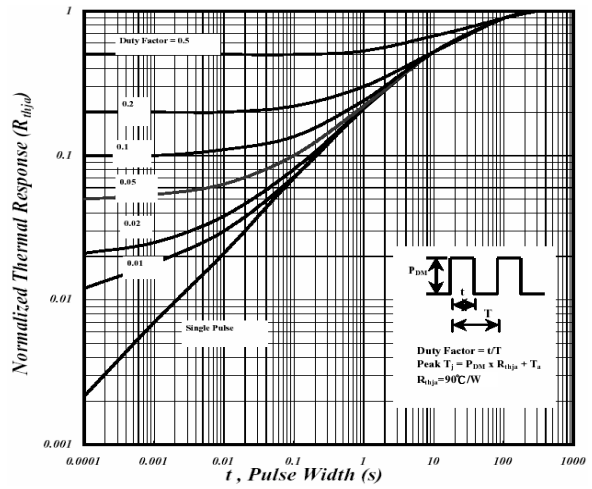


**Fig 6. Type Power Dissipation**

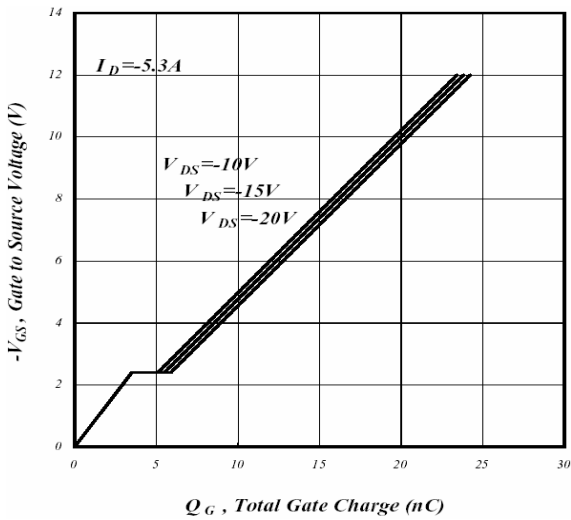
## P-Channel



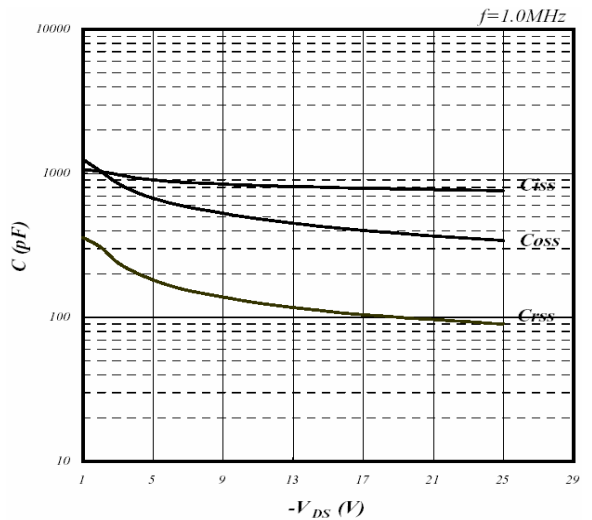
**Fig 7. Maximum Safe Operating Area**



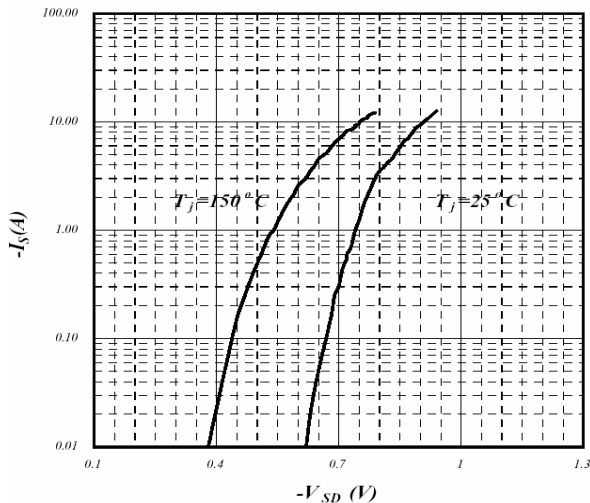
**Fig 8. Effective Transient Thermal Impedance**



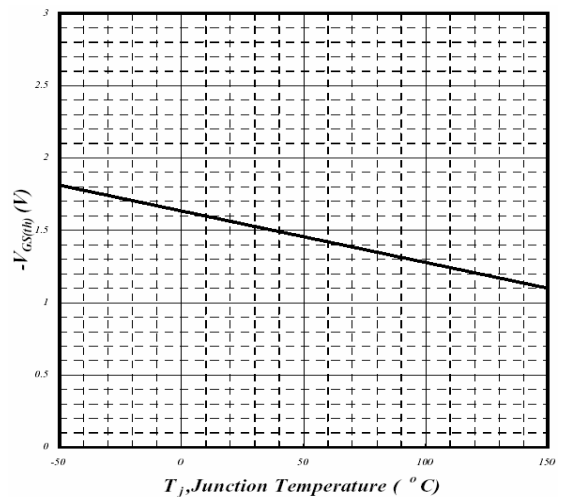
**Fig 9. Gate Charge Characteristics**



**Fig 10. Typical Capacitance Characteristics**



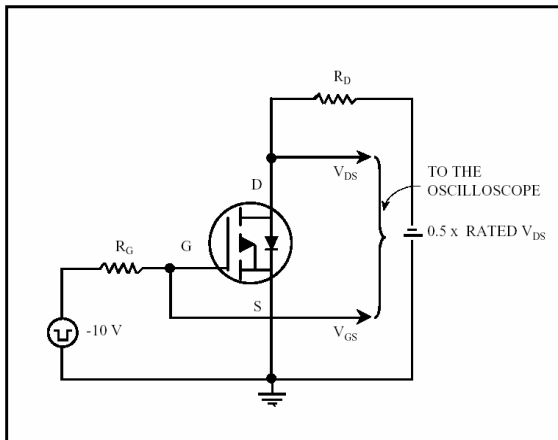
**Fig 11. Forward Characteristics of Reverse Diode**



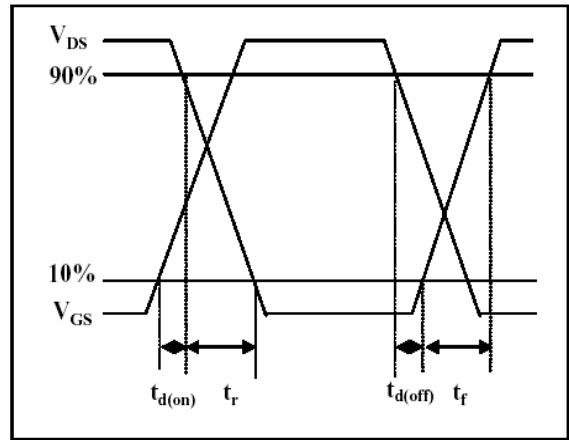
**Fig 12. Gate Threshold Voltage v.s. Junction Temperature**



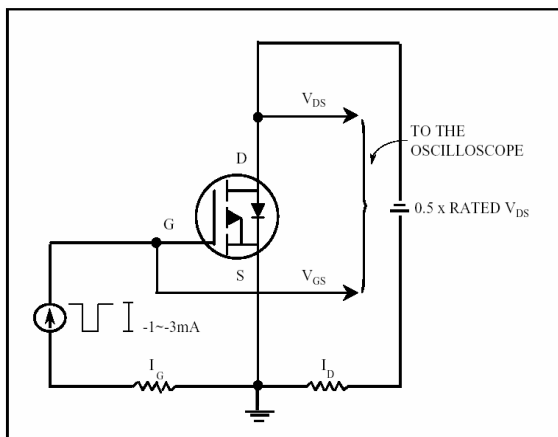
## P-Channel



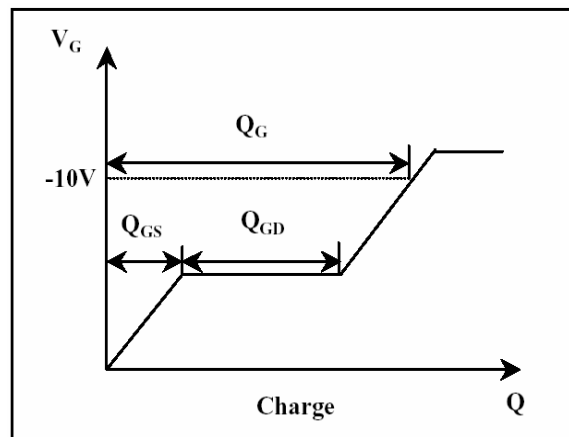
**Fig 13. Switching Time Circuit**



**Fig 14. Switching Time Waveform**



**Fig 15. Gate Charge Circuit**



**Fig 16. Gate Charge Waveform**

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