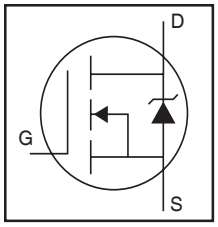
IRFR/U4615PbF

HEXFET® Power MOSFET

Applications

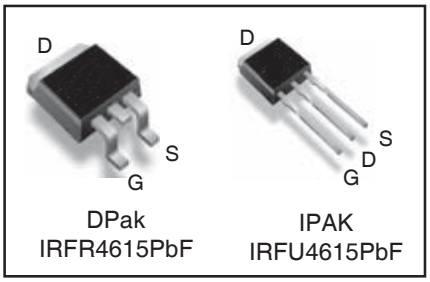
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}		150V
$R_{DS(on)}$	typ.	34mΩ
	max.	42mΩ
I_D		33A

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



DPak
IRFR4615PbF

IPAK
IRFU4615PbF

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	33	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	24	
I_{DM}	Pulsed Drain Current ①	140	
P_D @T_C = 25°C	Maximum Power Dissipation	144	W
	Linear Derating Factor	0.96	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	38	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	109	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ①		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	1.045	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑦	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

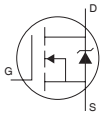
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.19	—	V/°C	Reference to 25°C, I_D = 5mA①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	34	42	mΩ	V_{GS} = 10V, I_D = 21A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = V_{GS}, I_D = 100μA
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V_{DS} = 150V, V_{GS} = 0V
		—	—	250		V_{DS} = 150V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
$R_{G(int)}$	Internal Gate Resistance	—	2.7	—	Ω	

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	35	—	—	S	V_{DS} = 50V, I_D = 21A
Q_g	Total Gate Charge	—	26		nC	I_D = 21A
Q_{gs}	Gate-to-Source Charge	—	8.6	—		V_{DS} = 75V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	9.0	—		V_{GS} = 10V ④
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	—	17	—		I_D = 21A, V_{DS} =0V, V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	V_{DD} = 98V
t_r	Rise Time	—	35	—		I_D = 21A
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		R_G = 7.3Ω
t_f	Fall Time	—	20	—		V_{GS} = 10V ④
C_{iss}	Input Capacitance	—	1750	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	155	—		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	—	40	—		f = 1.0MHz (See Fig.5)
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)⑥	—	179	—		V_{GS} = 0V, V_{DS} = 0V to 120V ⑥(See Fig.11)
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)⑤	—	382	—		V_{GS} = 0V, V_{DS} = 0V to 120V ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	33	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	140		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 21A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	70	—	ns	T_J = 25°C V_R = 100V,
		—	83	—		T_J = 125°C I_F = 21A
Q_{rr}	Reverse Recovery Charge	—	177	—	nC	T_J = 25°C di/dt = 100A/μs ④
		—	247	—		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	4.9	—	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

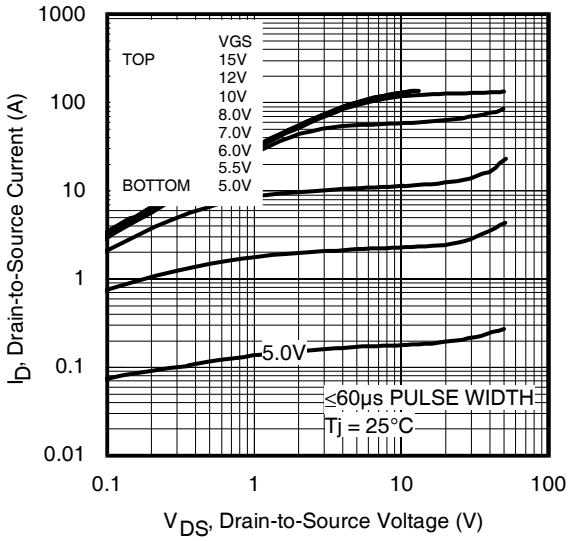


Fig 1. Typical Output Characteristics

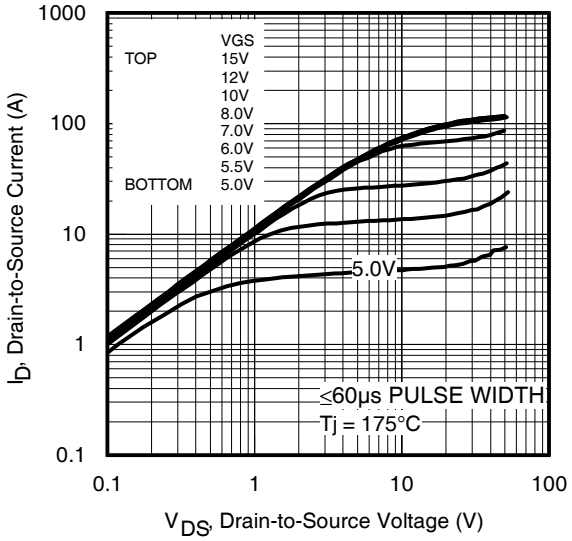


Fig 2. Typical Output Characteristics

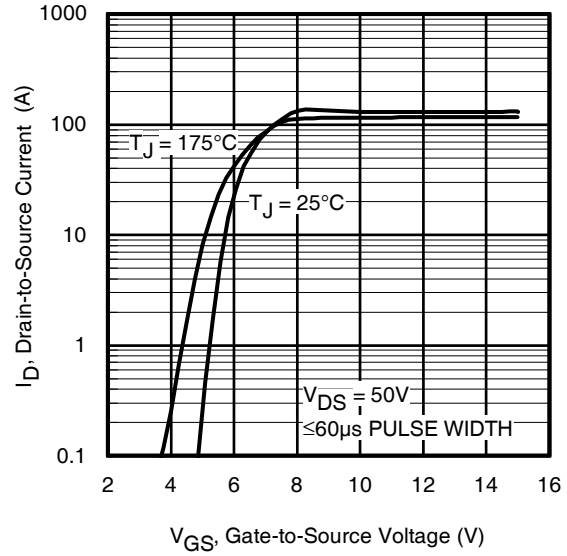


Fig 3. Typical Transfer Characteristics

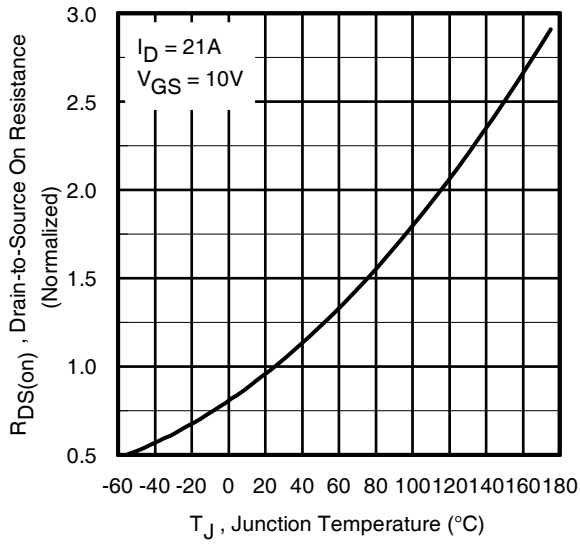


Fig 4. Normalized On-Resistance vs. Temperature

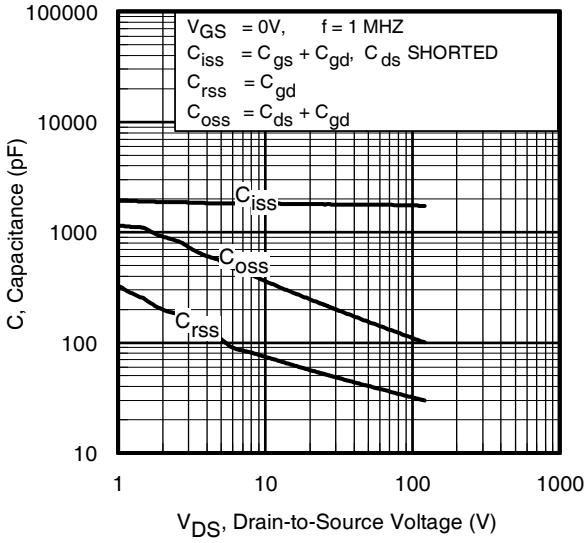


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

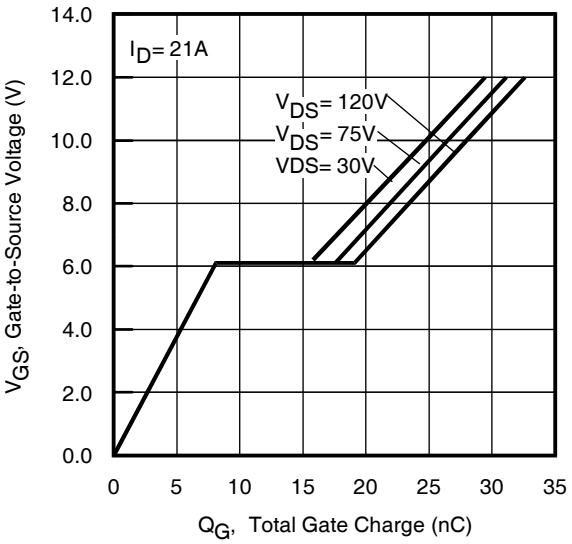


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

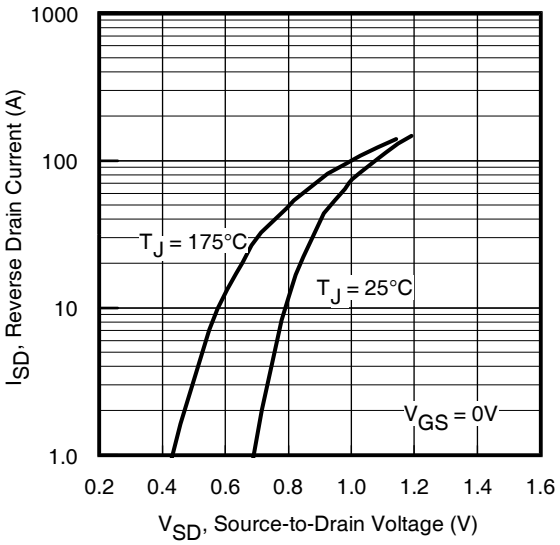


Fig 7. Typical Source-Drain Diode Forward Voltage

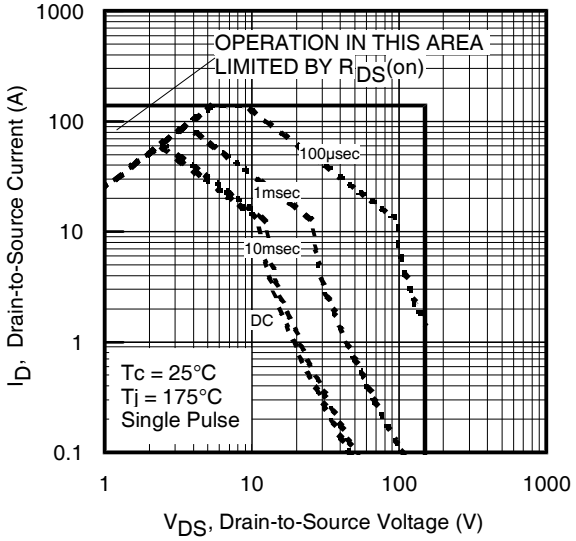


Fig 8. Maximum Safe Operating Area

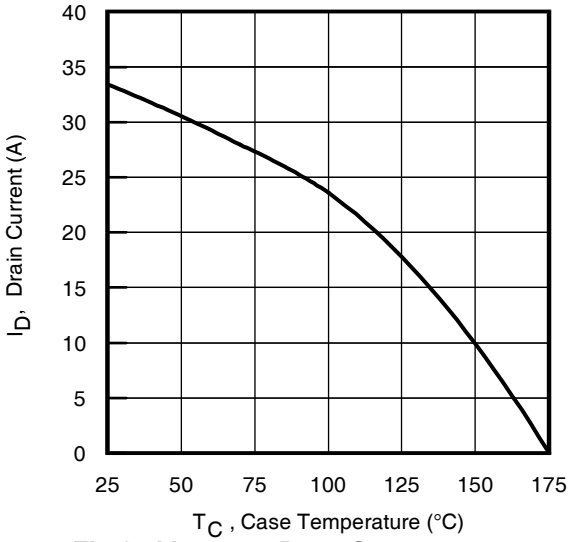


Fig 9. Maximum Drain Current vs. Case Temperature

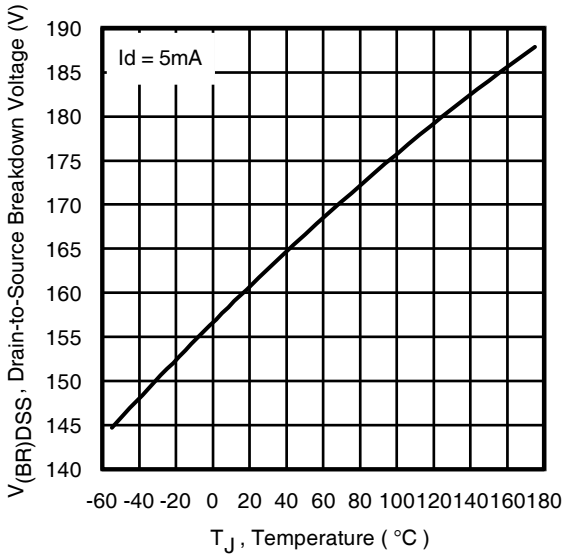


Fig 10. Drain-to-Source Breakdown Voltage

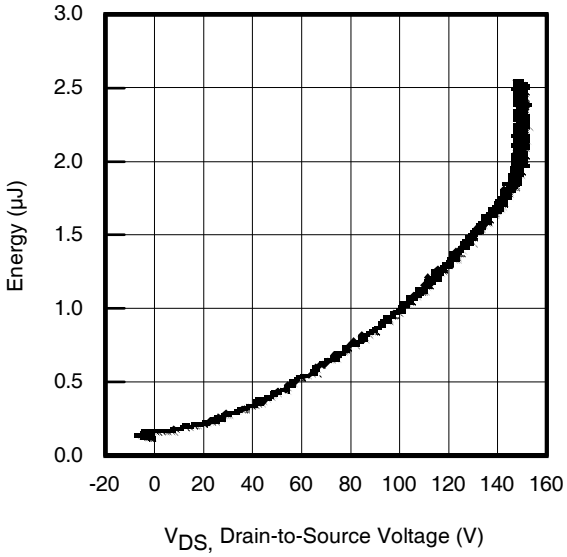


Fig 11. Typical C_{OSS} Stored Energy

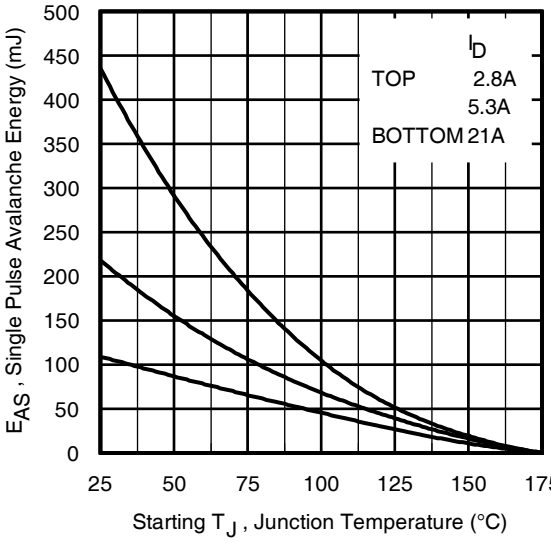


Fig 12. Maximum Avalanche Energy vs. DrainCurrent

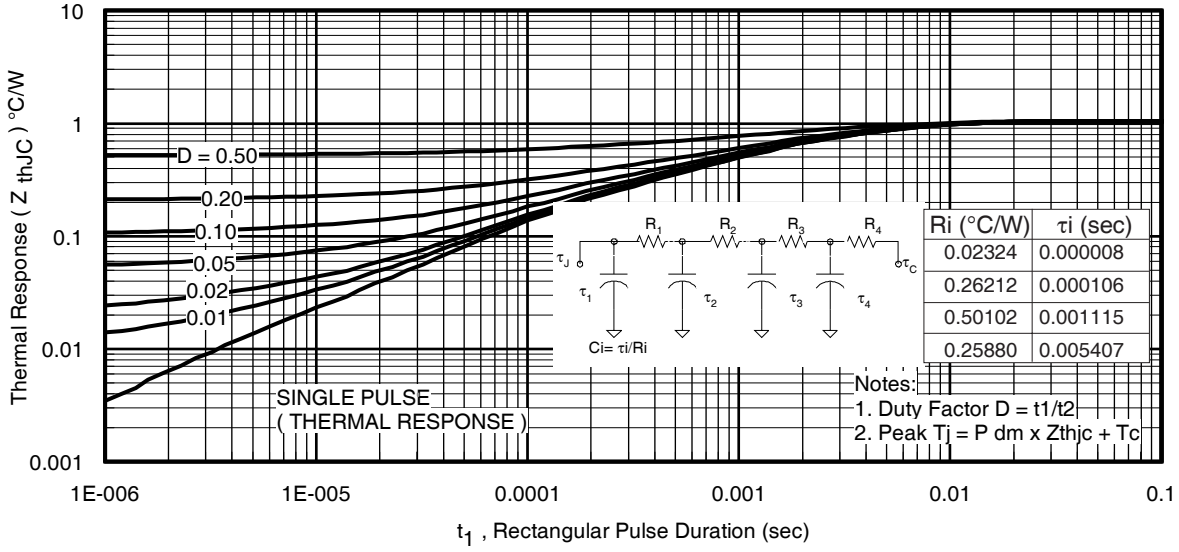


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

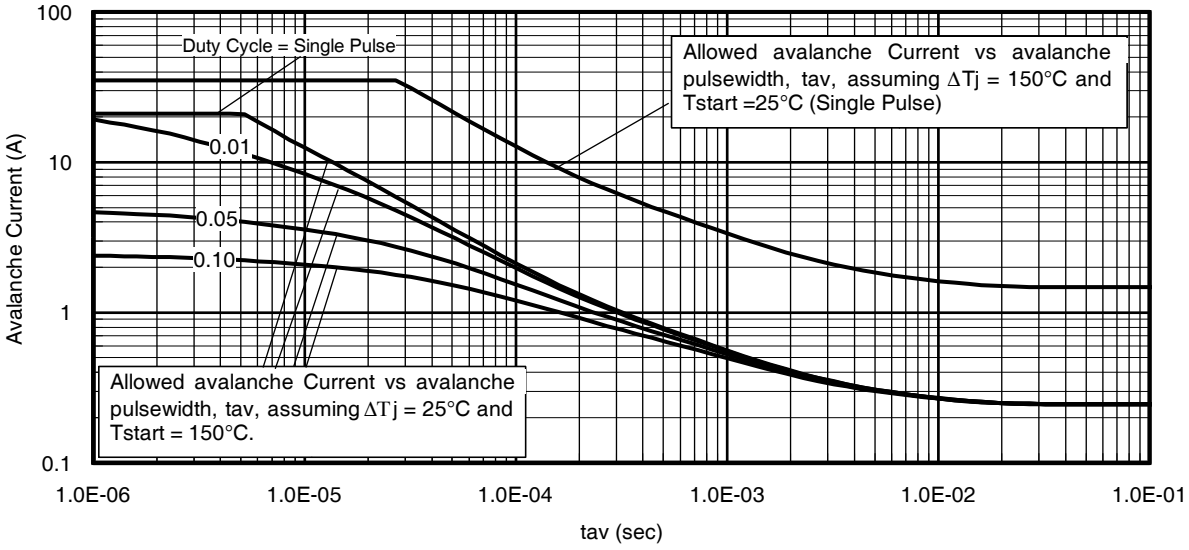


Fig 14. Typical Avalanche Current vs.Pulsewidth

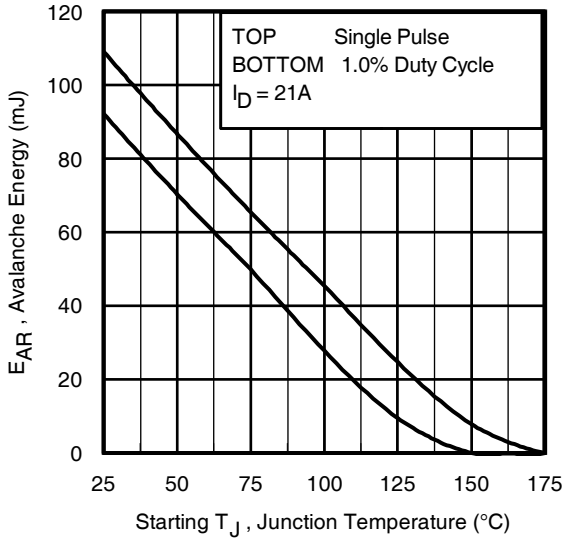


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

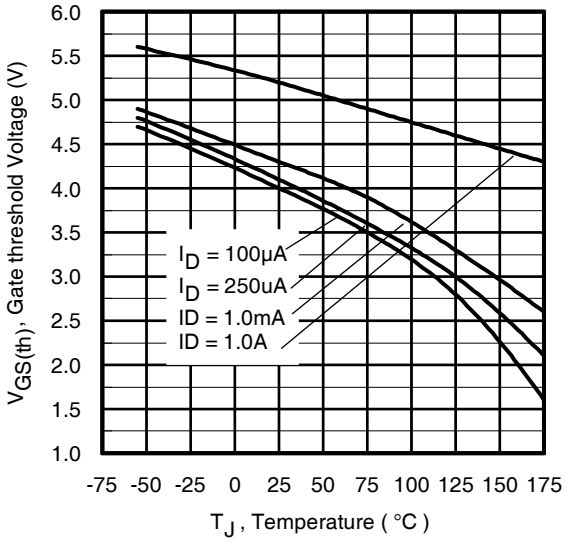


Fig 16. Threshold Voltage vs. Temperature

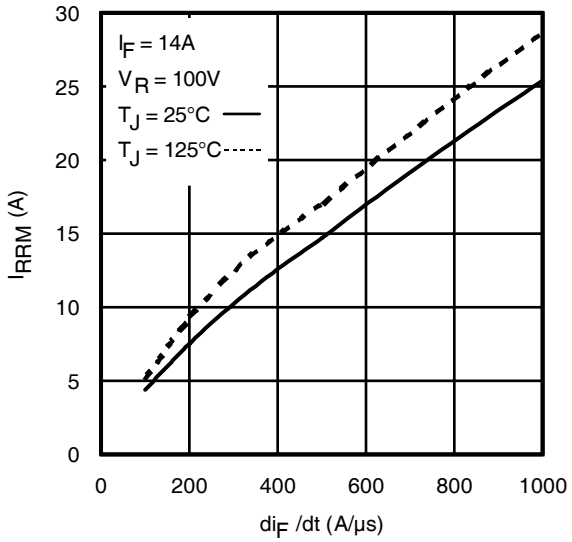


Fig. 17 - Typical Recovery Current vs. di_f/dt

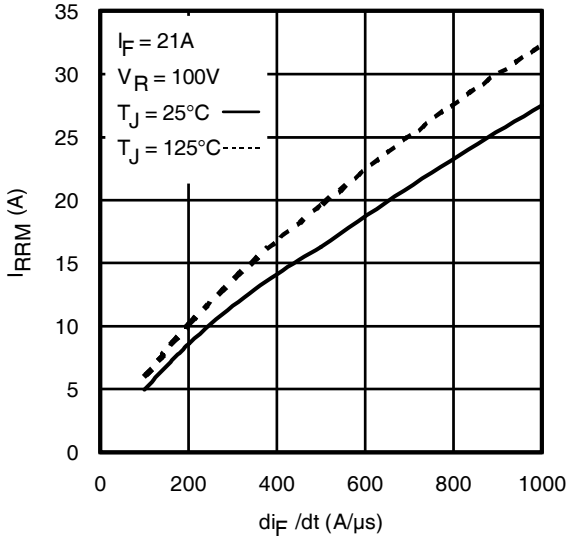


Fig. 18 - Typical Recovery Current vs. di_f/dt

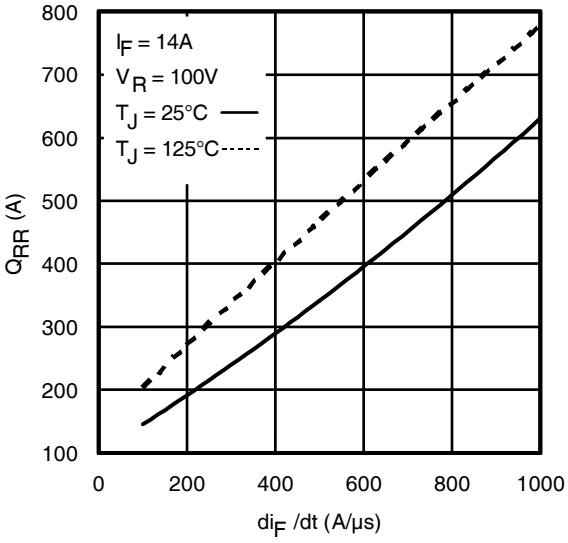


Fig. 19 - Typical Stored Charge vs. di_f/dt

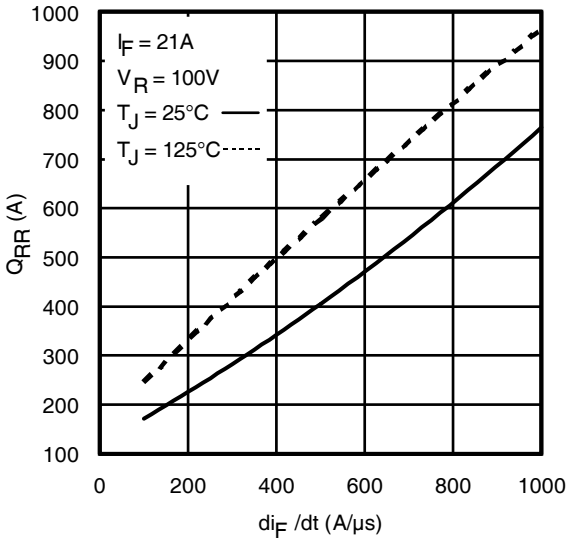


Fig. 20 - Typical Stored Charge vs. di_f/dt

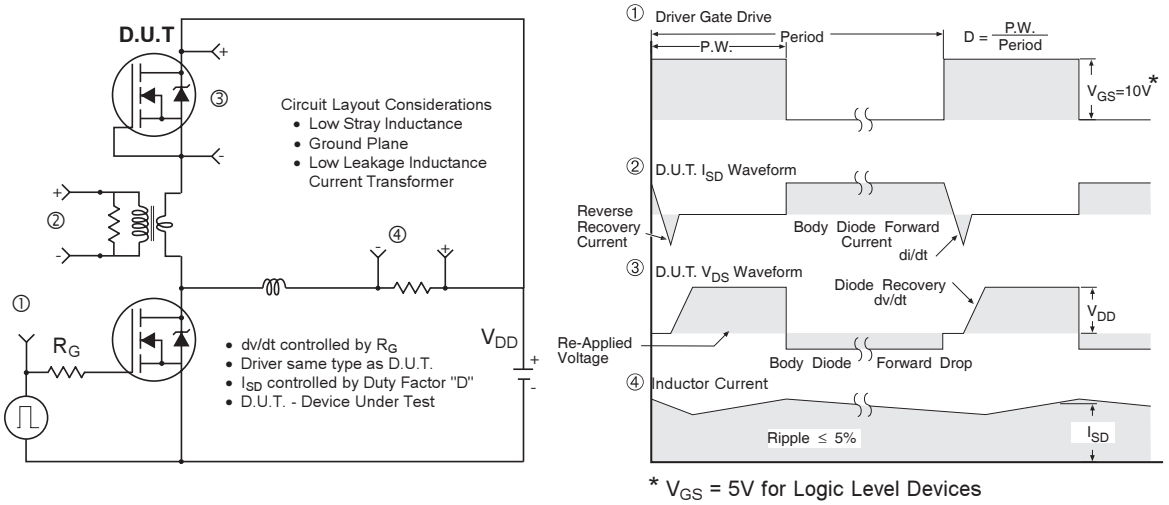


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

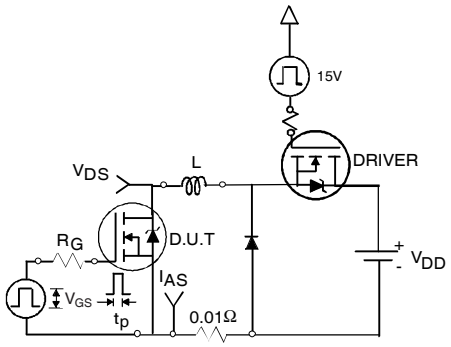


Fig 22a. Unclamped Inductive Test Circuit

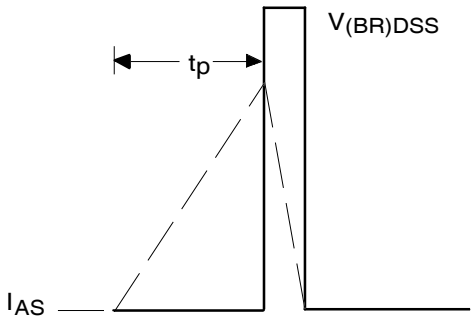


Fig 22b. Unclamped Inductive Waveforms

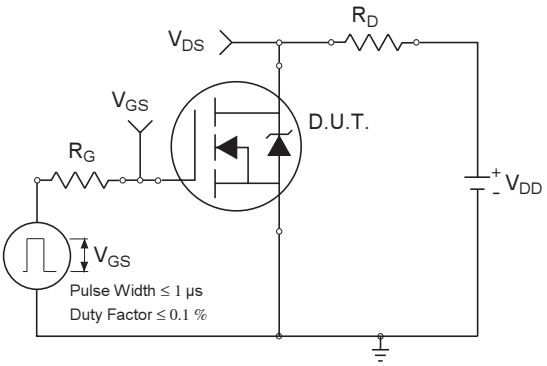


Fig 23a. Switching Time Test Circuit

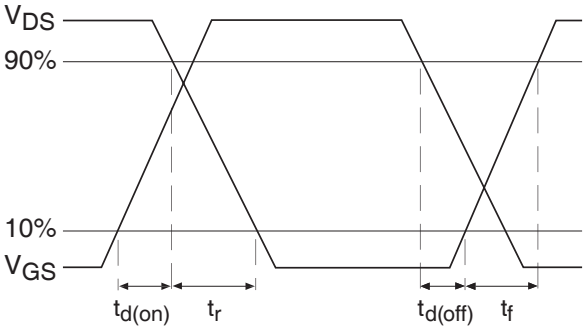


Fig 23b. Switching Time Waveforms

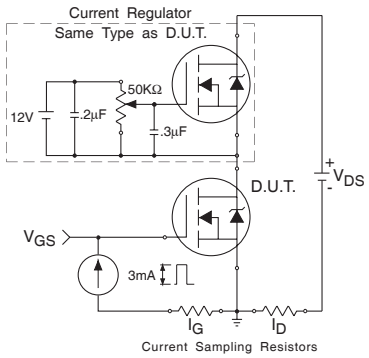


Fig 24a. Gate Charge Test Circuit

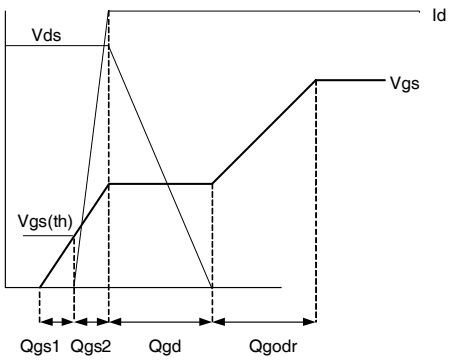
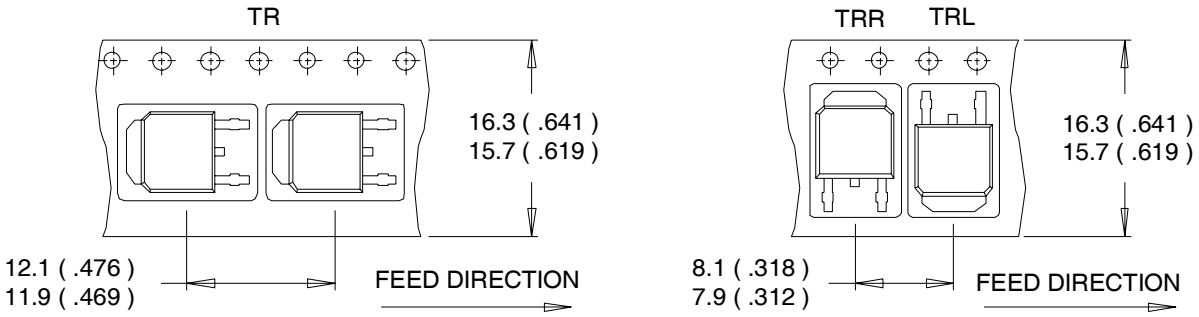


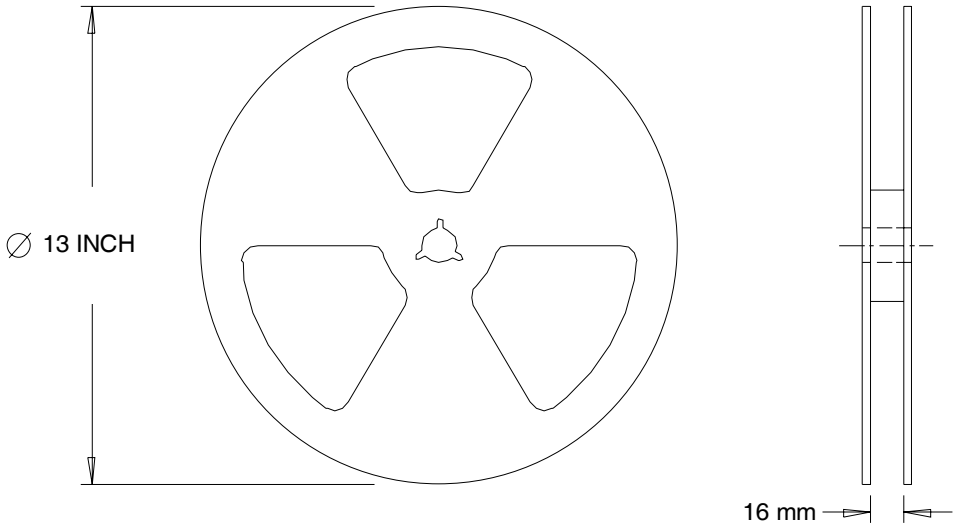
Fig 24b. Gate Charge Waveform

D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFR4615PbF	D-PAK	Tube/Bulk	75	
IRFR4615TRPbF	D-PAK	Tape and Reel	2000	
IRFU4615PbF	I-PAK	Tube/Bulk	75	

Qualification Information†

Qualification level	Industrial ††	
	(per JEDEC JESD47F††† guidelines)	
	Comments: This family of products has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level	D-PAK	MSL1
		(per JEDEC J-STD-020D†††)
	I-PAK	Not applicable
RoHS Compliant	Yes	

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.51mH R_G = 25Ω, I_{AS} = 21A, V_{GS} =10V. Part not recommended for use above this value .

③ $I_{SD} \leq$ 21A, di/dt ≤ 549A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.

④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

⑧ R_θ is measured at T_J approximately 90°C