



# High Speed CMOS 8-Bit Bus Interface Register Transceivers

QS29FCT52T  
QS29FCT53T

QS29FCT2052T  
QS29FCT2053T

## FEATURES/BENEFITS

- Pin and function compatible to the Am2952/3 29FCT52/53 and 29FCT52/53T
- CMOS power levels: <7.5 mW static
- Available in DIP, ZIP, SOIC, QSOP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

### FCT-T 2952T, 2953T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- A, B, and C speed grades with 5.5 ns  $t_{PD}$  for C
- $I_{OL} = 64$  mA Com., 48 mA Mil.

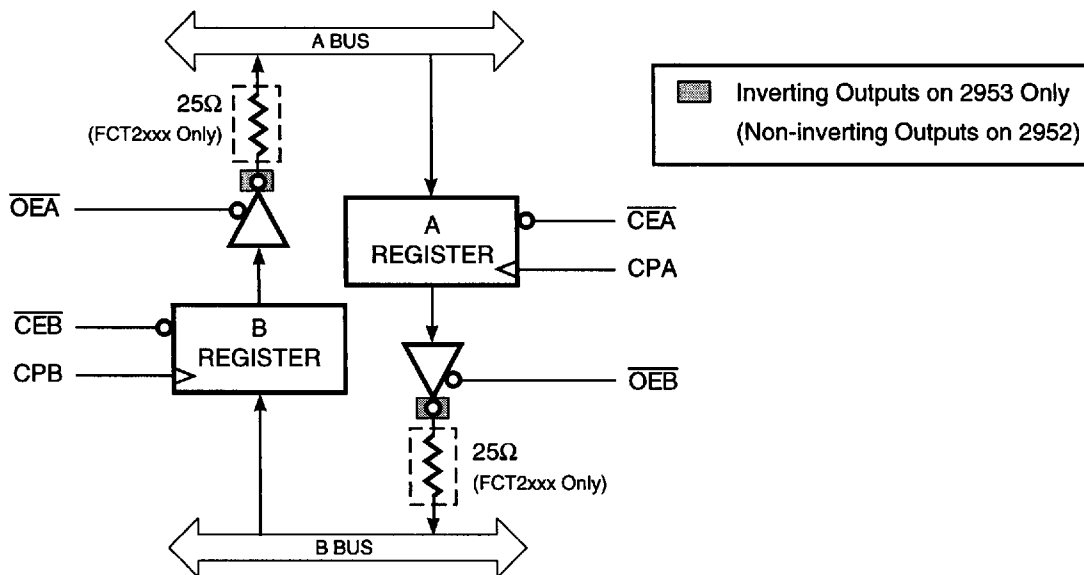
### FCT-T 2052T, 2053T

- Built-in  $25\Omega$  series resistor outputs reduce reflection and other system noise
- A, B, and C speed grades with 5.5 ns  $t_{PD}$  for C speed guaranteed with 50 pF loads

## DESCRIPTION

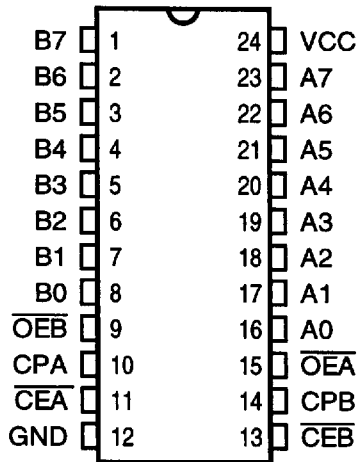
The QS29FCT52T/53T are 8-bit high-speed CMOS TTL-compatible registered bus transceivers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The QS29FCT2052/2053T devices are  $25\Omega$  resistor output versions useful for driving transmission lines and reducing system noise. The FCT2052/FCT2053 series parts can replace the FCT52/FCT53 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression, and will not load an active bus when  $V_{CC}$  is removed from the device.

## FUNCTIONAL BLOCK DIAGRAM

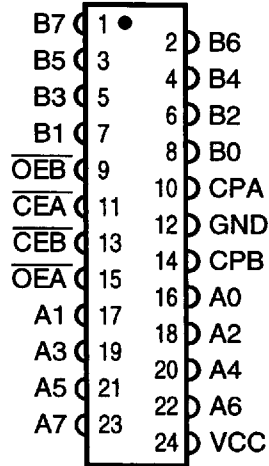


**PIN CONFIGURATIONS (All Pins Top View)**

**PDIP, SOIC, QSOP, HQSOP**



**ZIP**



**PIN DESCRIPTION**

Name	I/O	Description
A7-A0	I/O	A Bus
B7-B0	I/O	B Bus
CPA	I	Register A Clock Input
CPB	I	Register B Clock Input
$\overline{\text{CEA}}$	I	Register A Clock Enable
$\overline{\text{CEB}}$	I	Register B Clock Enable
$\overline{\text{OEA}}$	I	Output Enable, Reg. B to Bus A
$\overline{\text{OEB}}$	I	Output Enable, Reg. A to Bus B

**FUNCTION TABLES**

Inputs						Outputs	
CPA	CPB	$\overline{CEA}$	$\overline{CEB}$	$\overline{OEA}$	$\overline{OEB}$	A7-A0	B7-B0
X	X	X	X	H	L	Hi-Z	Reg. A
X	X	X	X	L	H	Reg. B	Hi-Z
X	X	X	X	H	H	Hi-Z	Hi-Z
X	X	X	X	L	L	Reg. B	Reg. A

Inputs				Outputs	
CPA	CPB	$\overline{CEA}$	$\overline{CEB}$	A7-A0	B7-B0
X	X	H	H	Hold	Hold
↑	X	L	H	Load	Hold
X	↑	H	L	Hold	Load
X	↑	L	L	X	Load
↑	X	L	L	Load	X

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20 mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50 mA
DC Output Current Max. Sink Current/Pin .....	120 mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

**CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1-11, 13-23	8	8	9	10	pF

**Note:** Capacitance is characterized but not tested.

**QS29FCT52T, 53T, 2052T, 2053T**

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current (FCTXXX)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
$I_{OR}$	Current Drive (FCT2XXX - $25\Omega$ )	$V_{CC} = \text{Max.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -12 \text{ mA (MIL)}$ $I_{OH} = -15 \text{ mA (COM)}$	2.4 2.4	—	—	V
$V_{OL}$	Output LOW Voltage (FCTXXX)	$V_{CC} = \text{Min.}, I_{OL} = 48 \text{ mA (MIL)}$ $I_{OL} = 64 \text{ mA (COM)}$	— —	—	0.55 0.55	V
$V_{OL}$	Output LOW Voltage (FCT2XXX - $25\Omega$ )	$V_{CC} = \text{Min.}, I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— —	—	0.50 0.50	V
$R_{OUT}$	Output Resistance (FCT2XXX - $25\Omega$ )	$V_{CC} = \text{Min.}, I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— 20	25 28	— 40	$\Omega$

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
I <sub>cc</sub>	Quiescent Power Supply Current	V <sub>cc</sub> = Max., freq = 0 0V ≤ V <sub>IN</sub> ≤ 0.2V or V <sub>cc</sub> -0.2V ≤ V <sub>IN</sub> ≤ V <sub>cc</sub>	—	1.5	mA
ΔI <sub>cc</sub>	Supply Current per Input @ TTL HIGH	V <sub>cc</sub> = Max., V <sub>IN</sub> = 3.4V, freq = 0 <sup>(2)</sup>	—	2.0	mA
Q <sub>ccd</sub>	Supply Current per Input per MHz	V <sub>cc</sub> = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V <sub>cc</sub> <sup>(3,4)</sup>	—	0.25	mA/ MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V<sub>IN</sub> = 3.4V).
3. For flip-flops, Q<sub>ccd</sub> is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I<sub>c</sub> can be computed using the above parameters as explained in the Technical Overview section.

**QS29FCT52T, 53T, 2052T, 2053T**

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{ pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description		52/53A 2052A 2053A		52/53B 2052B 2053B		52/53C 2052C 2053C		Unit
			Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay <sup>(1)</sup>	Com	2	10	2	6.5	2	5.8	ns
t <sub>PLH</sub>	CP to Ai, Bi, 52/53	Mil	2	11	2	7.2	0	6.8	
t <sub>PHL</sub>	Propagation Delay <sup>(1)</sup>	Com	2	10	2	6.5	2	5.8	ns
t <sub>PLH</sub>	CP to Ai, Bi, 2052/53	Mil	2	11	2	7.2	0	6.8	
t <sub>PZH</sub>	Output Enable Time <sup>(1)</sup>	Com	1.5	10.5	1.5	6.5	1.5	6.5	ns
t <sub>PZL</sub>	$\overline{OE}$ to Ai, Bi, 52/53	Mil	1.5	13	1.5	7.5	1.5	7.5	
t <sub>PZH</sub>	Output Enable Time <sup>(1)</sup>	Com	1.5	10.5	1.5	7.0	1.5	7.0	ns
t <sub>PZL</sub>	$\overline{OE}$ to Ai, Bi, 2052/53	Mil	1.5	13	1.5	7.5	1.5	7.5	
t <sub>PHZ</sub>	Output Disable Time <sup>(1,2)</sup>	Com	2	10	2	5.5	1.5	5.5	ns
t <sub>PLZ</sub>	$\overline{OE}$ to Ai, Bi	Mil	2	11	2	6.5	1.5	6.5	
t <sub>s</sub>	Data Setup Time Ai, Bi, to CP	Com	2	—	2	—	2	—	ns
		Mil	2.5	—	2	—	2	—	
t <sub>h</sub>	Data Hold Time Ai, Bi, to CP	Com	2	—	1.5	—	1.5	—	ns
		Mil	2	—	1.5	—	1.5	—	
t <sub>SCE</sub>	Clock Enable Setup Time, $\overline{CE}$ to CP	Com	2	—	2	—	2	—	ns
		Mil	2	—	2	—	2	—	
t <sub>HCE</sub>	Clock Enable Hold Time, $\overline{CE}$ to CP	Com	2	—	2	—	2	—	ns
		Mil	2	—	2	—	2	—	
t <sub>w</sub>	Clock Pulse Width <sup>(2)</sup> HIGH or LOW	Com	3	—	3	—	3	—	ns
		Mil	3	—	3	—	3	—	

**Notes:**

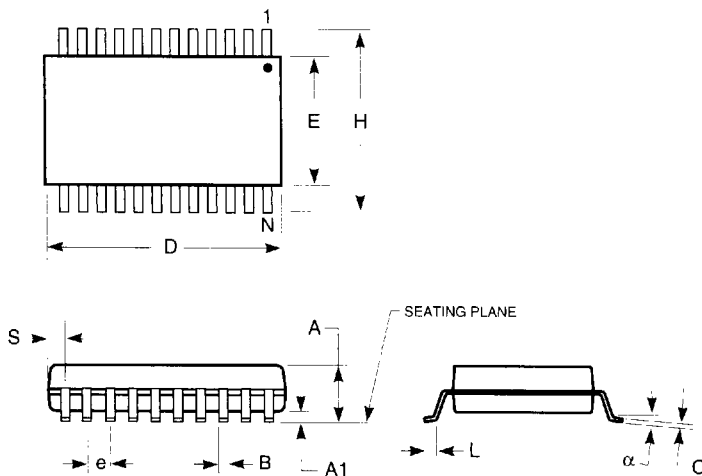
1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.

## PACKAGING INFORMATION

### 150-MIL HQSOP - Package Code H

Hermetic Quarter-Size Outline Package

Ceramic Small Outline Gull-Wing



JEDEC#	TBD			TBD		
DWG#	HSS-20A			HSS-24A		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.070	0.074	0.078	0.070	0.074	0.078
A1	0.008	0.012	0.016	0.008	0.012	0.016
B	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010
D	0.337	0.342	0.350	0.337	0.342	0.350
E	0.150	0.155	0.158	0.150	0.155	0.158
e	0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244
L	0.016	0.025	0.035	0.016	0.025	0.035
N	20			24		
$\alpha$	0°	5°	8°	0°	5°	8°
S	0.056	0.058	0.062	0.031	0.033	0.037

**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition.
5. Lead coplanarity is 0.004 in. maximum.

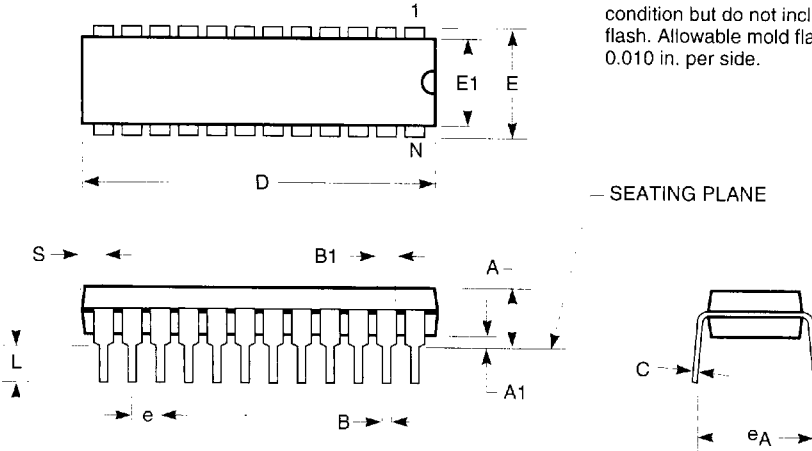
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## PACKAGING INFORMATION

### 300-MIL PDIP - Package Code P Plastic Dual In-line Package

**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010 in. per side.



JEDEC#	MS-001AC		MS001AA		MS-001AE		N/A		MS-001AF		MO-095AH	
DWG#	PD14A		PD16A		PD20A		PT22B		PT24A		PT28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.180
A1	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
B	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020
B1	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.060
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.745	0.765	0.745	0.765	1.020	1.040	1.020	1.040	1.150	1.260	1.345	1.385
E	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
E1	0.240	0.270	0.240	0.270	0.240	0.270	0.240	0.270	0.250	0.280	0.275	0.295
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
e <sub>A</sub>	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380
L	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
S	0.070	0.080	0.020	0.035	0.060	0.070	0.010	0.020	0.025	0.080	0.020	0.040
N	14		16		20		22		24		28	

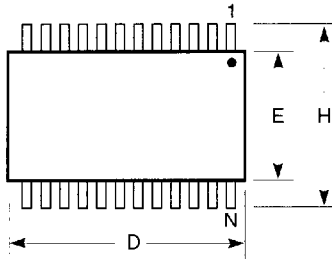
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## PACKAGING INFORMATION

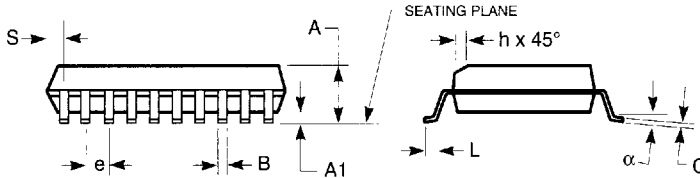
### 150-MIL QSOP - Package Code Q

Quarter-Size Outline Package  
Plastic Small Outline Gull-Wing



**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.



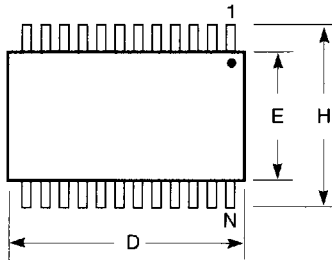
JEDEC#	MO-137AB			MO-137AD			MO-137AE			MO-137AF		
DWG#	PSS-16A			PSS-20A			PSS-24A			PSS-28A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
D	0.189	0.193	0.197	0.337	0.341	0.344	0.337	0.341	0.344	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24			28		
alpha	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.009	0.010	0.056	0.058	0.060	0.031	0.033	0.035	0.031	0.033	0.035

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## PACKAGING INFORMATION

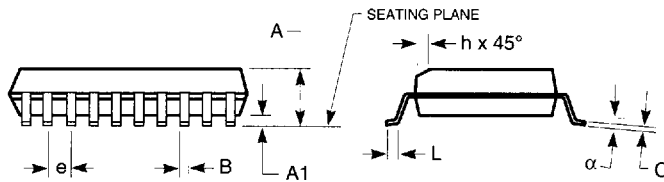
### 300-MIL SOIC - Package Code SO

Plastic Small Outline Gull-Wing



**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.



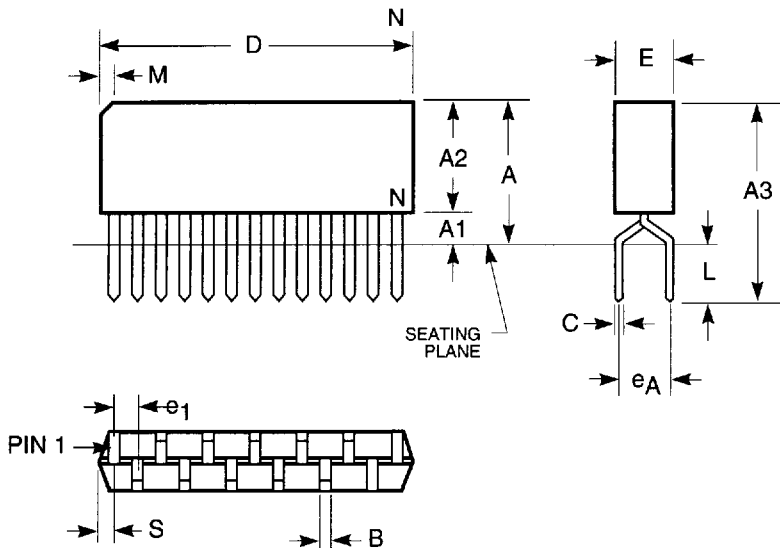
JEDEC#	MS-013AA		MS-013AC		MS-013AD		MS-013AE	
DWG#	PS16A		PS20A		PS24A		PS28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.096	0.104
A1	0.005	0.011	0.005	0.011	0.005	0.011	0.005	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.402	0.412	0.500	0.510	0.602	0.612	0.701	0.711
E	0.292	0.299	0.292	0.299	0.292	0.299	0.292	0.299
e	0.044	0.056	0.044	0.056	0.044	0.056	0.044	0.056
H	0.396	0.416	0.396	0.416	0.396	0.416	0.396	0.416
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
N	16		20		24		28	
α	0°	8°	0°	8°	0°	8°	0°	8°

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## PACKAGING INFORMATION

### 300-MIL ZIP - Package Code Z

Zig-zag In-line Packages



JEDEC#	MO-072AB		MO-072AC		MO-072AD	
DWG#	PZ20A		PZ24A		PZ28A	
Symbol	Min	Max	Min	Max	Min	Max
A	0.350	0.400	0.350	0.400	0.350	0.400
A1	0.030	0.070	0.030	0.070	0.032	0.055
A2	0.280	0.340	0.320	0.350	0.335	0.345
A3	0.450	0.550	0.450	0.550	0.460	0.550
B	0.015	0.024	0.015	0.024	0.015	0.024
C	0.008	0.012	0.008	0.012	0.008	0.012
D	1.008	1.030	1.200	1.250	1.409	1.424
E	0.100	0.120	0.100	0.120	0.110	0.120
e1	0.050 BSC		0.050 BSC		0.050 BSC	
eA	0.100 BSC		0.100 BSC		0.100 BSC	
L	0.100	0.150	0.100	0.150	0.110	0.150
M	0.035	0.085	0.035	0.085	0.035	0.085
N	20		24		28	
S	0.018	0.032	0.018	0.032	0.025	0.038

**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010 in. per side.

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