

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# HAT2141H

Silicon N Channel Power MOS FET  
Power Switching

**RENESAS**

ADE-208-1582E(Z)

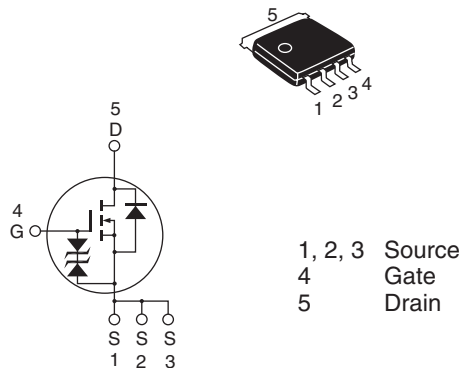
Preliminary  
6th. Edition  
Sep. 2002

## Features

- Capable of 7 V gate drive
- Low drive current
- High density mounting
- Low on-resistance  
 $R_{DS(on)} = 22 \text{ m}\Omega$  typ. (at  $V_{GS} = 10 \text{ V}$ )

## Outline

LFPAK



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	100	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	15	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	60	A
Body-drain diode reverse drain current	$I_{DR}$	15	A
Avalanche current	$I_{AP}$ <sup>Note 3</sup>	15	A
Avalanche energy	$E_{AR}$ <sup>Note 3</sup>	22.5	mJ
Channel dissipation	$Pch$ <sup>Note2</sup>	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to + 150	°C

Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$

2.  $T_c = 25^\circ C$

3. Value at Tch = 25°C,  $R_g \geq 50 \Omega$

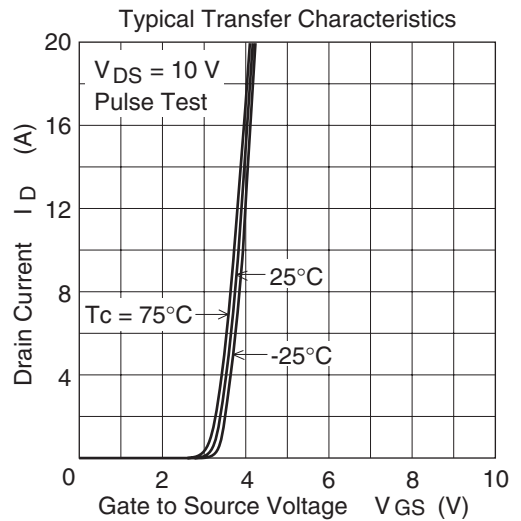
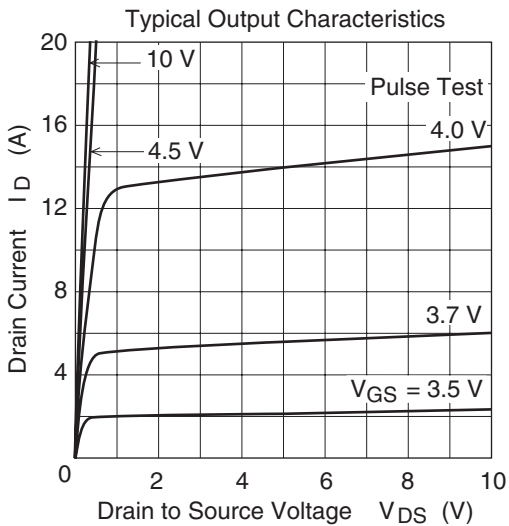
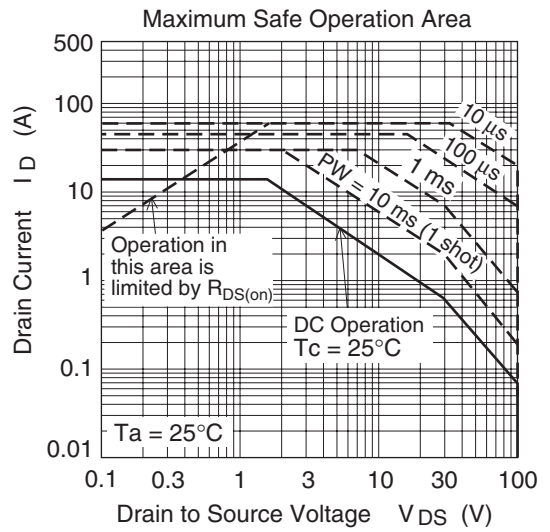
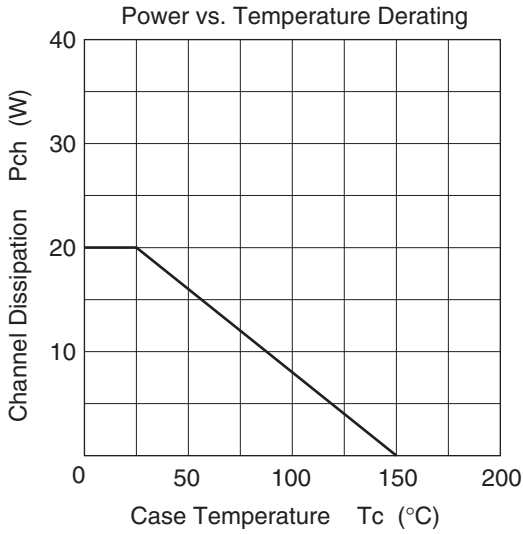
## Electrical Characteristics

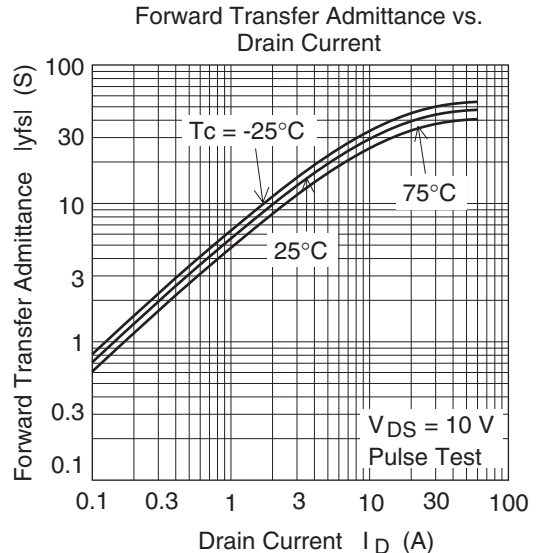
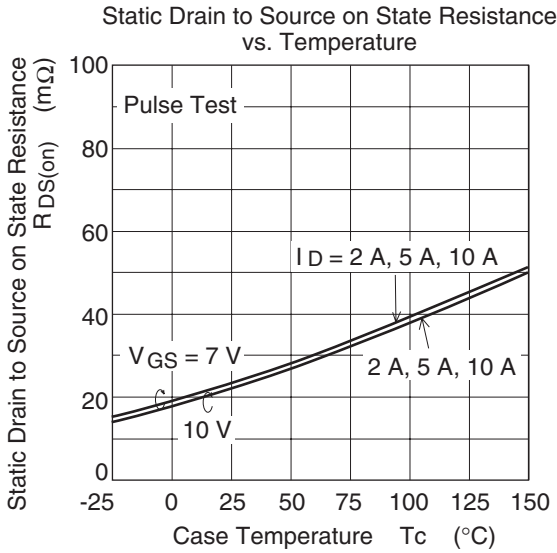
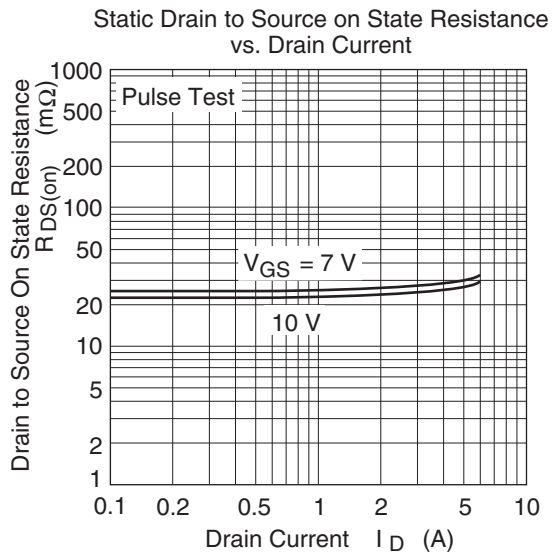
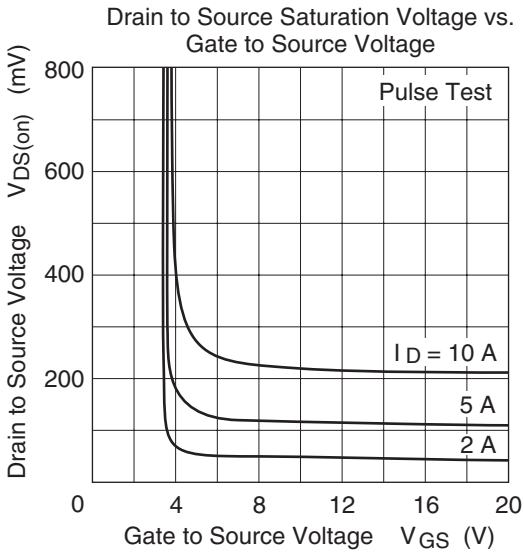
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 100 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	22	27.5	$\text{m}\Omega$	$I_D = 7.5 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	23.5	32	$\text{m}\Omega$	$I_D = 7.5 \text{ A}$ , $V_{GS} = 7 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	15	25	—	S	$I_D = 7.5 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note4</sup>
Input capacitance	Ciss	—	3200	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	Coss	—	255	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	125	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Qg	—	46	—	nc	$V_{DD} = 50 \text{ V}$
Gate to source charge	Qgs	—	11	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Qgd	—	10	—	nc	$I_D = 15 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	22	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 7.5 \text{ A}$
Rise time	$t_r$	—	13	—	ns	$V_{DD} \cong 30 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	$R_L = 4 \text{ }\Omega$
Fall time	$t_f$	—	10	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	$V_{DF}$	—	0.82	1.07	V	$I_F = 15 \text{ A}$ , $V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	50	—	ns	$I_F = 15 \text{ A}$ , $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

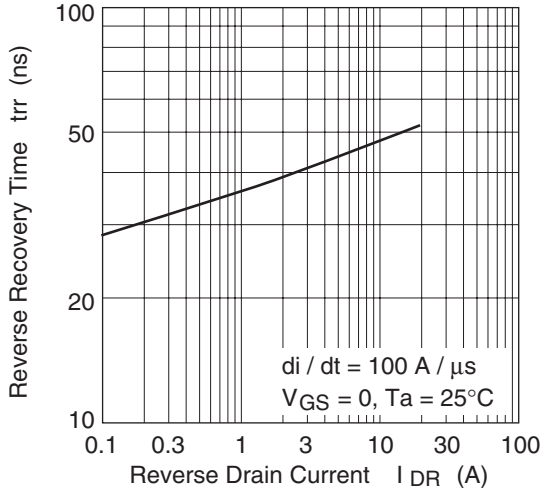
Notes: 4. Pulse test

## Main Characteristics

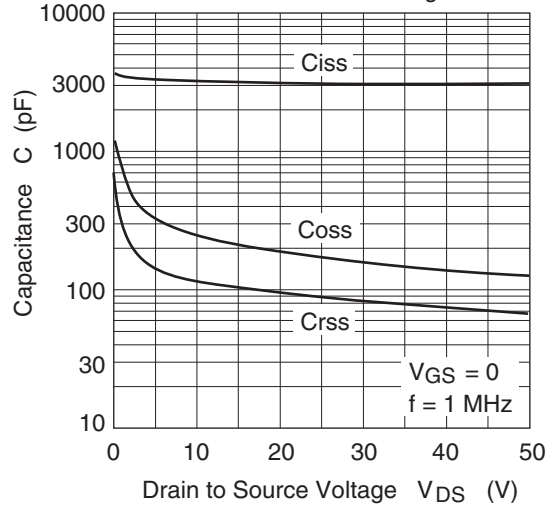




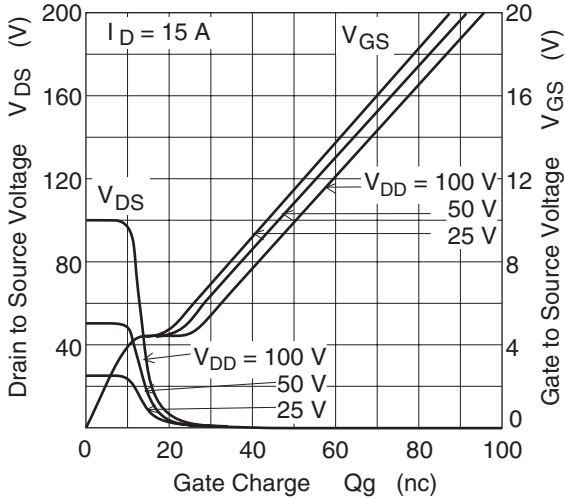
Body-Drain Diode Reverse Recovery Time



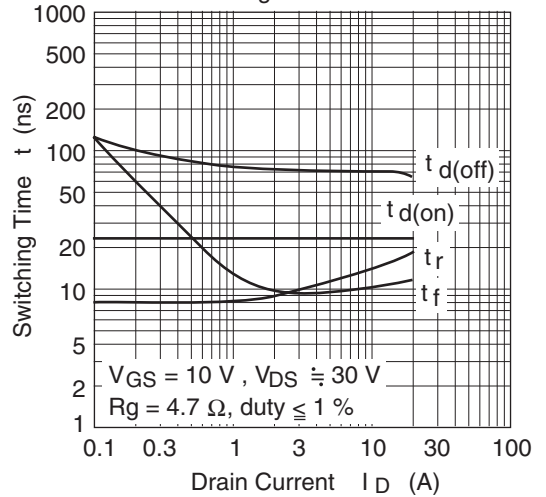
Typical Capacitance vs. Drain to Source Voltage



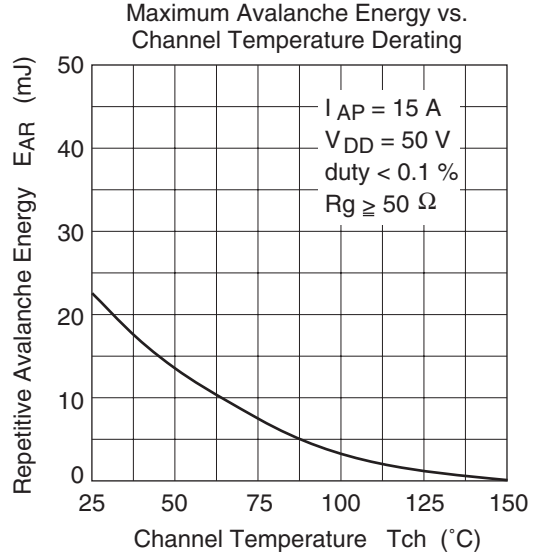
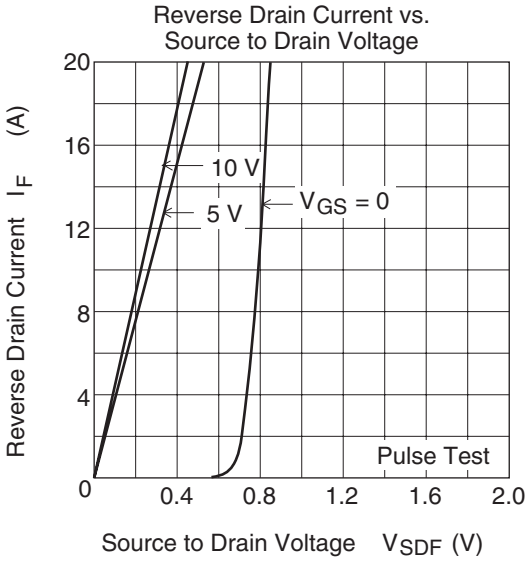
Dynamic Input Characteristics



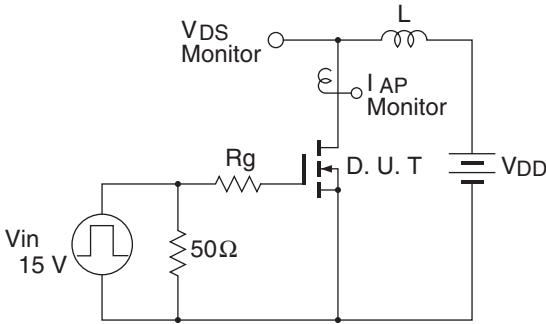
Switching Characteristics



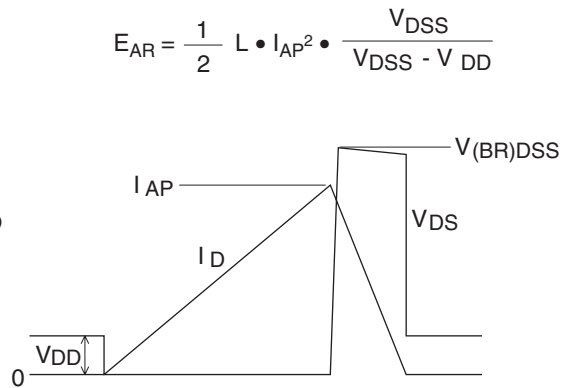




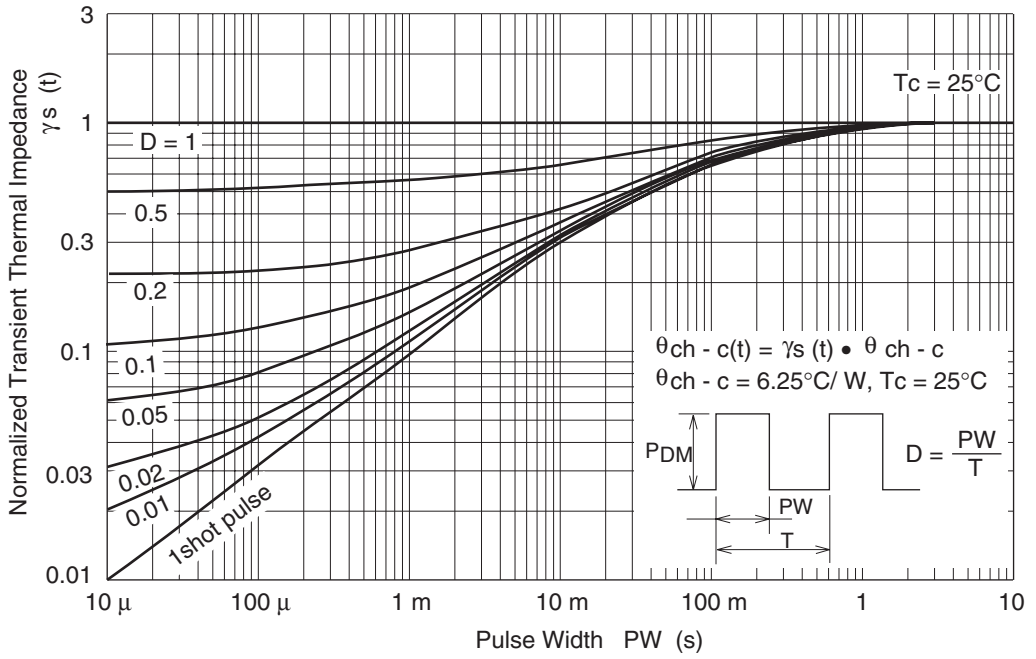
Avalanche Test Circuit



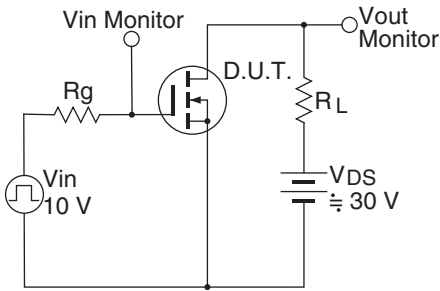
Avalanche Waveform



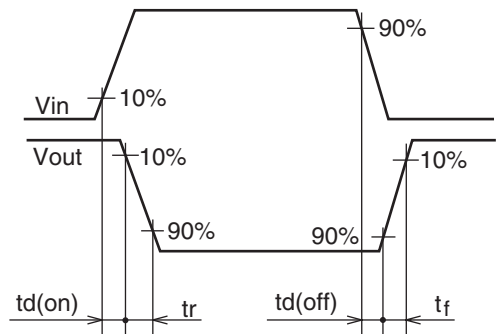
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

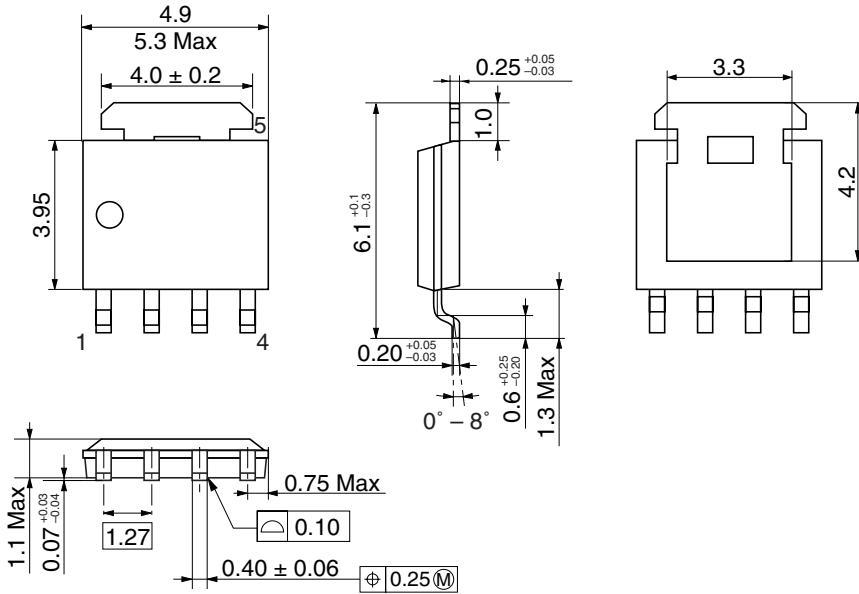
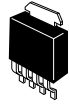


Switching Time Waveform



Package Dimensions

As of July, 2002  
Unit: mm



Hitachi Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

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