

4-1/2 Digit A/D Converter

Features

- Low Rollover Error: ± 1 Count Max
- Nonlinearity Error: ± 1 Count Max
- Reading for 0V Input
- True Polarity Indication at Zero for Null Detection
- Multiplexed BCD Data Output
- TTL-Compatible Outputs
- Differential Input
- Control Signals Permit Interface to UARTs and Microprocessors
- Blinking Display Visually Indicates Overrange Condition
- Low Input Current: 1pA
- Low Zero Reading Drift: $2\mu\text{V}/^\circ\text{C}$
- Auto-Ranging Supported with Overrange and Underrange Signals
- Available in PDIP and Surface-Mount Packages

Applications

- Precision Analog Signal Processor
- Precision Sensor Interface
- High Accuracy DC Measurements

Device Selection Table

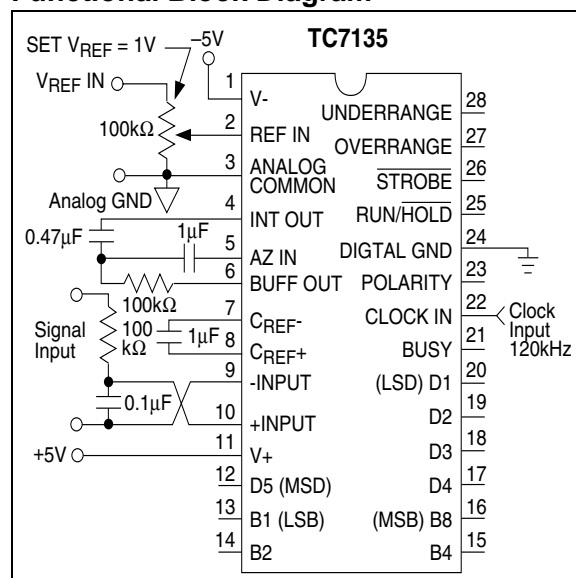
Part Number	Package	Temperature Range
TC7135CLI	28-Pin PLCC	0°C to +70°C
TC7135CPI	28-Pin PDIP	0°C to +70°C
TC7135CBU	64-Pin PQFP	0°C to +70°C

General Description

The TC7135 4-1/2 digit A/D converter (ADC) offers 50ppm (1 part in 20,000) resolution with a maximum nonlinearity error of 1 count. An auto zero cycle reduces zero error to below $10\mu\text{V}$ and zero drift to $0.5\mu\text{V}/^\circ\text{C}$. Source impedance errors are minimized by a 10pA maximum input current. Rollover error is limited to ± 1 count.

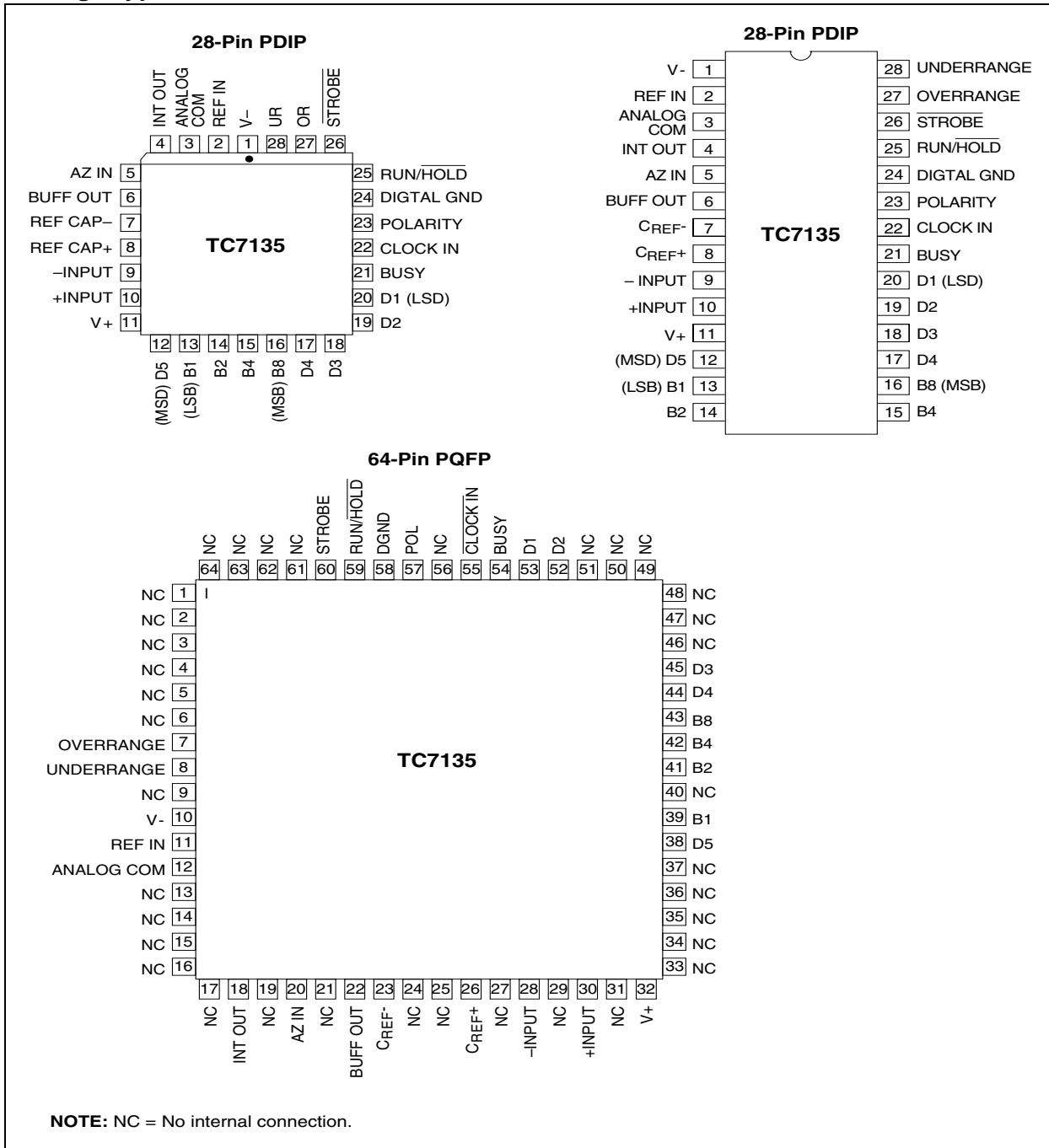
Microprocessor based measurement systems are supported by BUSY, STROBE and RUN/HOLD control signals. Remote data acquisition systems with data transfer via UARTs are also possible. The additional control pins and multiplexed BCD outputs make the TC7135 the ideal converter for display or microprocessor based measurement systems.

Functional Block Diagram



TC7135

Package Types



1.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings*

Positive Supply Voltage.....	+6V
Negative Supply Voltage	- 9V
Analog Input Voltage (Pin 9 or 10)	V+ to V- (Note 2)
Reference Input Voltage (Pin 2)	V+ to V-
Clock Input Voltage	0V to V+
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	- 65°C to +150°C
Package Power Dissipation; ($T_A \leq 70^\circ\text{C}$)	
28-Pin PDIP	1.14Ω
28-Pin PLCC	1.00Ω
64-Pin PQFP	1.14Ω

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC7135 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: $T_A = +25^\circ\text{C}$, $F_{\text{CLOCK}} = 120\text{kHz}$, $V_+ = +5\text{V}$, $V_- = -5\text{V}$, unless otherwise specified (see Functional Block Diagram).						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Analog						
	Display Reading with Zero Volt Input	-0.0000	± 0.0000	+0.0000	Display Reading	Note 2 and Note 3
TC_Z	Zero Reading Temperature Coefficient	—	0.5	2	$\mu\text{V}/^\circ\text{C}$	$V_{\text{IN}} = 0\text{V}$, (Note 4)
TC_{FS}	Full Scale Temperature Coefficient	—	—	5	ppm/ $^\circ\text{C}$	$V_{\text{IN}} = 2\text{V}$, (Note 4 and Note 5)
NL	Nonlinearity Error	—	0.5	1	Count	Note 6
DNL	Differential Linearity Error	—	0.01	—	LSB	Note 6
	Display Reading in Ratiometric Operation	+0.9996	+0.9999	+1.0000	Display Reading	$V_{\text{IN}} = V_{\text{REF}}$, (Note 2)
$\pm\text{FSE}$	\pm Full Scale Symmetry Error (Rollover Error)	—	0.5	1	Count	$-V_{\text{IN}} = +V_{\text{IN}}$, (Note 7)
I_{IN}	Input Leakage Current	—	1	10	pA	Note 3
e_{N}	Noise	—	15	—	$\mu\text{V}_{\text{P-P}}$	Peak-to-Peak Value not Exceeded 95% of Time
Digital						
I_{IL}	Input Low Current	—	10	100	μA	$V_{\text{IN}} = 0\text{V}$
I_{IH}	Input High Current	—	0.08	10	μA	$V_{\text{IN}} = +5\text{V}$
V_{OL}	Output Low Voltage	—	0.2	0.4	V	$I_{\text{OL}} = 1.6\text{mA}$
V_{OH}	Output High Voltage; B ₁ , B ₂ , B ₄ , B ₈ , D ₁ –D ₅ Busy, Polarity, Overrange, Underrange, Strobe	2.4	4.4	5	V	$I_{\text{OH}} = 1\text{mA}$
		4.9	4.99	5	V	$I_{\text{OH}} = 10\mu\text{A}$
F_{CLK}	Clock Frequency	0	200	1200	kHz	Note 8

Note 1: Limit input current to under 100 μA if input voltages exceed supply voltage.
 2: Full scale voltage = 2V.
 3: $V_{\text{IN}} = 0\text{V}$.
 4: $30^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
 5: External reference temperature coefficient less than 0.01ppm/ $^\circ\text{C}$.
 6: $-2\text{V} \leq V_{\text{IN}} \leq +2\text{V}$. Error of reading from best fit straight line.
 7: $|V_{\text{IN}}| = 1.9959$.
 8: Specification related to clock frequency range over which the TC7135 correctly performs its various functions. Increased errors result at higher operating frequencies.

TC7135

TC7135 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: $T_A = +25^\circ\text{C}$, $F_{\text{CLOCK}} = 120\text{kHz}$, $V_+ = +5\text{V}$, $V_- = -5\text{V}$, unless otherwise specified (see Functional Block Diagram).

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Power Supply						
V+	Positive Supply Voltage	4	5	6	V	
V-	Negative Supply Voltage	-3	-5	-8	V	
I+	Positive Supply Current	—	1	3	mA	$F_{\text{CLK}} = 0\text{Hz}$
I-	Negative Supply Current	—	0.7	3	mA	$F_{\text{CLK}} = 0\text{Hz}$
PD	Power Dissipation	—	8.5	30	mW	$F_{\text{CLK}} = 0\text{Hz}$

- Note**
- 1: Limit input current to under $100\mu\text{A}$ if input voltages exceed supply voltage.
 - 2: Full scale voltage = 2V.
 - 3: $V_{\text{IN}} = 0\text{V}$.
 - 4: $30^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
 - 5: .External reference temperature coefficient less than $0.01\text{ppm}/^\circ\text{C}$.
 - 6: $-2\text{V} \leq V_{\text{IN}} \leq +2\text{V}$. Error of reading from best fit straight line.
 - 7: $|V_{\text{IN}}| = 1.9959$.
 - 8: Specification related to clock frequency range over which the TC7135 correctly performs its various functions. Increased errors result at higher operating frequencies.

2.0 PIN DESCRIPTIONS

The description of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number 28-Pin PDIP	Symbol	Description
1	V-	Negative power supply input.
2	REF IN	External reference input.
3	ANALOG COMMON	Reference point for REF IN.
4	INT OUT	Integrator output. Integrator capacitor connection.
5	AZ IN	Auto zero inpt. Auto-zero capacitor connection.
6	BUFF OUT	Analog input buffer output. Integrator resistor connection.
7	C _{REF-}	Reference capacitor input. Reference capacitor negative connection.
8	C _{REF+}	Reference capacitor input. Reference capacitor positive connection.
9	-INPUT	Analog input. Analog input negative connection.
10	+INPUT	Analog input. Analog input positive connection.
11	V+	Positive power supply input.
12	D5	Digit drive output. Most Significant Digit (MSD)
13	B1	Binary Coded Decimal (BCD) output. Least Significant Bit (LSB)
14	B2	BCD output.
15	B4	BCD output.
16	B8	BCD output. Most Significant Bit (MSB)
17	D4	Digit drive output.
18	D3	Digit drive output.
19	D2	Digit drive output.
20	D1	Digit drive output. Least Significant Digit (LSD)
21	BUSY	Busy output. At the beginning of the signal-integration phase, BUSY goes High and remains High until the first clock pulse after the integrator zero crossing.
22	CLOCK IN	Clock input. Conversion clock connection.
23	POLARITY	Polarity output. A positive input is indicated by a logic High output. The polarity output is valid at the beginning of the reference integrate phase and remains valid until determined during the next conversion.
24	DGND	Digital logic reference input.
25	RUN/HOLD	Run / Hold input. When at a logic High, conversions are performed continuously. A logic Low holds the current data as long as the Low condition exists.
26	$\overline{\text{STROBE}}$	Strobe output. The STROBE output pulses low in the center of the digit drive outputs.
27	OVERRANGE	Over range output. A logic High indicates that the analog input exceeds the full scale input range.
28	UNDERRANGE	Under range output. A logic High indicates that the analog input is less than 9% of the full scale input range.

TC7135

3.0 DETAILED DESCRIPTION

(All Pin Designations Refer to 28-Pin DIP)

3.1 Dual Slope Conversion Principles

The TC7135 is a dual slope, integrating A/D converter. An understanding of the dual slope conversion technique will aid in following the detailed TC7135 operational theory.

The conventional dual slope converter measurement cycle has two distinct phases:

1. Input signal integration
2. Reference voltage integration (de-integration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

EQUATION 3-1:

$$\frac{1}{R_{INT}C_{INT}} \int_0^{T_{INT}} V_{IN}(T)DT = \frac{V_{REF} T_{DEINT}}{R_{INT}C_{INT}}$$

where:

- V_{REF} = Reference voltage
- T_{INT} = Signal integration time (fixed)
- T_{DEINT} = Reference voltage integration time (variable).

For a constant V_{IN} :

EQUATION 3-2:

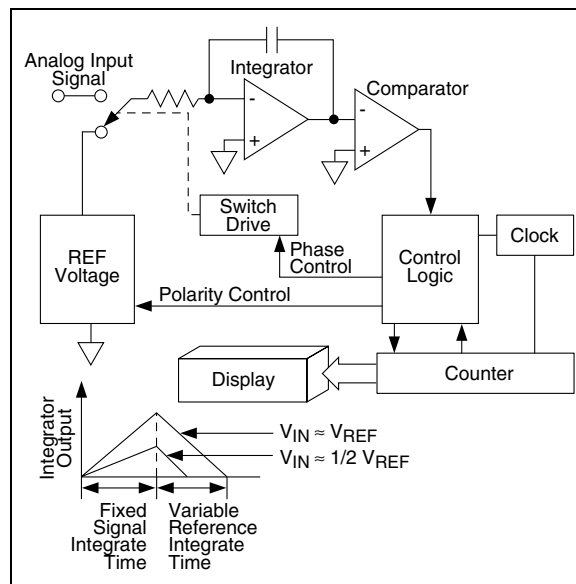
$$V_{IN} = \frac{V_{REF} T_{DEINT}}{T_{INT}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. An inher-

ent benefit is noise immunity. Noise spikes are integrated, or averaged, to zero during the integration periods.

Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments (see Figure 3-1).

FIGURE 3-1: BASIC DUAL SLOPE CONVERTER



3.2 TC7135 Operational Theory

The TC7135 incorporates a system zero phase and integrator output voltage zero phase to the normal two-phase dual-slope measurement cycle. Reduced system errors, fewer calibration steps, and a shorter over-range recovery time result.

The TC7135 measurement cycle contains four phases:

1. System zero
2. Analog input signal integration
3. Reference voltage integration
4. Integrator output zero

Internal analog gate status for each phase is shown in Figure 3-1.

TABLE 3-1: INTERNAL ANALOG GATE STATUS

Conversion Cycle Phase	SW _I	SW _{RI+}	SW _{RI-}	SW _Z	SW _R	SW ₁	SW _{Iz}	Reference Figures
System Zero				Closed	Closed	Closed		Figure 3-2
Input Signal Integration	Closed							Figure 3-3
Reference Voltage Integration		Closed*				Closed		Figure 3-4
Integrator Output Zero						Closed	Closed	Figure 3-5

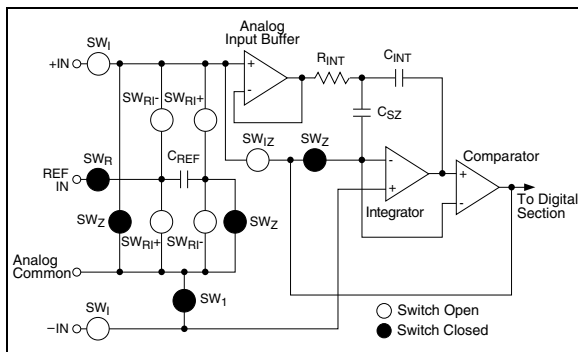
*Note: Assumes a positive polarity input signal. SW_{RI-} would be closed for a negative input signal.

3.2.1 SYSTEM ZERO

During this phase, errors due to buffer, integrator, and comparator offset voltages are compensated for by charging C_{AZ} (auto zero capacitor) with a compensating error voltage. With a zero input voltage the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_1 switches. The internal input points connect to ANALOG COMMON. The reference capacitor charges to the reference voltage potential through SW_R . A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator, and comparator offset voltages (see Figure 3-2).

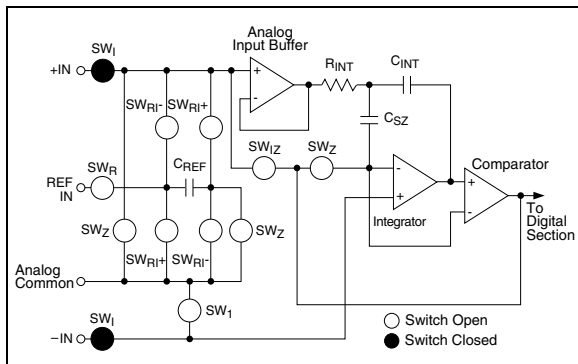
FIGURE 3-2: SYSTEM ZERO PHASE



3.2.2 ANALOG INPUT SIGNAL INTEGRATION

The TC7135 integrates the differential voltage between the +INPUT and -INPUT pins. The differential voltage must be within the device Common mode range; -1V from either supply rail, typically. The input signal polarity is determined at the end of this phase. See Figure 2-3

FIGURE 3-3: INPUT SIGNAL INTEGRATION PHASE



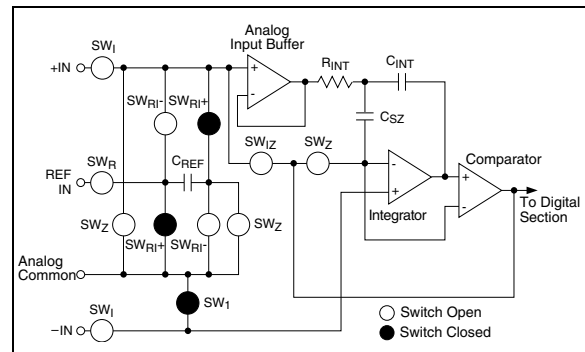
3.2.3 REFERENCE VOLTAGE INTEGRATION

The previously-charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero (see Figure 3-4). The digital reading displayed is:

EQUATION 3-3:

$$\text{Reading} = 10,000 \frac{[\text{Differential Input}]}{V_{\text{REF}}}$$

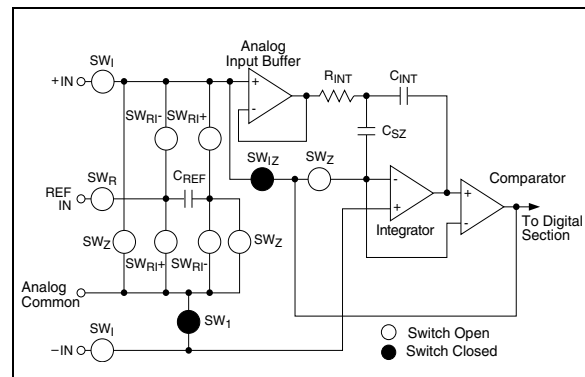
FIGURE 3-4: REFERENCE VOLTAGE INTEGRATION CYCLE



3.2.4 INTEGRATOR OUTPUT ZERO

This phase ensures the integrator output is at 0V when the system zero phase is entered. It also ensures that the true system offset voltages are compensated for. This phase normally lasts 100 to 200 clock cycles. If an overrange condition exists, the phase is extended to 6200 clock cycles (see Figure 3-5).

FIGURE 3-5: INTEGRATOR OUTPUT ZERO PHASE



4.0 ANALOG SECTION FUNCTIONAL DESCRIPTION

4.1 Differential Inputs

The TC7135 operates with differential voltages (+INPUT, pin 10 and -INPUT, pin 9) within the input amplifier Common mode range, which extends from 1V below the positive supply to 1V above the negative supply. Within this Common mode voltage range, an 86dB Common mode rejection ratio is typical.

The integrator output also follows the Common mode voltage and must not be allowed to saturate. A worst-case condition exists, for example, when a large positive Common mode voltage with a near full scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive Common mode voltage. For these critical applications, the integrator swing can be reduced to less than the recommended 4V full scale swing, with some loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

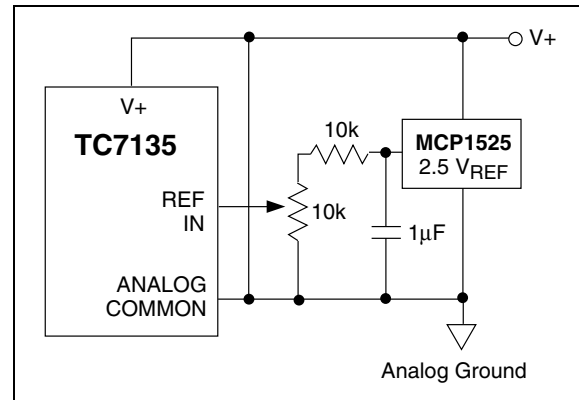
4.2 Analog Common Input

ANALOG COMMON is used as the -INPUT return during auto zero and de-integrate. If -INPUT is different from ANALOG COMMON, a Common mode voltage exists in the system. However, this signal is rejected by the excellent CMRR of the converter. In most applications, -INPUT will be set at a fixed, known voltage (power supply common, for instance). In this application, ANALOG COMMON should be tied to the same point, thus removing the Common mode voltage from the converter. The reference voltage is referenced to ANALOG COMMON.

4.3 Reference Voltage Input

The reference voltage input (REF IN) must be a positive voltage with respect to ANALOG COMMON. A reference voltage circuit is shown in Figure 4-1.

FIGURE 4-1: USING AN EXTERNAL REFERENCE



5.0 DIGITAL SECTION FUNCTIONAL DESCRIPTION

The major digital subsystems within the TC7135 are illustrated in Figure 5-1, with timing relationships shown in Figure 5-2. The multiplexed BCD output data can be displayed on LCD or LED displays. The digital section is best described through a discussion of the control signals and data outputs.

FIGURE 5-1: DIGITAL SECTION FUNCTIONAL DIAGRAM

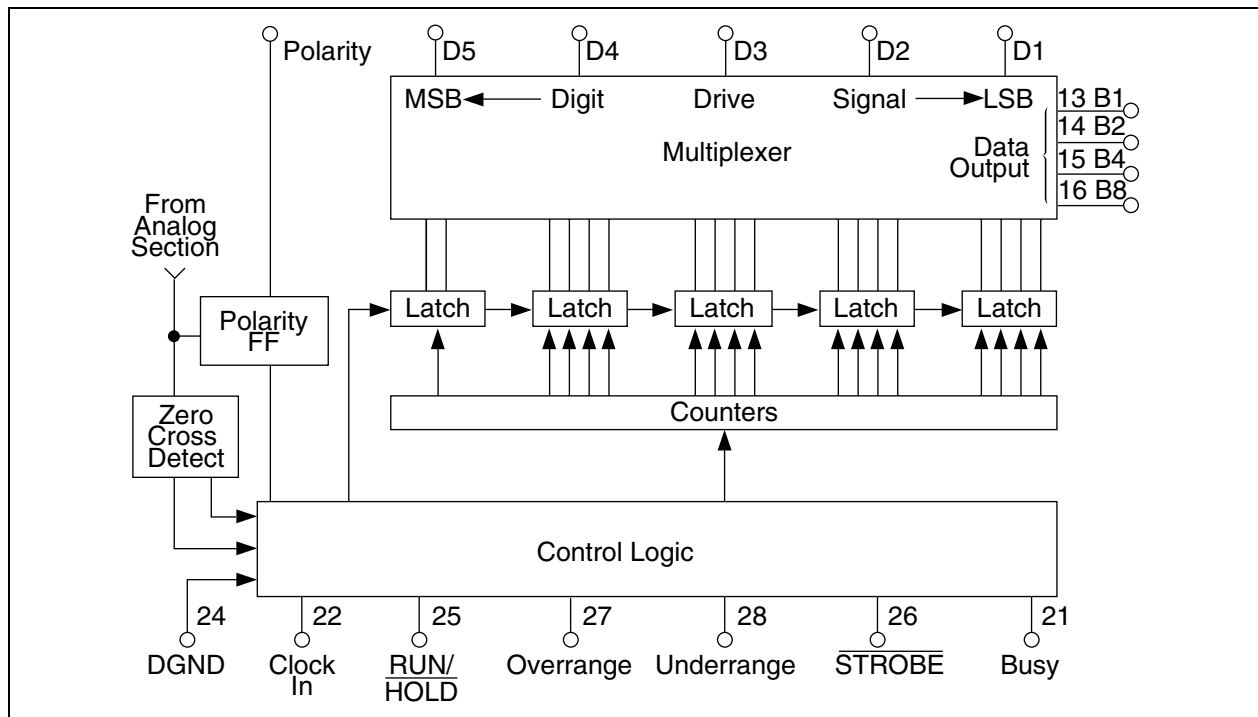
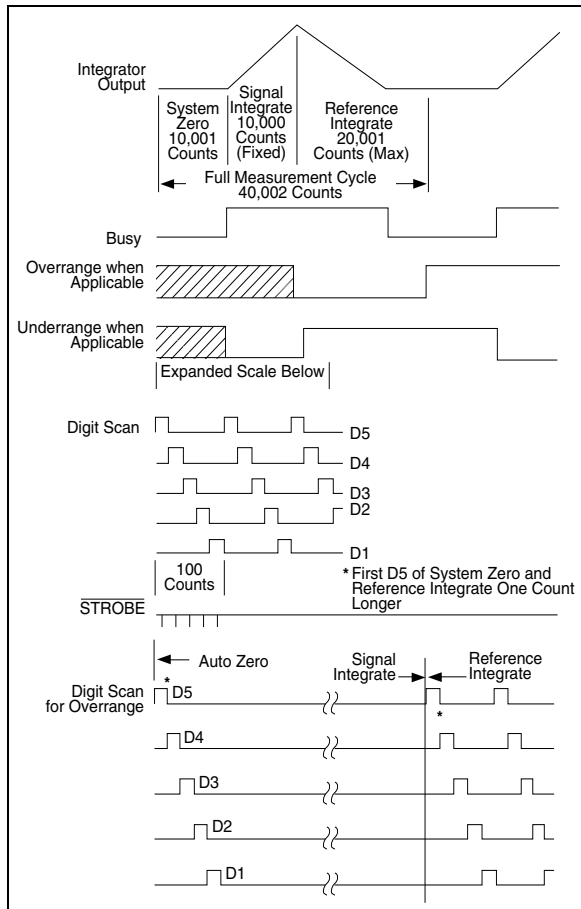


FIGURE 5-2: TIMING DIAGRAMS FOR OUTPUTS



5.1 RUN/HOLD Input

When left open, this pin assumes a logic "1" level. With a RUN/HOLD = 1, the TC7135 performs conversions continuously, with a new measurement cycle beginning every 40,002 clock pulses.

When RUN/HOLD changes to a logic "0," the measurement cycle in progress will be completed, data held and displayed, as long as the logic "0" condition exists.

A positive pulse (>300nsec) at RUN/HOLD initiates a new measurement cycle. The measurement cycle in progress when RUN/HOLD initially assumed the logic "0" state must be completed before the positive pulse can be recognized as a single conversion run command.

The new measurement cycle begins with a 10,001-count auto zero phase. At the end of this phase the busy signal goes high.

5.2 STROBE Output

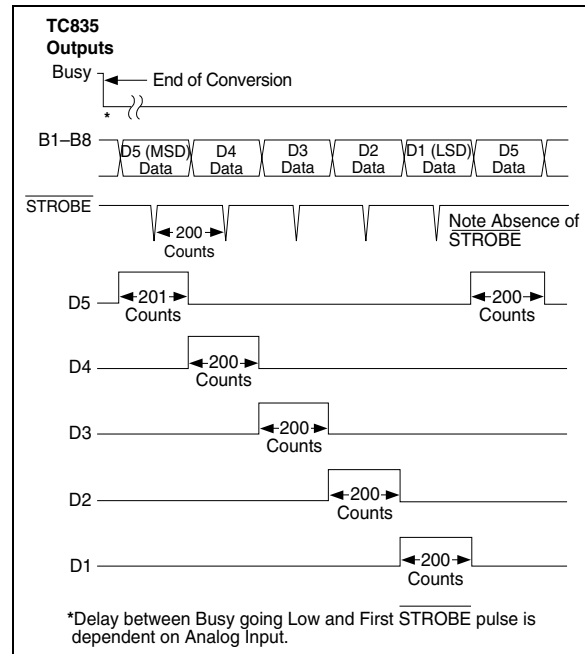
During the measurement cycle, the $\overline{\text{STROBE}}$ control line is pulsed low five times. The five low pulses occur in the center of the digit drive signals (D₁, D₂, D₃, D₅) (see Figure 5-3).

D₅ (MSD) goes high for 201 counts when the measurement cycles end. In the center of the D₅ pulse, 101 clock pulses after the end of the measurement cycle, the first $\overline{\text{STROBE}}$ occurs for one half clock pulse. After the D₅ digit strobe, D₄ goes high for 200 clock pulses. The $\overline{\text{STROBE}}$ then goes low 100 clock pulses after D₄ goes high. This continues through the D₁ digit drive pulse.

The digit drive signals will continue to permit display scanning. $\overline{\text{STROBE}}$ pulses are not repeated until a new measurement is completed. The digit drive signals will not continue if the previous signal resulted in an overrange condition.

The active low $\overline{\text{STROBE}}$ pulses aid BCD data transfer to UARTs, processors and external latches. For more information, please refer to Application Note 784.

FIGURE 5-3: STROBE SIGNAL LOW FIVE TIMES PER CONVERSION



5.3 BUSY Output

At the beginning of the signal integration phase, BUSY goes high and remains high until the first clock pulse after the integrator zero crossing. BUSY returns to the logic "0" state after the measurement cycle ends in an overrange condition. The internal display latches are loaded during the first clock pulse after BUSY and are latched at the clock pulse end. The BUSY signal does not go high at the beginning of the measurement cycle, which starts with the auto zero cycle.

5.4 OVERRANGE Output

If the input signal causes the reference voltage integration time to exceed 20,000 clock pulses, the OVERRANGE output is set to a logic "1." The overrange output register is set when BUSY goes low and is reset at the beginning of the next reference integration phase.

5.5 UNDERRANGE Output

If the output count is 9% of full scale or less (-1800 counts), the underrange register bit is set at the end of BUSY. The bit is set low at the next signal integration phase.

5.6 POLARITY Output

A positive input is registered by a logic "1" polarity signal. The polarity bit is valid at the beginning of reference integrate and remains valid until determined during the next conversion.

The polarity bit is valid even for a zero reading. Signals less than the converter's LSB will have the signal polarity determined correctly. This is useful in null applications.

5.7 Digit Drive Outputs

Digit drive signals are positive-going signals. The scan sequence is D_5 to D_1 . All positive pulses are 200 clock pulses wide, with the exception D_5 , which is 201 clock pulses wide.

All five digits are scanned continuously, unless an overrange condition occurs. In an overrange condition, all digit drives are held low from the final STROBE pulse until the beginning of the next reference integrate phase. The scanning sequence is then repeated. This provides a blinking visual display indication.

5.8 BCD Data Outputs

The binary coded decimal (BCD) bits B_8 , B_4 , B_2 , and B_1 are positive-true logic signals. The data bits become active at the same time as the digit drive signals. In an overrange condition, all data bits are at a logic "0" state.

6.0 TYPICAL APPLICATIONS

6.1 Component Value Selection

6.1.1 INTEGRATING RESISTOR

The integrating resistor R_{INT} is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor, C_{INT} . Both the buffer amplifier and the integrator have a class A output stage, with 100 μ A of quiescent current. A 20 μ A drive current gives negligible linearity errors. Values of 5 μ A to 40 μ A give good results. The exact value of an integrating resistor for a 20 μ A current is easily calculated.

EQUATION 6-1:

$$R_{INT} = \frac{\text{Full scale voltage}}{20\mu\text{A}}$$

6.1.2 INTEGRATING CAPACITOR (C_{INT})

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing that ensures the tolerance buildup will not saturate the integrator swing (approximately 0.3V from either supply). For ± 5 V supplies and ANALOG COMMON tied to supply ground, a ± 3.5 V to ± 4 V full scale integrator swing is adequate. A 0.10 μ F to 0.47 μ F is recommended. In general, the value of C_{INT} is given by:

EQUATION 6-2:

$$C_{INT} = \frac{[10,000 \times \text{clock period}] \times I_{INT}}{\text{Integrator output voltage swing}}$$

$$= \frac{(10,000) (\text{clock period}) (20\mu\text{A})}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor C_{INT} is that it has low dielectric absorption to prevent rollover or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half scale 0.9999, with any deviation probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

6.1.3 AUTO ZERO AND REFERENCE CAPACITORS

The size of the auto zero capacitor has some influence on the noise of the system. A large capacitor reduces the noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference and auto zero capacitors are only important at power-on or when the circuit is recovering from an overload. Smaller or cheaper capacitors can be used if accurate readings are not required for the first few seconds of recovery.

6.1.4 REFERENCE VOLTAGE

The analog input required to generate a full scale output is $V_{IN} = 2 V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high-quality reference be used where high-accuracy absolute measurements are being made.

6.2 Conversion Timing

6.2.1 LINE FREQUENCY REJECTION

A signal integration period at a multiple of the 60Hz line frequency will maximize 60Hz "line noise" rejection. A 100kHz clock frequency will reject 50Hz, 60Hz and 400Hz noise. This corresponds to five readings per second (see Table 6-1 and Table 6-2).

TABLE 6-1: CONVERSION RATE VS. CLOCK FREQUENCY

Oscillator Frequency (kHz)	Conversion Rate (Conv./Sec.)
100	2.5
120	3
200	5
300	7.5
400	10
800	20
1200	30

TABLE 6-2: LINE FREQUENCY REJECTION VS. CLOCK FREQUENCY

Oscillator Frequency (kHz)	Line Frequency Rejection (Hz)
300	60
200	
150	
120	
100	
40	
33-1/3	50
250	
166-2/3	
125	
100	50, 60,400
100	

The conversion rate is easily calculated:

EQUATION 6-3:

$$\text{Reading 1/sec} = \frac{\text{Clock Frequency (Hz)}}{4000}$$

6.3 High Speed Operation

The maximum conversion rate of most dual slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3µsec delay, at a clock frequency of 160 kHz (6µsec period), Half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50µV input, 1 to 2 with 150µV, 2 to 3 at 250µV, etc. This transition at midpoint is considered desirable by most users. However, if the clock frequency is increased appreciably above 200kHz, the instrument will flash "1" on noise peaks, even when the input is shorted.

For many dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the nonlinearity and noise do not increase substantially with frequency, clock rates of up to ~1MHz may be used. For a fixed clock frequency, the extra count, or counts, caused by comparator delay, will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 160kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the compar-

ator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second-order breaks will cause significant nonlinearities in the first few counts of the instrument.

The minimum clock frequency is established by leakage on the auto zero and reference capacitors. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in Section 6.0, Typical Applications. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

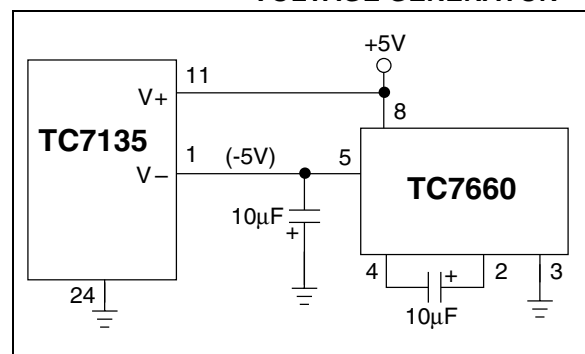
6.4 Zero Crossing Flip Flop

The flip flop interrogates the data once every clock pulse and half after the transients of the previous clock pulse and half clock pulse have died down. False zero crossings caused by clock pulses are not recognized. Of course, the flip flop delays the true zero crossing by up to one count in every instance. If a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of the reference integrate (de-integrate) phase. This one-count delay compensates for the delay of the zero crossing flip flop and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of auto zero gives an overload display of 0000 instead of 0001. No delay occurs during signal integrate so that true ratiometric readings result.

6.5 Generating a Negative Supply

A negative voltage can be generated from the positive supply by using a TC7660 (see Figure 6-1).

FIGURE 6-1: NEGATIVE SUPPLY VOLTAGE GENERATOR



TC7135

FIGURE 6-2: 4-1/2 DIGIT ADC WITH MULTIPLEXED COMMON ANODE LED DISPLAY

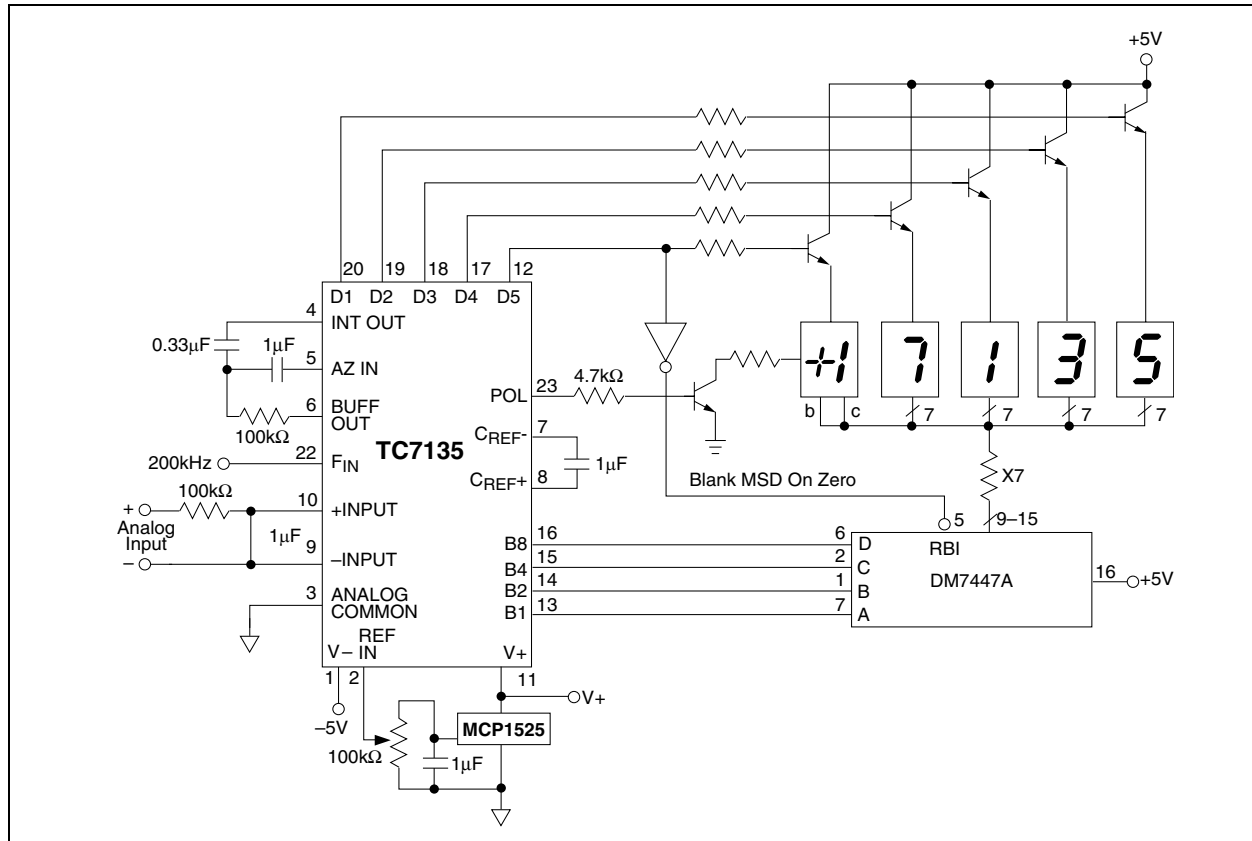


FIGURE 6-3: RC OSCILLATOR CIRCUIT

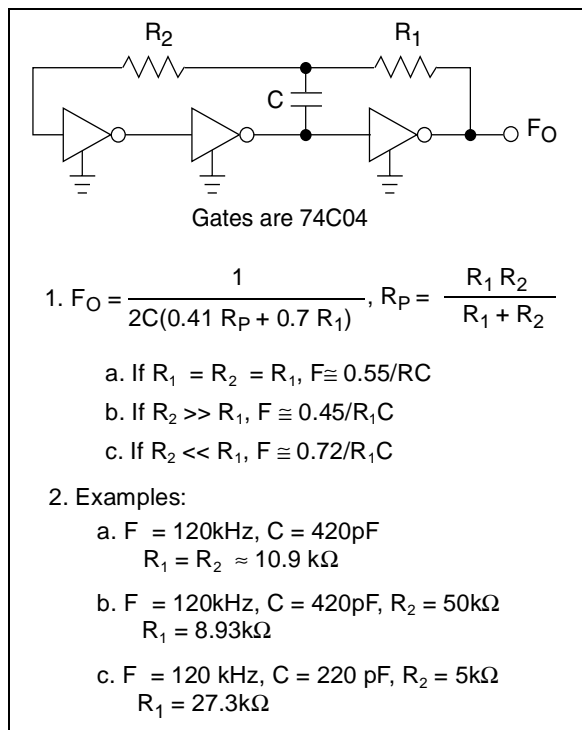


FIGURE 6-4: COMPARATOR CLOCK CIRCUITS

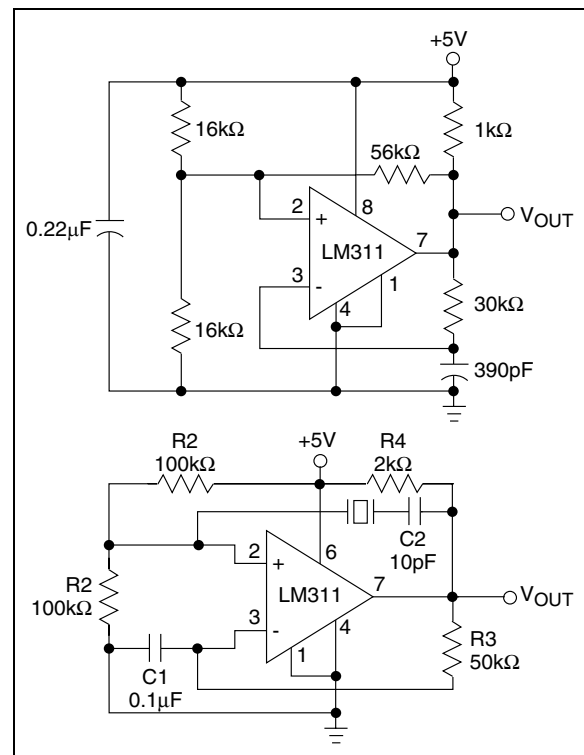
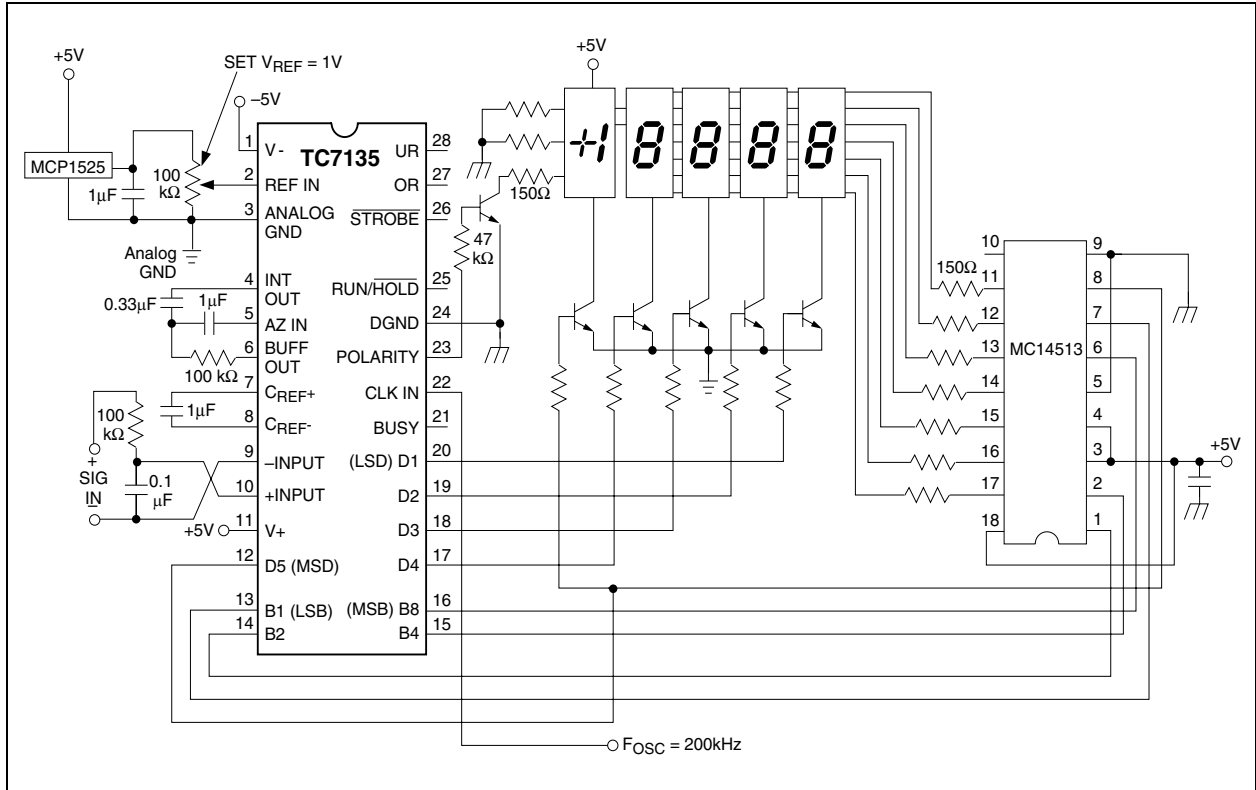


FIGURE 6-5: 4-1/2 DIGIT ADC WITH MULTIPLEXED COMMON CATHODE LED DISPLAY



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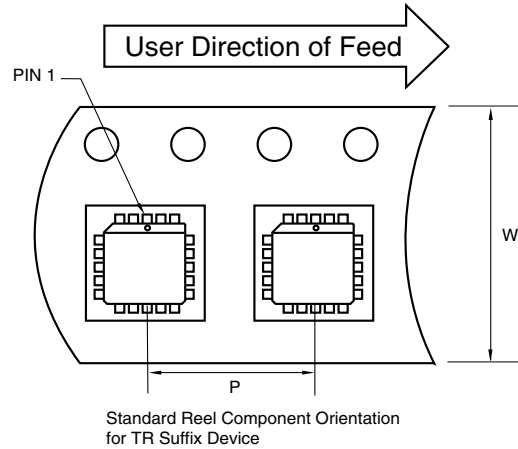
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

Package marking data not available at this time.

7.2 Taping Forms

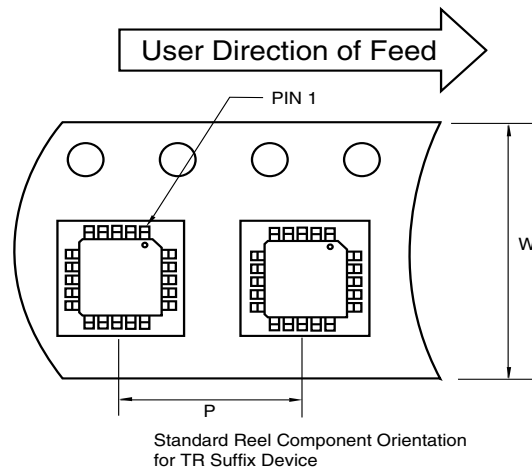
Component Taping Orientation for 28-Pin PLCC Devices



Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
28-Pin PLCC	24 mm	16 mm	750	13 in

Component Taping Orientation for 64-Pin PQFP Devices

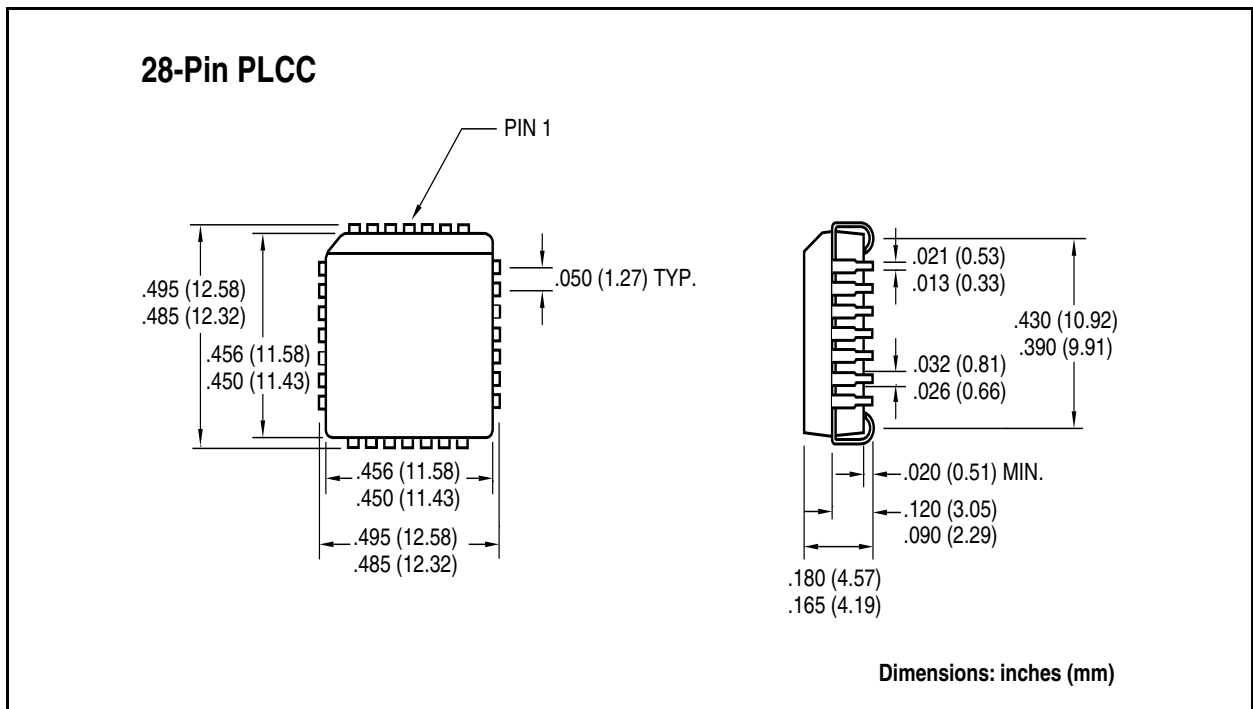
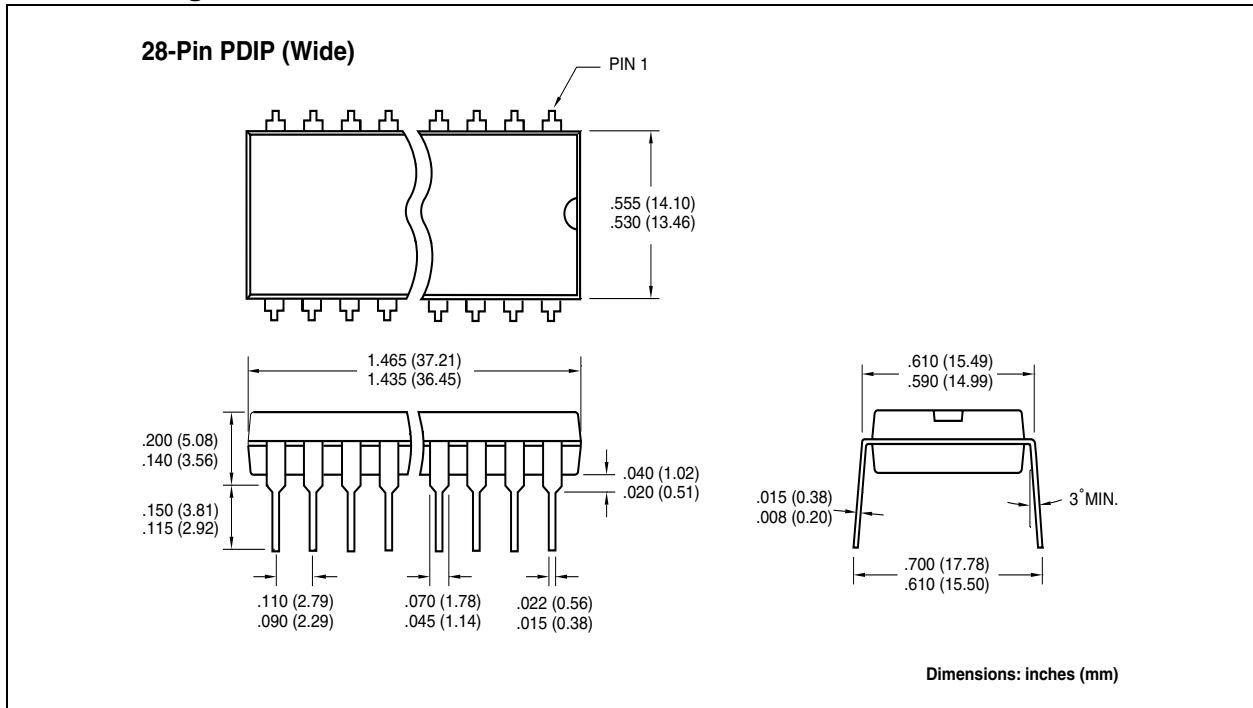


Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
64-Pin PQFP	32 mm	24 mm	250	13 in

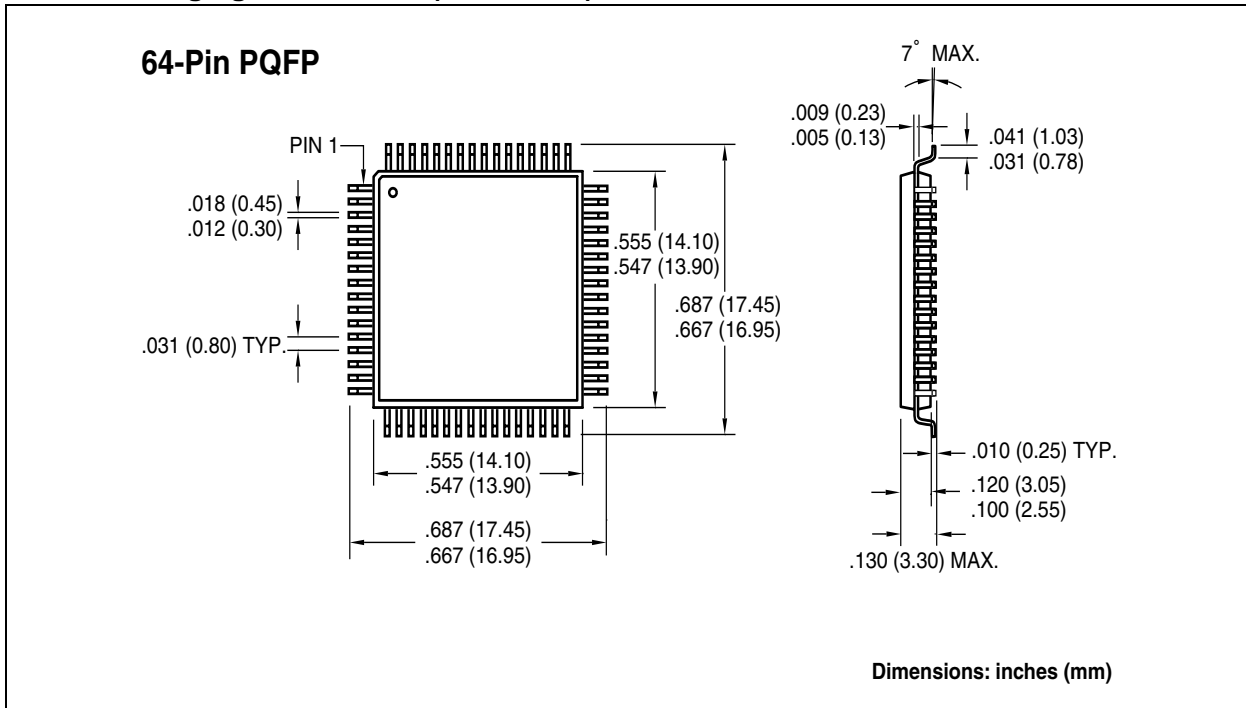
NOTE: Drawing does not represent total number of pins.

7.3 Package Dimensions



TC7135

7.3 Packaging Dimensions (Continued)



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New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

China - Hong Kong SAR

Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Nordic ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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