

Quad D latch

BU4042B

The BU4042B is a four-circuit D latch with a common clock line and separate data input terminals.

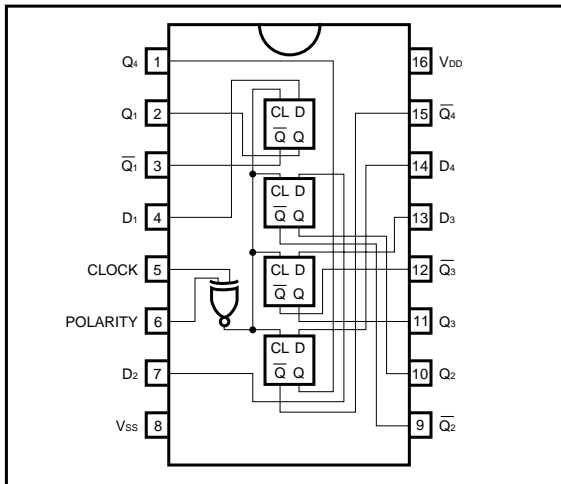
When the polarity input is set to "H", input (D) is presented to output (Q) as is, as long as the clock input is rising, and when the clock input falls, output (Q) holds input (D) at that point. While the clock input is falling, output (Q) does not change even if input (D) changes.

Also, if the polarity input is set to "L", input (D) is presented to output (Q) as is, as long as the clock input is at "L" level, and when the clock input goes to "H" level, latching takes place.

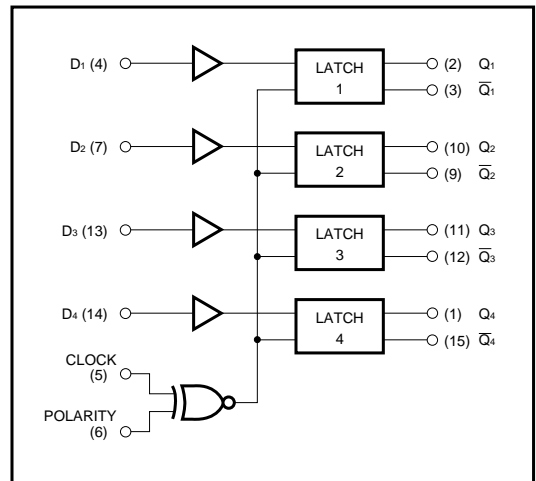
●Features

- 1) Low power dissipation.
- 2) Wide range of operating power supply voltages.
- 3) High input impedance.
- 4) High fan-out.
- 5) Direct drive of 2 L-TTL inputs and 1LS-TTL input.

●Block diagram



●Logic circuit diagram



●Truth table

CLOCK	POLARITY	Q
L	L	D
H	L	LATCH
H	H	D
L	H	LATCH

● Absolute maximum ratings ($T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	$-0.3 \sim +18$	V
Power dissipation	P_d	1000 (DIP)	mW
Operating temperature	T_{opr}	$-40 \sim +85$	$^\circ\text{C}$
Storage temperature	T_{stg}	$-55 \sim +150$	$^\circ\text{C}$
Input voltage	V_{IN}	$-0.3 \sim V_{DD} + 0.3$	V

● Electrical characteristics

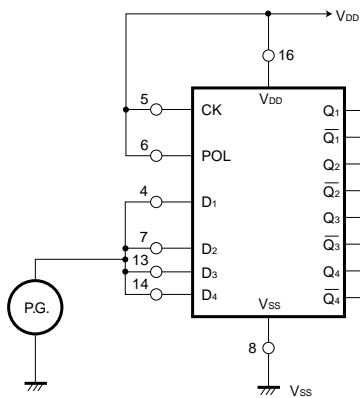
DC characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V _{DD} (V)	Conditions
Input high level voltage (DATA)	V_{IH}	3.5	—	—	V	5	—
		7.0	—	—		10	
		11.0	—	—		15	
Input high level voltage (CLOCK POLARITY)	V_{IH}	3.5	—	—	V	5	—
		7.0	—	—		10	
		11.25	—	—		15	
Input low level voltage (DATA)	V_{IL}	—	—	1.5	V	5	—
		—	—	3.0		10	
		—	—	4.0		15	
Input low level voltage (CLOCK POLARITY)	V_{IL}	—	—	1.5	V	5	—
		—	—	3.0		10	
		—	—	3.75		15	
Input high level current	I_{IH}	—	—	0.3	μA	15	$V_{IH} = 15\text{V}$
Input low level current	I_{IL}	—	—	-0.3	μA	15	$V_{IL} = 0\text{V}$
Output high level voltage	V_{OH}	4.95	—	—	V	5	$I_o = 0\text{mA}$
		9.95	—	—		10	
		14.95	—	—		15	
Output low level voltage	V_{OL}	—	—	0.05	V	5	$I_o = 0\text{mA}$
		—	—	0.05		10	
		—	—	0.05		15	
Output high level current	I_{OH}	-0.16	—	—	mA	5	$V_{OH} = 4.6\text{V}$
		-0.4	—	—		10	$V_{OH} = 9.5\text{V}$
		-1.2	—	—		15	$V_{OH} = 13.5\text{V}$
Output low level current	I_{OL}	0.44	—	—	mA	5	$V_{OL} = 0.4\text{V}$
		1.1	—	—		10	$V_{OL} = 0.5\text{V}$
		3.0	—	—		15	$V_{OL} = 1.5\text{V}$
Static current dissipation	I_{DD}	—	—	4.0	μA	5	$V_i = V_{DD}$ or GND
		—	—	8.0		10	
		—	—	16.0		15	

Switching characteristics (unless otherwise noted, Ta = 25°C, CL = 50pF, VSS = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	VDD (V)	Conditions	Measurement circuit
						5		
Output rise time	t _{TLH}	—	180	—	ns	5	—	Fig.1
		—	90	—		10		
		—	65	—		15		
Output fall time	t _{THL}	—	100	—	ns	5	—	Fig.1
		—	50	—		10		
		—	40	—		15		
Propagation delay time D→Q, Q̄	t _{PLH} t _{PHL}	—	220	—	ns	5	—	Fig.1
		—	90	—		10		
		—	70	—		15		
Propagation delay time CLOCK→Q, Q̄	t _{PLH} t _{PHL}	—	220	—	ns	5	—	Fig.2
		—	90	—		10		
		—	70	—		15		
Minimum clock pulse width	t _{WH} t _{WL}	—	150	—	ns	5	—	Fig.2
		—	50	—		10		
		—	40	—		15		
Hold time	t _H	—	50	—	ns	5	—	Fig.2
		—	25	—		10		
		—	20	—		15		
Setup time	t _{SU}	—	50	—	ns	5	—	Fig.2
		—	20	—		10		
		—	5	—		15		
Input capacitance	C _{IN}	—	5	—	pF	—	—	—

●Measurement circuits



Note: Connect CL = 50pF to each of the output pins.

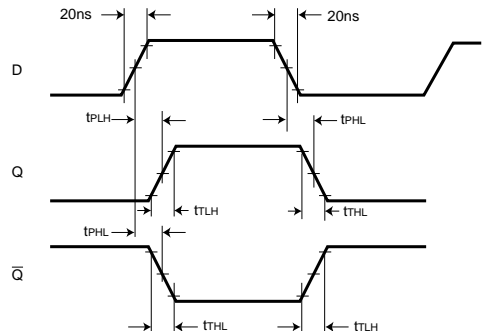
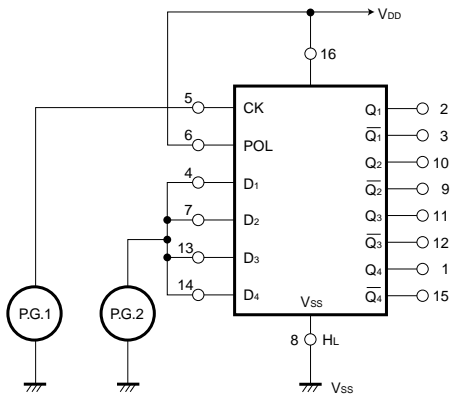


Fig. 1 (a) Switching characteristics measurement circuit I

Fig. 1 (b) Switching time measurement waveform I



Note : Connect $C_L = 50\text{pF}$ to each of the output pins.

Fig. 2 (a) Switching characteristics measurement circuit II

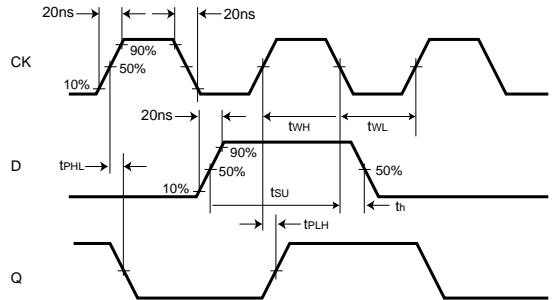


Fig. 2 (b) Switching time measurement waveform II

●Electrical characteristic curve

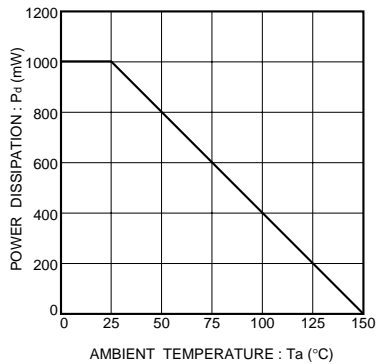
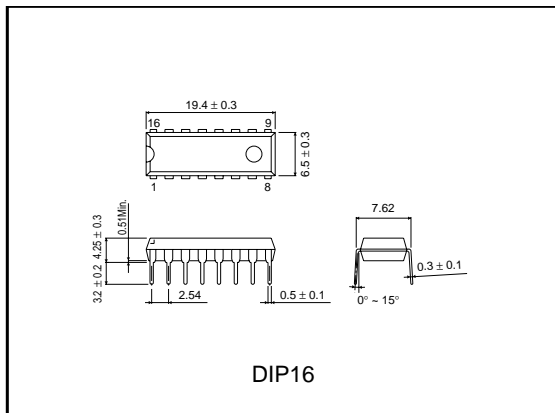


Fig.3 Power dissipation vs. Ta

●External dimensions (Units: mm)



DIP16