SONY

CXD3009Q

CD Digital Signal Processor

Description

The CXD3009Q is a digital signal processor LSI for CD players and is equipped with built-in digital filters, zero detection circuit, 1-bit DAC, and analog low-pass filter on a single chip.

Features

Digital Signal Processor (DSP) Block

- Playback mode supporting CAV (Constant Angular Velocity)
  - – Frame jitter-free
  - – Allows 0.5 to double-speed continuous playback
  - – Allows relative rotational velocity readout
  - – Supports external spindle control
- Wide capture range playback mode
  - – Spindle rotational velocity following method
  - – Supports normal-speed and double-speed playback
- 16K RAM
- EFM data demodulation
- Enhanced EFM frame sync protection
- SEC strategy-based error correction
- Subcode demodulation and Sub Q data error detection
- Digital spindle servo
- 16-bit traverse counter
- Asymmetry compensation circuit
- Serial bus-based CPU interface
- Error correction monitor signals, etc. are output from a new CPU interface.
- Servo auto sequencer
- Digital audio interface output
- Digital peak meter
- CD-TEXT data demodulation

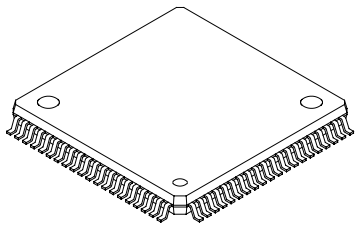
Digital Filter, DAC, Analog Low-Pass Filter Block

- DBB (Digital Bass Boost)
- Supports double-speed playback
- Digital de-emphasis
- Digital attenuation function
- Zero detection function
- 8Fs oversampling digital filter

Applications

CD players

80 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

• Supply voltage	V_{DD}	–0.3 to +4.6	V
• Input voltage	V_I	–0.3 to +4.6	V
		(Vss – 0.3V to V_{DD} + 0.3V)	
• Output voltage	V_O	–0.3 to +4.6	V
• Storage temperature	Tstg	–40 to +125	°C
• Supply voltage difference			
	V_{SS} – AV_{SS}	–0.3 to +0.3	V
	V_{DD} – AV_{DD}	–0.3 to +0.3	V

Note) AV_{DD} includes XV_{DD}, and AV_{SS} includes XV_{SS}.

Recommended Operating Conditions

• Supply voltage	V_{DD}	2.5 to 3.6	V
• Operating temperature	Topr	–20 to +75	°C

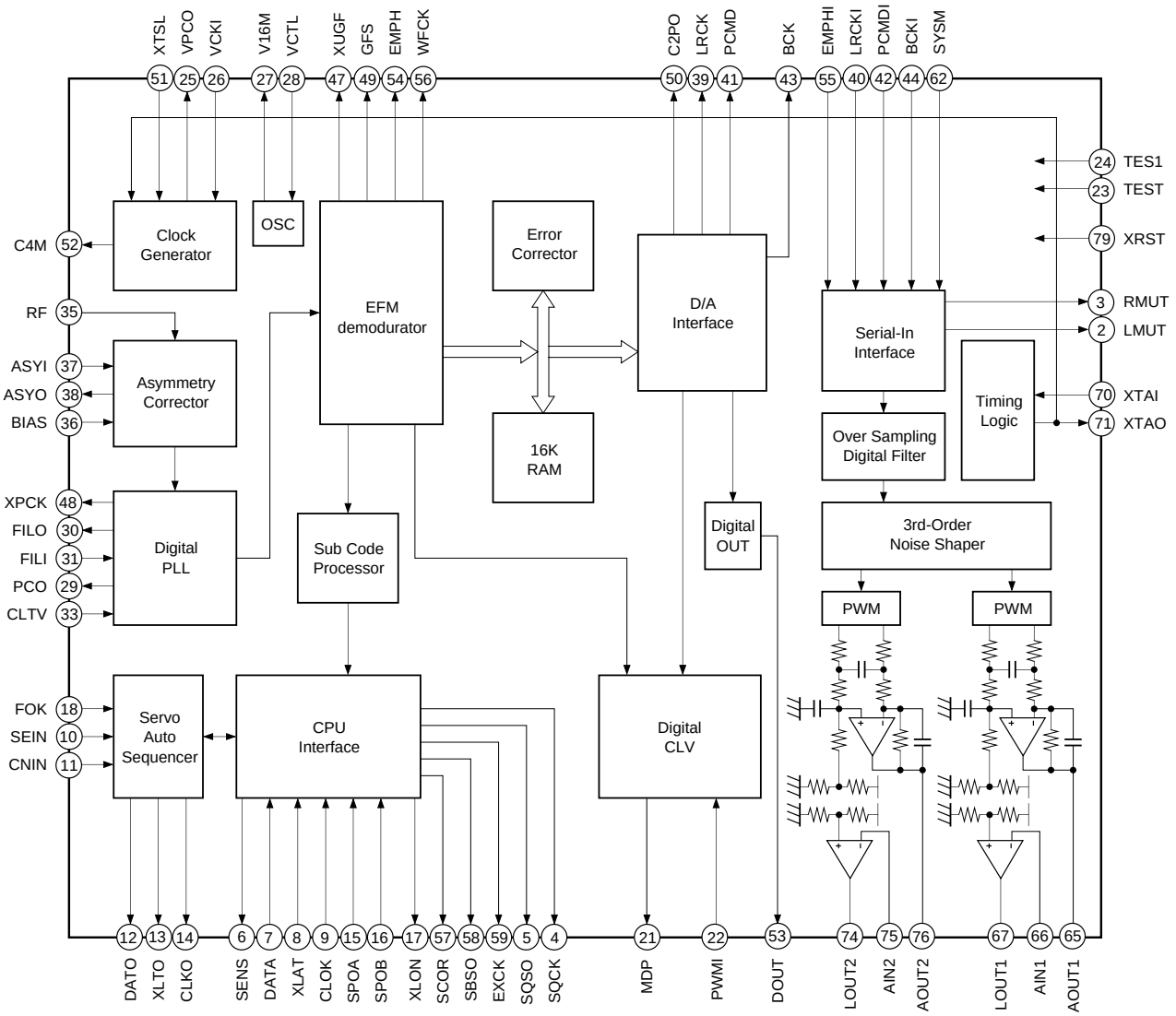
Input/Output Capacitances

• Input capacitance	C_I	12 (max.)	pF
• Output capacitance	C_O	12 (max.)	pF

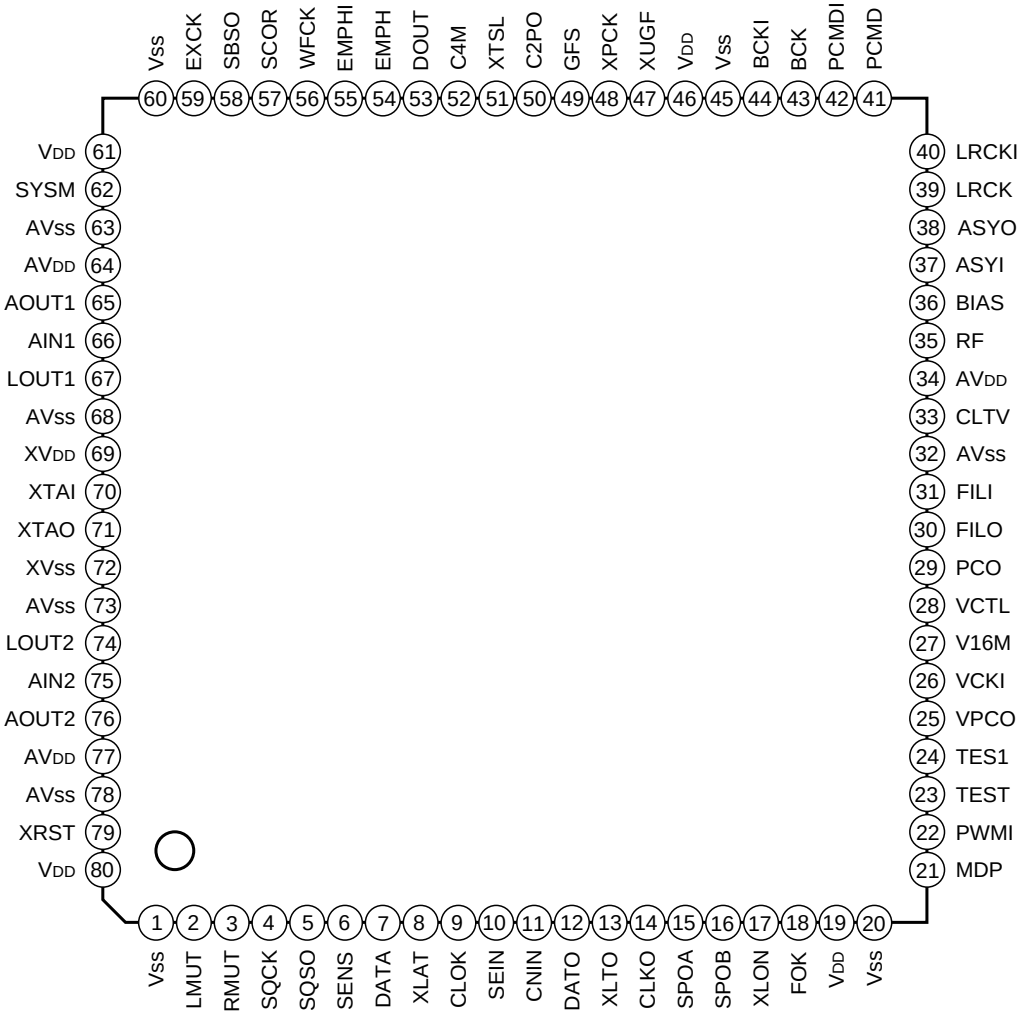
Note) Measurement conditions $V_{DD} = V_I = 0V$
f_M = 1MHz

E97322C11

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O		Description
1	V_{SS}	—	—	GND
2	LMUT	O	1, 0	Left-channel zero detection flag.
3	RMUT	O	1, 0	Right-channel zero detection flag.
4	SQCK	I		SQSO readout clock input.
5	SQSO	O	1, 0	Sub Q 80-bit serial output.
6	SENS	O	1, 0	SENS output to CPU.
7	DATA	I		Serial data input from CPU.
8	XLAT	I		Latch input from CPU. Serial data is latched at the falling edge.
9	CLOK	I		Serial data transfer clock input from CPU.
10	SEIN	I		SENS input from SSP.
11	CNIN	I		Track jump count signal input.
12	DATO	O	1, 0	Serial data output to SSP.
13	XLTO	O	1, 0	Serial data latch output to SSP. Latched at the falling edge.
14	CLKO	O	1, 0	Serial data transfer clock output to SSP.
15	SPOA	I		Microcomputer extended interface (input A).
16	SPOB	I		Microcomputer extended interface (input B).
17	XLON	O	1, 0	Microcomputer extended interface (output).
18	FOK	I		Focus OK input. Used for SENS output and the servo auto sequencer.
19	V_{DD}	—	—	Power supply (+3V).
20	V_{SS}	—	—	GND
21	MDP	O	1, Z, 0	Spindle motor servo control.
22	PWMI	I		Spindle motor external control input.
23	TEST	I		TEST pin; normally GND.
24	TES1	I		TEST pin; normally GND.
25	VPCO	O	1, Z, 0	Charge pump output for the wide-band EFM PLL.
26	VCKI	I		VCO2 oscillation input for the wide-band EFM PLL.
27	V16M	O	1, 0	VCO2 oscillation output for the wide-band EFM PLL.
28	VCTL	I		VCO2 control voltage input for the wide-band EFM PLL.
29	PCO	O	1, Z, 0	Master PLL charge pump output.
30	FILO	O	Analog	Master PLL (slave = digital PLL) filter output.
31	FILI	I		Master PLL filter input.
32	AV_{SS}	—	—	Analog GND.
33	CLTV	I		Master VCO control voltage input.
34	AV_{DD}	—	—	Analog power supply (+3V).
35	RF	I		EFM signal input.

Pin No.	Symbol	I/O		Description
36	BIAS	I		Constant current input of the asymmetry circuit.
37	ASYI	I		Asymmetry comparator voltage input.
38	ASYO	O	1, 0	EFM full-swing output (low = V_{SS}, high = V_{DD}).
39	LRCK	O	1, 0	D/A interface. LR clock output f = Fs.
40	LRCKI	I		LR clock input.
41	PCMD	O	1, 0	D/A interface. Serial data output (two's complement, MSB first).
42	PCMDI	I		D/A interface. Serial data input (two's complement, MSB first).
43	BCK	O	1, 0	D/A interface. Bit clock output.
44	BCKI	I		D/A interface. Bit clock input.
45	V_{SS}	—	—	GND
46	V_{DD}	—	—	Power supply (+3V).
47	XUGF	O	1, 0	XUGF output. Switched to MNT1 or RFCK output by a command.
48	XPCK	O	1, 0	XPLCK output. Switched to MNT0 output by a command.
49	GFS	O	1, 0	GFS output. Switched to MNT3 or XRAOF output by a command.
50	C2PO	O	1, 0	C2PO output. Switched to GTOP output by a command.
51	XTSL	I		Crystal selector input. Low: 16.9344MHz; high: 33.8688MHz.
52	C4M	O	1, 0	4.2336MHz output. 1/4 frequency-divided VCKI output in CAV-W mode.
53	DOUT	O	1, 0	Digital Out output.
54	EMPH	O	1, 0	Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis.
55	EMPHI	I		Inputs a high signal when de-emphasis is on, and a low signal when de-emphasis is off.
56	WFCK	O	1, 0	WFCK output.
57	SCOR	O	1, 0	Outputs a high signal when either subcode sync S0 or S1 is detected.
58	SBSO	O	1, 0	Sub P to W serial output.
59	EXCK	I		SBSO readout clock input.
60	V_{SS}	—	—	GND
61	V_{DD}	—	—	Power supply (+3V).
62	SYSM	I		Mute input. Active when high.
63	AV_{SS}	—	—	Analog GND.
64	AV_{DD}	—	—	Analog power supply (+3V).
65	AOUT1	O		Left-channel analog output.
66	AIN1	I		Left-channel operational amplifier input.
67	LOUT1	O		Left-channel LINE output.
68	AV_{SS}	—	—	Analog GND.
69	XV_{DD}			Power supply for master clock.
70	XTAI	I		Crystal oscillation circuit input. Input the external master clock via this pin.
71	XTAO	O		Crystal oscillation circuit output.

Pin No.	Symbol	I/O		Description
72	XV_{SS}			GND for master clock.
73	AV_{SS}	—	—	Analog GND.
74	LOUT2	O		Right-channel LINE output.
75	AIN2	I		Right-channel operational amplifier input.
76	AOUT2	O		Right-channel analog output.
77	AV_{DD}	—	—	Analog power supply (+3V).
78	AV_{SS}	—	—	Analog GND.
79	XRST	I		System reset. Reset when low.
80	V_{DD}	—	—	Power supply (+3V).

Notes)
- PCMD is an MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window open.)
- XUGF is the frame sync obtained from the EFM signal, and a negative pulse. It is the signal before sync protection.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge of XPLCK and the EFM signal transition point coincide.
- GFS goes high when the frame sync and the insertion protection timing match.
- RFCK is derived with the crystal accuracy. This signal has a cycle of 136µs (during normal speed).
- C2PO represents the data error status.
- XRAOF is generated when the 16K RAM exceeds the ±4F jitter margin.

Electrical Characteristics

DC Characteristics (V_{DD} = AV_{DD} = 3.3V ± 5%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C) *

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1
	Low level input voltage	V_{IL} (1)				0.2V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)	Schmitt input	0.7V_{DD}			V	*2
	Low level input voltage	V_{IL} (2)				0.2V_{DD}	V	
Input voltage (3)	Input voltage	V_{IN} (3)	Analog input	Vss		V_{DD}	V	*3
Output voltage (1)	High level output voltage	V_{OH} (1)	I_{OH} = –4mA	V_{DD} – 0.4		V_{DD}	V	*4
	Low level output voltage	V_{OL} (1)	I_{OL} = 4mA	0		0.4	V	
Output voltage (2)	High level output voltage	V_{OH} (2)	I_{OH} = –2mA	V_{DD} – 0.4		V_{DD}	V	*5
	Low level output voltage	V_{OL} (2)	I_{OL} = 4mA	0		0.4	V	
Output voltage (4)	High level output voltage	V_{OH} (4)	I_{OH} = –0.28mA	V_{DD} – 0.4		V_{DD}	V	*6
	Low level output voltage	V_{OL} (4)	I_{OL} = 0.36mA	0		0.4	V	
Input leak current		I_{LI}	V_I = 0 to 3.60V	–5		5	µA	*1, *2, *3
Tri-state pin output leak current		I_{LO}	V_O = 0 to 3.60V	–5		5	µA	*7

Applicable pins

*1 XTSL, DATA, XLAT, PWMI, SYSM, EMPHI, PCMDI

*2 CLOK, XRST, EXCK, SQCK, FOK, SEIN, CNIN, VCKI, LRCKI, BCKI, SPOA, SPOB

*3 CLTV, FILI, RF, VCTL, AIN1, AIN2

*4 MDP, PCO, VPCO

*5 ASYO, DOUT, C4M, SBSO, SQSO, SCOR, EMPH, DATO, CLKO, XLTO, SENS, WFCK, V16M, LMUT, RMUT, XLON, LRCK, PCMD, BCK, XUGF, XPCK, GFS, RFCK, C2PO

*6 FILO

*7 SENS, PCO, VPCO

*note) : XV_{DD} and XV_{SS} are included for AV_{PP} and AV_{SS}, respectively.
Those are the same for the explanation from the next page.

AC Characteristics

1. XTAI pin

(1) When using self-excited oscillation

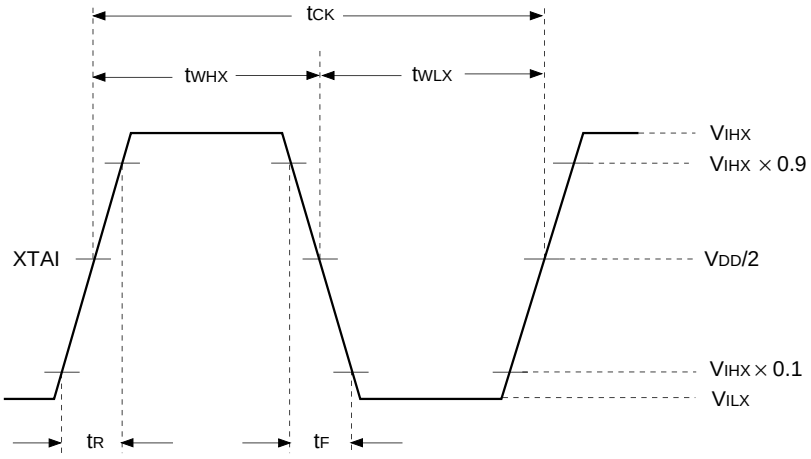
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.3V ± 5%)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7		34	MHz

(2) When inputting pulses to XTAI pin

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.3V ± 5%)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	13		500	ns
Low level pulse width	t_{WLX}	13		500	ns
Pulse cycle	t_{CK}	26		1,000	ns
Input high level	V_{IHX}	0.7V_{DD}			V
Input low level	V_{ILX}			0.2V_{DD}	V
Rise time, fall time	t_R, t_F			10	ns



(3) When inputting sine waves to XTAI pin via a capacitor

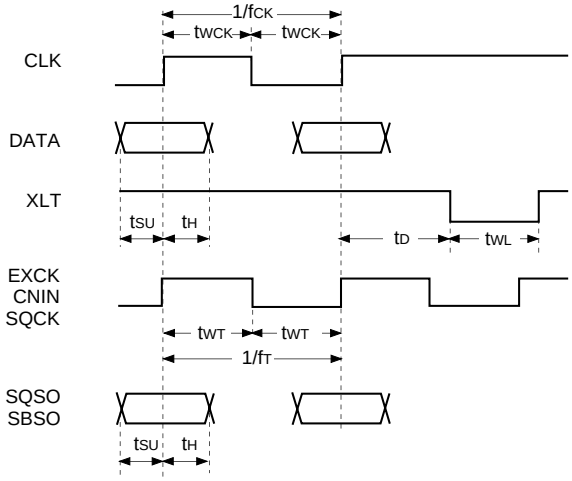
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.3V ± 5%)

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_1	0.5V_{DD}		V_{DD} + 0.3	Vp-p

2. CLOK, DATA, XLAT, CNIN, SQCK and EXCK pins

(V_{DD} = AV_{DD} = 3.3V ± 5%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

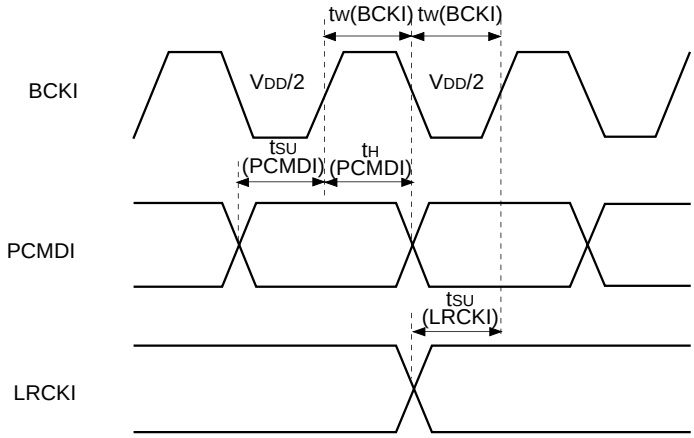
Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK SQCK frequency	f_T			0.65*	MHz
EXCK SQCK pulse width	f_{WT}	750*			ns



* In pseudo double-speed playback mode, except when SQSO is Sub Q Read, the maximum operating frequency for SQCK is 300kHz and the minimum pulse width is 1.5µs.

3. BCKI, LRCKI and PCMDI pins (V_{DD} = AV_{DD} = 3.3V ± 5%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
BCK pulse width	t_W		94			ns
DATAL, R setup time	t_{SU}		18			ns
DATAL, R hold time	t_H		18			ns
LRCK setup time	t_{SU}		18			ns



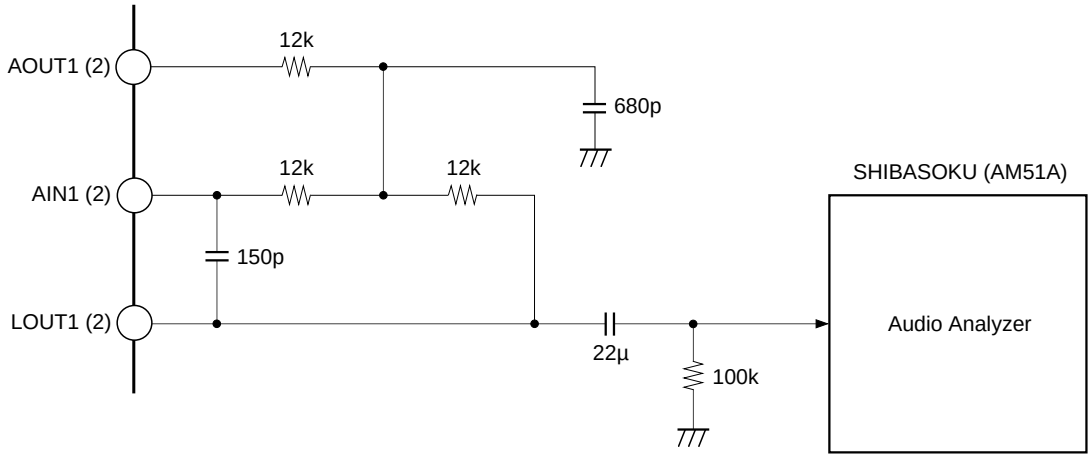
1-bit DAC, LPF Block Analog Characteristics

Analog Characteristics (V_{DD} = AV_{DD} = 3.3V, V_{SS} = AV_{SS} = 0V, Ta = 25°C)

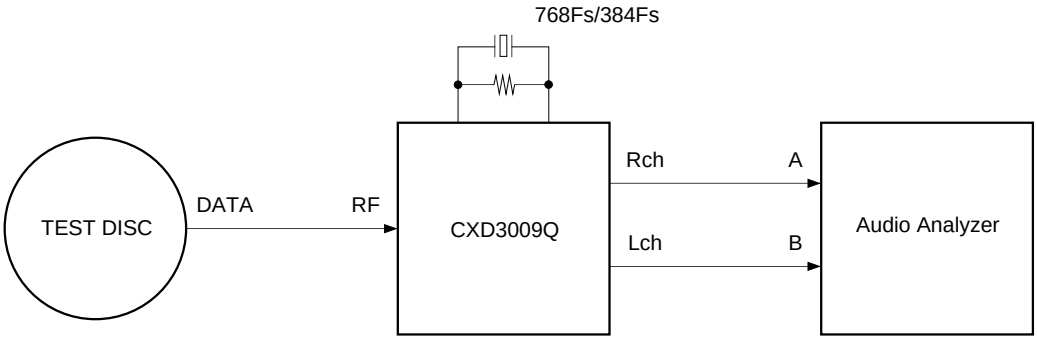
Item	Symbol	Conditions	Crystal	Min.	Typ.	Max.	Unit
Total harmonic distortion	THD	1kHz, 0dB data	384Fs		0.015	0.025	%
			768Fs		0.015	0.025	
S/N ratio	S/N	1kHz, 0dB data (using A-weighting filter)	384Fs	90	94		dB
			768Fs	90	94		

For both items, Fs = 44.1kHz.

The total harmonic distortion and S/N ratio measurement circuits are shown below.



LPF External Circuit Diagram



Block Diagram for Measuring Analog Characteristics

(V_{DD} = AV_{DD} = 3.3V, V_{SS} = AV_{SS} = 0V, Topr = – 20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Applicable pins
Output voltage	V_{OUT}		0.70*		Vrms	*1
Load resistance	R_L	20			kΩ	*1

* Measured using the circuits on the previous page when a sine wave of 1kHz and 0dB is output.

Applicable pins

*1 LOUT1, LOUT2

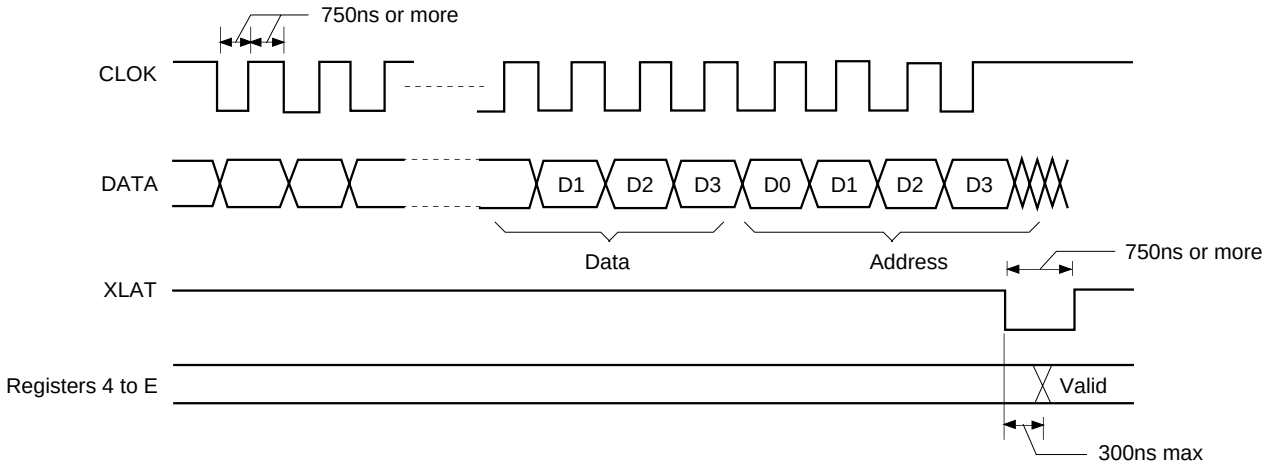
Description of Functions

1. CPU Interface and Commands

• CPU Interface

This interface uses DATA, CLOK and XLAT to set the modes.

The interface timing chart is shown below.



• Information on each address and the data is provided in Table 1-1.

• The internal registers are initialized by a reset when XRST is low; the initialization data is shown in Table 1-2.

Note) When XLAT is low, SQCK must be set high.

Command Table

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4				Data 5				Data 6			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind (A, E), Overflow (C)	0	1	0	1	0.18ms	0.09ms	0.05ms	0.02ms	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Brake (B)					0.36ms	0.18ms	0.09ms	0.05ms																				
6	Kick (D)	0	1	1	0	11.6ms	5.8ms	2.9ms	1.45ms	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequence (N) track jump count	0	1	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	—	—	—	—	—	—	—	—
8	MODE specification	1	0	0	0	CDROM	DOUT Mute	DOUT ON/OFF	WSEL	VCO SEL1	0	SOCT	VCO SEL2	KSL3	KSL2	KSL1	KSL0	0	0	VCO2 THRU	0	0	0	0	0	TXON	TXOUT	OUTL1	OUTL0
9	Function specification	1	0	0	1	0	DSPB ON/OFF	0	0	0	0	0	SYCOF	OPSL10	MCSL	0	0	ZDPL	ZMUT	—	—	—	—	—	—	—	—	—	—
		1	0	0	1	0	DSPB ON/OFF	0	0	0	0	0	SYCOF	OPSL11	MCSL	0	0	ZDPL	ZMUT	0	0	0	DCOF	0	0	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	Mute	ATT	0	0	OPSL20	EMPH	SMUT	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—
		1	0	1	0	0	0	Mute	ATT	0	0	OPSL21	EMPH	SMUT	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FMUT	LRWO	BSBST	BBSL
B	Serial bus CTRL	1	0	1	1	SL1	SL0	CPUSR	0	TRMI	TRMO	MTSL1	MTSL0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
C	Servo coefficient setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	0	TB	TP	Gain CLVS	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON	Gain CAV1	Gain CAV0	0	0	—	—	—	—	—	—	—	—

Table 1-1

Reset Initialization

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4				Data 5				Data 6			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind (A, E), Overflow (C) / Brake (B)	0	1	0	1	0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	Kick (D)	0	1	1	0	0	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequence (N) track jump count setting	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
8	MODE specification	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
9	Function specification	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B	Serial bus CTRL	1	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
C	Servo coefficient setting	1	1	0	0	0	1	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	0	0	0	0	1	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—

Table 1-2

1-1. The meaning of the data for each address is explained below.

$4X commands

Command	AS3	AS2	AS1	AS0
CANCEL	0	0	0	0
FOCUS-ON	0	1	1	1
1 TRACK JUMP	1	0	0	RXF
10 TRACK JUMP	1	0	1	RXF
2N TRACK JUMP	1	1	0	RXF
N TRACK MOVE	1	1	1	RXF

RXF = 0 FORWARD
RXF = 1 REVERSE

- When the Focus-on command ($47) is canceled, $02 is sent and the auto sequence is interrupted.
- When the Track jump/move commands ($48 to $4F) are canceled, $25 is sent and the auto sequence is interrupted.

$5X commands

Auto sequence timer setting
Setting timers: A, E, C, B

Command	D3	D2	D1	D0
Blind (A, E), Over flow (C)	0.18ms	0.09ms	0.05ms	0.02ms
Brake (B)	0.36ms	0.18ms	0.09ms	0.05ms

Ex.) D2 = D0 = 1, D3 = D1 = 0 (Initial Reset)
A = E = C = 0.11ms
B = 0.23ms

$6X commands

Auto sequence timer setting
Setting timer: D

Command	D3	D2	D1	D0
KICK (D)	11.6ms	5.8ms	2.9ms	1.45ms

Ex.) D3 = 0, D2 = D1 = D0 = 1 (Initial Reset)
D = 10.15ms

$7X commands

Auto sequence track jump/move count setting (N)

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Auto sequence track jump count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

This command is used to set N when a 2N-track jump and an N-track move are executed for auto sequence.

- The maximum track count is 65,535, but note that with 2N-track jumps the maximum track jump count is determined by the mechanical limitations of the optical system.
- The number of tracks jumped is counted according to the signals input from the CNIN pin.

$8X commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
MODE specification	CDROM	DOUT Mute	DOUT ON/OFF	WSEL	VCO SEL1	0	SOCT	VCO SEL2	KSL3	KSL2	KSL1	KSL0

See the $BX commands.

Data 4				Data 5				Data 6			
D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
0	0	VCO2 THRU	0	0	0	0	0	TXON	TXOUT	OUTL1	OUTL0

Command bit	C2PO timing	Processing
CDROM = 1	See Timing Chart 1-1.	CDROM mode; average value interpolation and pre-value hold are not performed.
CDROM = 0	See Timing Chart 1-1.	Audio mode; average value interpolation and pre-value hold are performed.

Command bit	Processing
DOUT Mute = 1	Digital Out output is muted. (DA output is not muted.)
DOUT Mute = 0	When no other mute conditions are set, Digital Out output is not muted.

Command bit	Processing
DOUT ON/OFF = 1	Digital Out is output from the DOUT pin.
DOUT ON/OFF = 0	Digital Out is not output from the DOUT pin.

Command bit	Sync protection window width	Application
WSEL = 1	±26 channel clock*1	Anti-rolling is enhanced.
WSEL = 0	±6 channel clock	Sync window protection is enhanced.

*1 In normal-speed playback, channel clock = 4.3218MHz.

Command bit			Processing
VCOSEL1	KSL3	KSL2	
0	0	0	Multiplier PLL VCO1 is set to normal speed, and the output is 1/1 frequency-divided.
0	0	1	Multiplier PLL VCO1 is set to normal speed, and the output is 1/2 frequency-divided.
0	1	0	Multiplier PLL VCO1 is set to normal speed, and the output is 1/4 frequency-divided.
0	1	1	Multiplier PLL VCO1 is set to normal speed, and the output is 1/8 frequency-divided.
1	0	0	Multiplier PLL VCO1 is set to high speed*1, and the output is 1/1 frequency-divided.
1	0	1	Multiplier PLL VCO1 is set to high speed*1, and the output is 1/2 frequency-divided.
1	1	0	Multiplier PLL VCO1 is set to high speed*1, and the output is 1/4 frequency-divided.
1	1	1	Multiplier PLL VCO1 is set to high speed*1, and the output is 1/8 frequency-divided.

*1 Approximately twice the normal speed.

Command bit			Processing
VCOSEL2	KSL1	KSL0	
0	0	0	Wide-band PLL VCO2 is set to normal speed, and the output is 1/1 frequency-divided.
0	0	1	Wide-band PLL VCO2 is set to normal speed, and the output is 1/2 frequency-divided.
0	1	0	Wide-band PLL VCO2 is set to normal speed, and the output is 1/4 frequency-divided.
0	1	1	Wide-band PLL VCO2 is set to normal speed, and the output is 1/8 frequency-divided.
1	0	0	Wide-band PLL VCO2 is set to high speed*2, and the output is 1/1 frequency-divided.
1	0	1	Wide-band PLL VCO2 is set to high speed*2, and the output is 1/2 frequency-divided.
1	1	0	Wide-band PLL VCO2 is set to high speed*2, and the output is 1/4 frequency-divided.
1	1	1	Wide-band PLL VCO2 is set to high speed*2, and the output is 1/8 frequency-divided.

*2 Approximately twice the normal speed.

Command bit	Processing
VCO2 THRU = 0	V16M output is connected to VCKI inside the IC. Set VCKI to low in this time.
VCO2 THRU = 1	V16M output is not connected to VCKI inside the IC. Input the clock from VCKI in this time.

* These commands are used to set the internal or external connection of VCO2 used in CAV-W mode.

Command bit	Processing
TXON = 0	Set TXON to 0 when the CD-TEXT data is not demodulated.
TXON = 1	Set TXON to 1 when the CD-TEXT data is demodulated.

* See "4-9. CD-TEXT Data Demodulation".

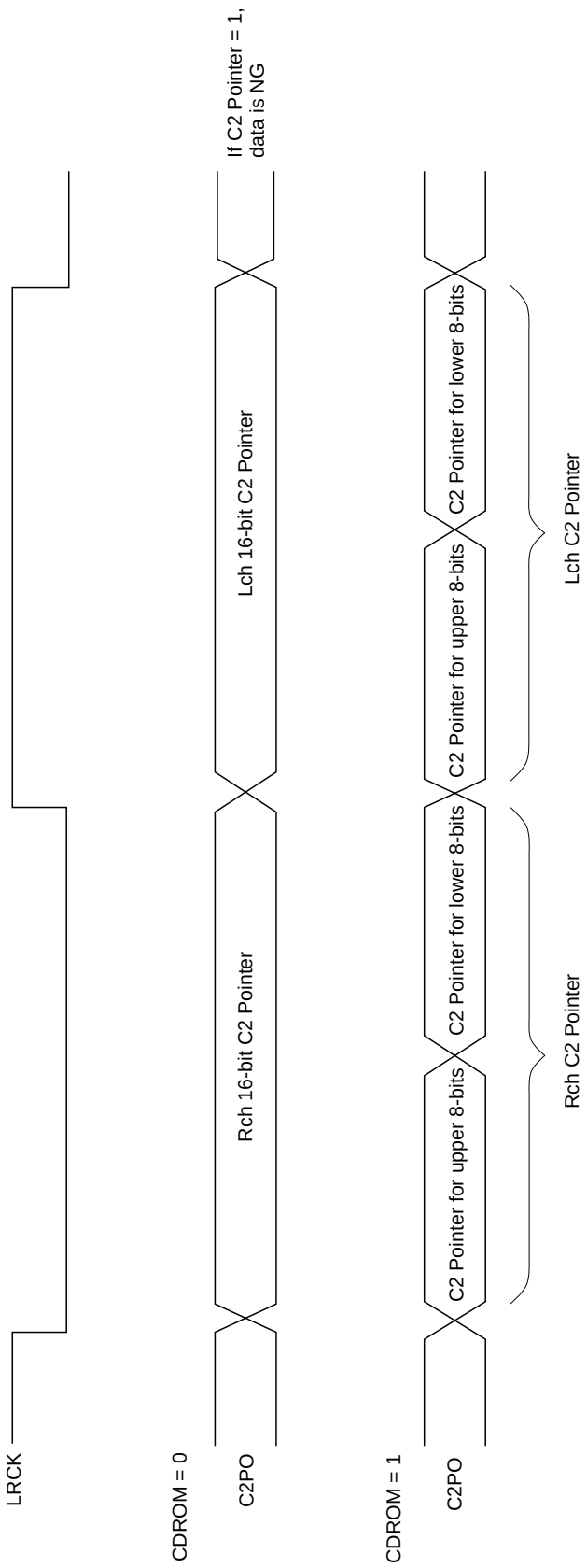
Command bit	Processing
TXOUT = 0	Various signals except CD-TEXT are output from SQSO pin. See $BX commands.
TXOUT = 1	CD-TEXT data is output from SQSO pin.

* See "4-9. CD-TEXT Data Demodulation".

Command bit	Processing
OUTL1 = 0	WFCK, XPCK and C4M are output.
OUTL1 = 1	WFCK, XPCK and C4M outputs are set to low.

Command bit	Processing
OUTL0 = 0	PCMD, BCK, LRCK and EMPH are output.
OUTL0 = 1	PCMD, BCK, LRCK and EMPH outputs are set to low. PCMD and PCMDI, BCK and BCKI, LRCK and LRCKI, EMPH and EMPHI are connected inside the IC, respectively. At this time, set PCMDI = BCKI = LRCKI = EMPHI = low.

Timing Chart 1-1



$9X commands (OPSL1= 0)

* Data 2 D0 and subsequent data are DF/DAC function settings.

Command	Data 1				Data 2		Data 3				Data 4			
	D3	D2	D1	D0	D3 to D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Function specification	0	DSPB ON/OFF	0	0	000	SYCOF	0	MCSL	0	0	ZDPL	ZMUT	—	—

OPSL1

Data 5			
D3	D2	D1	D0
—	—	—	—

$9X commands (OPSL1= 1)

* Data 2 D0 and subsequent data are DF/DAC function settings.

Command	Data 1				Data 2		Data 3				Data 4			
	D3	D2	D1	D0	D3 to D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Function specification	0	DSPB ON/OFF	0	0	000	SYCOF	1	MCSL	0	0	ZDPL	ZMUT	0	0

OPSL1

Data 5			
D3	D2	D1	D0
0	DCOF	0	0

Command bit	Processing
DSPB = 1	Double-speed playback (CD-DSP block)
DSPB = 0	Normal-speed playback (CD-DSP block)

Command bit	Processing
SYCOF = 1	LRCK asynchronous mode
SYCOF = 0	Normal operation

* Set SYCOF = 0 in advance when setting the $AX command LRWO to 1.

Command bit	Processing
OPSL1 = 1	DCOF can be set.
OPSL1 = 0	DCOF cannot be set.

Command bit	Processing
MCSL = 1	DF/DAC block master clock selection. Crystal = 768Fs (33.8688MHz)
MCSL = 0	DF/DAC block master clock selection. Crystal = 384Fs (16.9344MHz)

Command bit	Processing
ZDPL = 1	LMUT and RMUT pins are high when muted.
ZDPL = 0	LMUT and RMUT pins are low when muted.

* See "Mute flag output" for the mute flag output conditions.

Command bit	Processing
ZMUT = 1	Zero detection mute is on.
ZMUT = 0	Zero detection mute is off.

Command bit	Processing
DCOF = 1	DC offset is off.
DCOF = 0	DC offset is on.

* DCOF can be set when OPSL1 = 1.
* Set DC offset to off when zero detection mute is on.

$AX commands (OPSL2 = 0)

* Data 2 and subsequent data are DF/DAC function settings.

Command	Data 1				Data 2				Data 3	
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2
Audio CTRL	0	0	Mute	ATT	0	0	0	EMPH	SMUT	AD10

OPSL2

Data 3		Data 4				Data 5				Data 6			
D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—

$AX commands (OPSL2 = 1)

* Data 2 and subsequent data are DF/DAC function settings.

Command	Data 1				Data 2				Data 3	
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2
Audio CTRL	0	0	Mute	ATT	0	0	1	EMPH	SMUT	AD10

OPSL2

Data 3		Data 4				Data 5				Data 6			
D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FMUT	LRWO	BSBST	BBSL

Command bit	Processing
Mute = 1	CD-DSP block mute is on. 0 data is output from the CD-DSP block.
Mute = 0	CD-DSP block mute is off.

Command bit	Processing
ATT = 1	CD-DSP block output is attenuated (–12dB).
ATT = 0	CD-DSP block attenuation is off.

Command bit	Meaning
OPSL2 = 1	FMUT, LRWO, BSBST and BBSL can be set.
OPSL2 = 0	FMUT, LRWO, BSBST and BBSL cannot be set.

Command bit	Processing
EMPH = 1	De-emphasis is on.
EMPH = 0	De-emphasis is off.

* If either the EMPHI pin or EMPH is high, de-emphasis is on.

Command bit	Processing
SMUT = 1	Soft mute is on.
SMUT = 0	Soft mute is off.

* If either the SMUT pin or SMUT is high, soft mute is on.

Command bit	Meaning
AD9 to 0	Attenuation data.

The attenuation data consists of 10 bits, and is set as follows.

Attenuation data	Audio output
400h	0dB
3FFh 3FEh : 001h	–0.0085dB –0.017dB –60.206dB
000h	– ∞

The attenuation data (AD10 to AD0) consists of 11bits, and can be set in 1024 different ways.
The audio output from 001h to 400h is obtained using the following equation.

$$\text{Audio output} = 20\log \frac{\text{Attenuation data}}{1024} \quad [\text{dB}]$$

Command bit	Meaning
FMUT = 1	Forced mute is on.
FMUT = 0	Forced mute is off.

* FMUT can be set when OPSL2 = 1.

Command bit	Meaning
LRWO = 1	Forced synchronization mode **Note)**
LRWO = 0	Normal operation.

* LRWO can be set when OPSL2 = 1.

Note) Synchronization is performed at the first falling edge of LRCK during reset, so there is normally no need to set this mode. However, synchronization can be forcibly performed by setting LRWO = 1.

Command bit	Processing
BSBST = 1	Bass boost is on.
BSBST = 0	Bass boost is off.

* BSBST can be set when OPSL2 = 1.

Command bit	Processing
BBSL = 1	Bass boost is Max.
BBSL = 0	Bass boost is Mid.

* BBSL can be set when OPSL2 = 1.

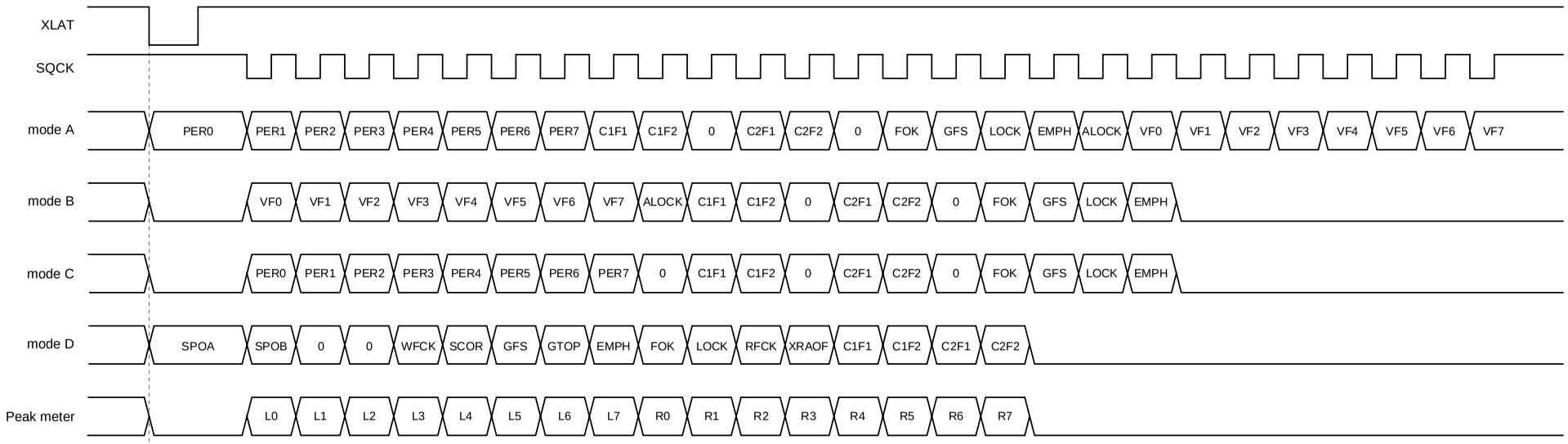
$BX commands

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
Serial bus CTRL	SL1	SL0	CPUSR	0	TRM1	TRM0	MTSL1	MTSL0

SOCT	SL1	SL0	mode
0	0	0	SubQ
0	0	1	Peak meter
0	1	0	SENS
0	1	1	D
1	0	0	SubQ
1	0	1	A
1	1	0	B
1	1	1	C

The SQSO pin output can be switched to the various signals by setting the SOCT command of $8X and the SL1 and SL0 commands of $BX. Set SQCK to high at the falling edge of XLAT.

Except for Sub Q and peak meter, the signals are loaded to the register when they are set at the falling edge of XLAT. Sub Q is loaded to the register with each SCOR, and Peak meter is loaded when a peak is detected.



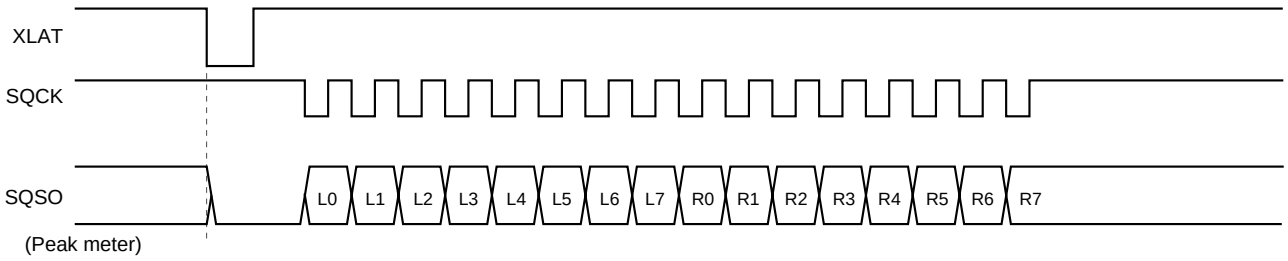
Signal	Description
PER0 to 7	RF jitter amount (used to adjust the focus bias). 8-bit binary data in PER0 = LSB, PER7 = MSB.
FOK	Focus OK
GFS	High when the frame sync and the insertion protection timing match.
LOCK	GFS is sampled at 460Hz; when GFS is high, a high signal is output. If GFS is low eight consecutive samples, a low signal is output.
EMPH	High when the playback disc has emphasis.
ALOCK	GFS is sampled at 460Hz; when GFS is high eight consecutive samples, a high signal is output. If GFS is low eight consecutive samples, a low signal is output.
VF0 to 7	Used in CAV-W mode. Results of measuring the disc rotational velocity. (See Timing Chart 2-3.) VF0 = LSB, VF7 = MSB.
SPOA, B	SPOA and B pin inputs.
WFCK	Write frame clock output.
SCOR	High when either subcode sync S0 or S1 is detected.
GTOP	High when the sync protection window is open.
RFCK	Read frame clock output.
XRAOF	Low when the built-in 16K RAM exceeds the ±4 frame jitter margin.
L0 to L7, R0 to R7	Peak meter register output. L0 to 7 are the left-channel and R0 to 7 are the right-channel peak data. L0 and R0 are LSB.

C1F1	C1F2	C1 correction status
0	0	No Error
1	0	Single Error Correction
1	1	Irretrievable Error

C2F1	C2F2	C2 correction status
0	0	No Error
1	0	Single Error Correction
1	1	Irretrievable Error

Command bit	Processing
CPUSR = 1	XLON pin is high.
CPUSR = 0	XLON pin is low.

Peak meter



Setting the SOCT command of $8X to 0 and the SL1 and SL0 commands of $BX to 0 and 1, respectively, results in peak detection mode. The SQSO output is connected to the peak register. The maximum PCM data values (absolute value, upper 8bits) for the left and right channels can be read from SQSO by inputting 16 clocks to SQCK. Peak detection is not performed during SQCK input, and the peak register does not change during readout. This SQCK input judgment uses a retriggerable monostable multivibrator with a time constant of 270µs to 400µs. The time during which SQCK input is high should be 270µs or less. Also, peak detection is restarted 270µs to 400µs after SQCK input.

The peak register is reset with each readout (16 clocks input to SQCK).
The maximum value in peak detection mode is detected and held in this status until the next readout. When switching to peak detection mode, readout should be performed one time initially to reset the peak detection register.

Peak detection can also be performed for previous value hold and average value interpolation data.

Traverse monitor count value setting

These bits are set when monitoring the traverse condition of the SENS output according to the CNIN frequency division.

Command bit		Processing
TRM1	TRM0	
0	0	1/64 frequency division
0	1	1/128 frequency division
1	0	1/256 frequency division
1	1	1/512 frequency division

Monitor output switching

The monitor output can be switched to the various signals by setting the MTSL1 and MTSL0 commands of $B.

		Mode description			
Command bit \ Pin No.		47	48	49	50
MTSL1	MTSL0				
0	0	XUGF	XPCK	GFS	C2PO
0	1	MNT1	MNT0	MNT3	C2PO
1	0	RFCK	XPCK	XROF	GTOP

$CX commands

Command	D3	D2	D1	D0
Servo coefficient setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0
CLV CTRL ($DX)				Gain CLVS

• CLV mode gain setting: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	–12dB
0	0	1	–6dB
0	1	0	–6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

• CLVP mode gain setting: GMDP: GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	–6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	–6dB
0	1	0dB
1	0	+6dB

$DX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
CLV CTRL	0	TB	TP	Gain CLVS	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0

See the $CX commands.

Command bit	Description
TB = 0	Bottom hold at a cycle of RFCK/32 in CLVS mode.
TB = 1	Bottom hold at a cycle of RFCK/16 in CLVS mode.
TP = 0	Peak hold at a cycle of RFCK/4 in CLVS mode.
TP = 1	Peak hold at a cycle of RFCK/2 in CLVS mode.

Command bit	Description
VP0 to 7 = F0 (H)	Playback at half (normal) speed to Playback at normal (double) speed
:	
VP0 to 7 = E0 (H)	

The rotational velocity R of the spindle can be expressed with the following equation.

$$R = \frac{256 - n}{32}$$

R: Relative velocity at normal speed = 1

n: VP0 to 7 setting value

Note) • Values in parentheses are for when DSPB is 1.
• Values when crystal is 16.9344MHz and XTSL is low or when crystal is 33.8688MHz and XTSL is high.
• VP0 to 7 setting values are valid in CAV-W mode.

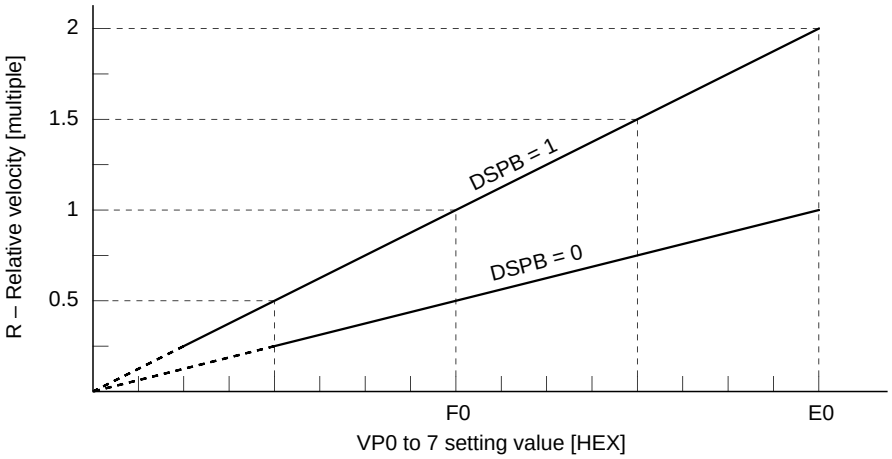


Fig. 1-1

$EX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
CLV mode	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON

Command bit				Mode	Description
CM3	CM2	CM1	CM0		
0	0	0	0	STOP	Spindle stop mode.*1
1	0	0	0	KICK	Spindle forward rotation mode.*1
1	0	1	0	BRAKE	Spindle reverse rotation mode. Valid only when LPWR = 0, in any mode.*1
1	1	1	0	CLVS	Rough servo mode. When the RF-PLL circuit isn't locked, this mode is used to pull the disc rotations within the RF-PLL capture range.
1	1	1	1	CLVP	PLL servo mode.
0	1	1	0	CLVA	Automatic CLVS/CLVP switching mode. Used for normal playback.

*1 See Timing Charts 1-2 to 1-6.

Command bit								Mode	Description
EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON		
0	0	0	0	0	0	0	0	CLV-N	Crystal reference CLV servo.
0	0	0	0	1	1	0	0	CLV-W	Used for normal-speed playback in CLV-W mode.*2
0	1	1	0	0	1	0	1	CAV-W	Spindle control with VP0 to 7.
1	0	1	0	0	1	0	1	CAV-W	Spindle control with the external PWM.

*2 Figs. 3-1 and 3-2 show the control flow with the microcomputer software in CLV-W mode.

Command	Data 4			
	D3	D2	D1	D0
SPD mode	Gain CAV1	Gain CAV0	0	0

Gain CAV1	Gain CAV0	Gain
0	0	0dB
0	1	–6dB
1	0	–12dB
1	1	–18dB

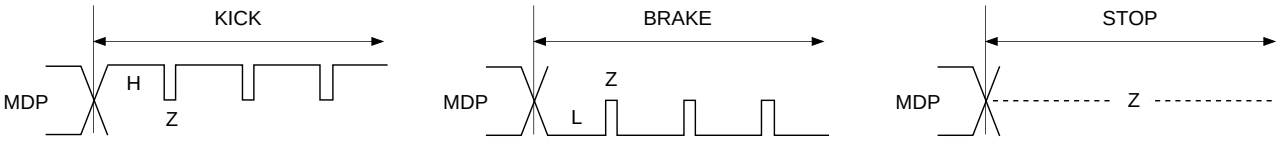
- This sets the gain when controlling the spindle with the phase comparator in CAV-W mode.

Mode	LPWR	Command	Timing chart
CLV-N	0	KICK	1-2 (a)
		BRAKE	1-2 (b)
		STOP	1-2 (c)
CLV-W	0	KICK	1-3 (a)
		BRAKE	1-3 (b)
		STOP	1-3 (c)
	1	KICK	1-4 (a)
		BRAKE	1-4 (b)
		STOP	1-4 (c)
CAV-W	0	KICK	1-5 (a)
		BRAKE	1-5 (b)
		STOP	1-5 (c)
	1	KICK	1-6 (a)
		BRAKE	1-6 (b)
		STOP	1-6 (c)

Mode	LPWR	Timing chart
CLV-N	0	1-7
CLV-W	0	1-8
	1	1-9
CAV-W	0	1-10 (EPWM = 0)
	1	1-11 (EPWM = 0)
	0	1-12 (EPWM = 1)
	1	1-13 (EPWM = 1)

Timing Chart 1-2

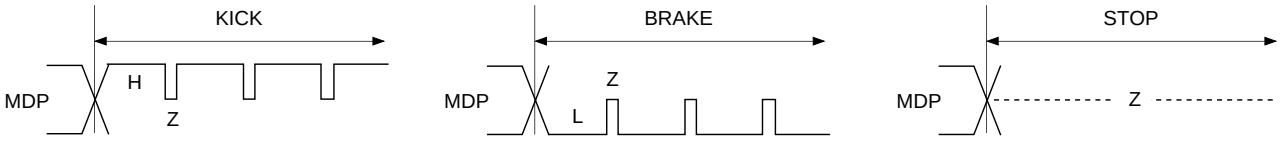
CLV-N mode LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-3

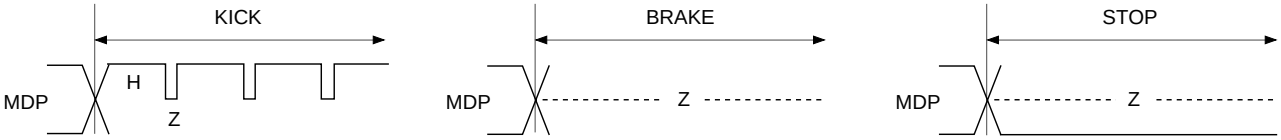
CLV-W mode (when following the spindle rotational velocity) LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-4

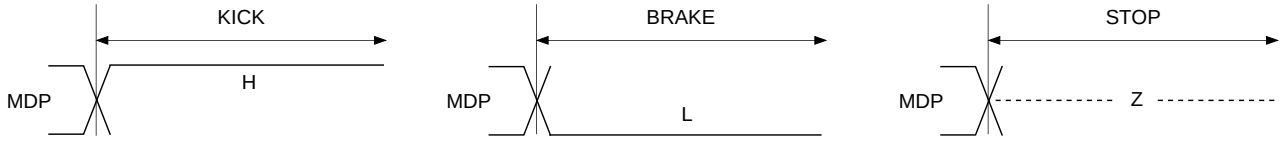
CLV-W mode (when following the spindle rotational velocity) LPWR = 1



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-5

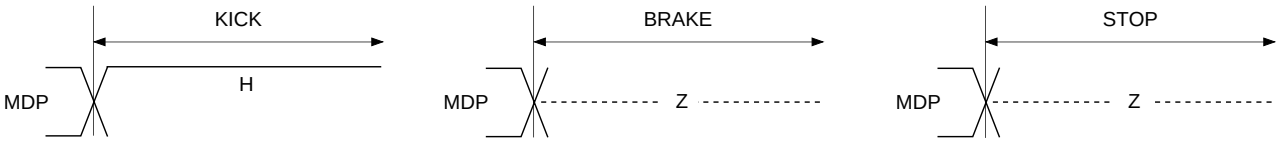
CAV-W mode LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-6

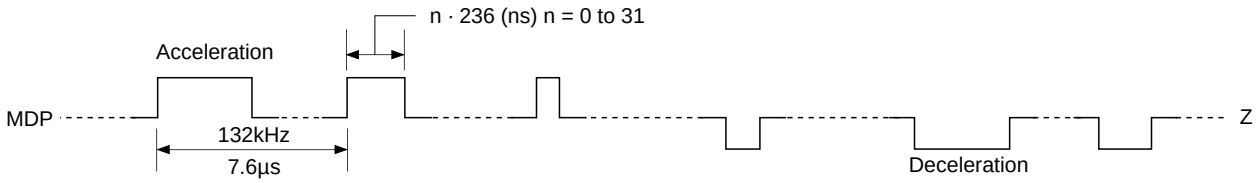
CAV-W mode LPWR = 1



(a) KICK (b) BRAKE (c) STOP

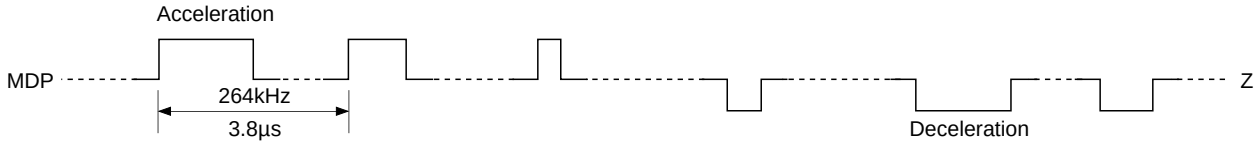
Timing Chart 1-7

CLV-N mode LPWR = 0



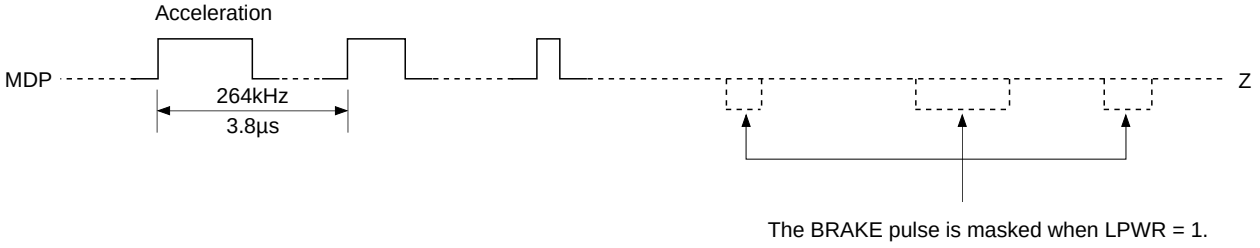
Timing Chart 1-8

CLV-W mode LPWR = 0



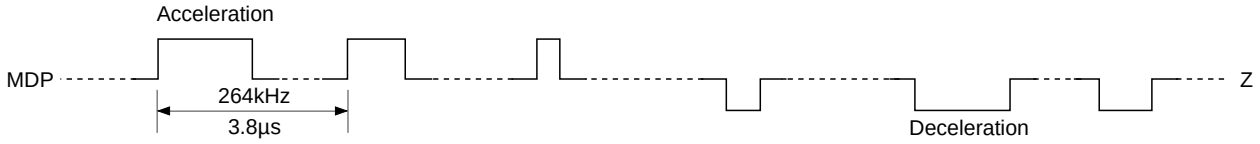
Timing Chart 1-9

CLV-W mode LPWR = 1



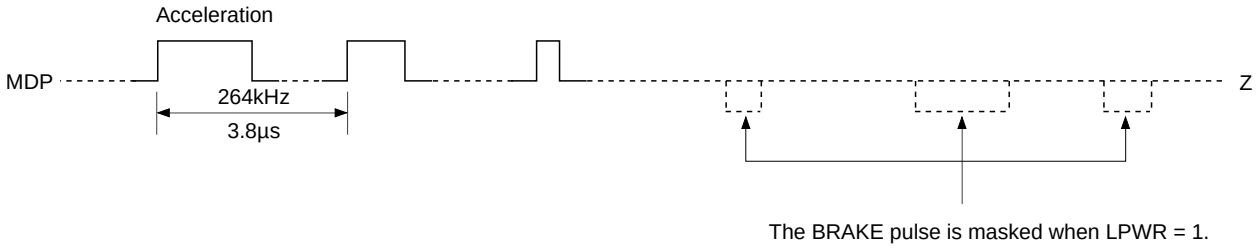
Timing Chart 1-10

CAV-W mode EPWM = LPWR = 0



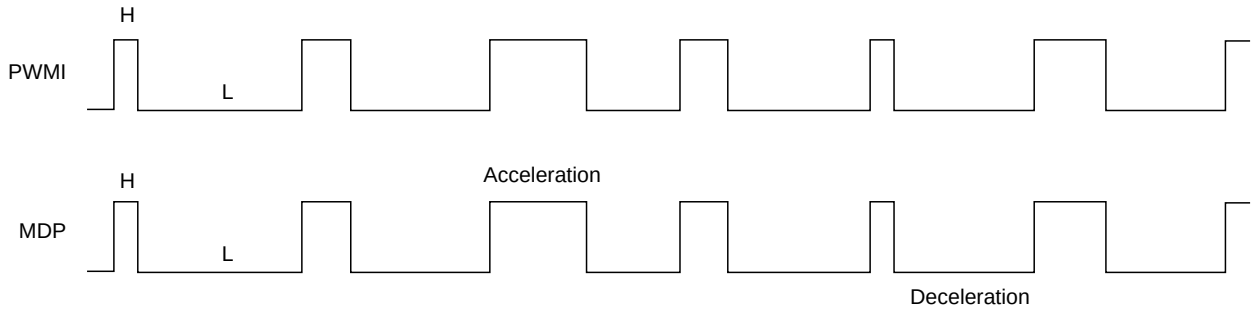
Timing Chart 1-11

CAV-W mode EPWM = LPWR = 1



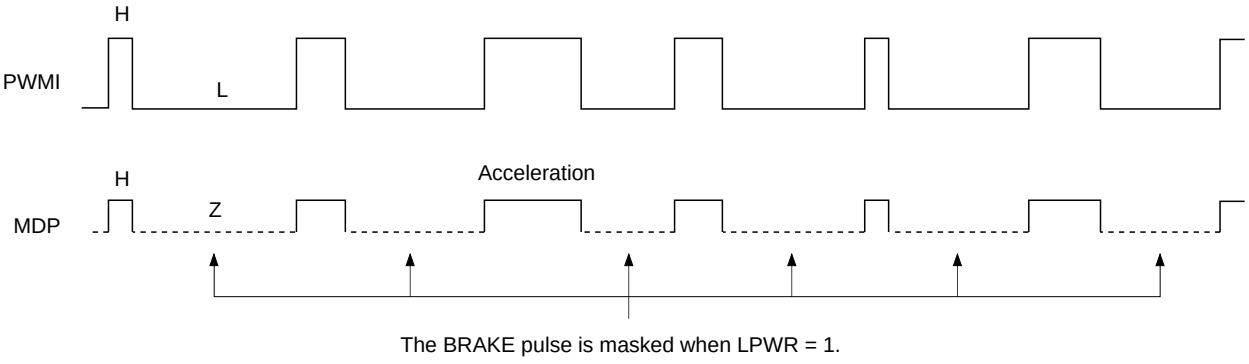
Timing Chart 1-12

CAV-W mode EPWM = 1, LPWR = 0



Timing Chart 1-13

CAV-W mode EPWM = LPWR = 1



1-2. Description of SENS Output

The following signals are output from SENS, depending on the microcomputer serial register value (latching not required).

Microcomputer serial register value (latching not required)	SENS output	Meaning
$0X, 1X, 2X, 3X	SEIN	SEIN, a signal input to this LSI from the SSP, is output.
$4X	XBUSY	Low while the auto sequencer is in operation, high when operation terminates.
$5X	FOK	Outputs the signal input to the FOK pin. Normally, FOK (from RF) is input. High for "focus OK".
$6X	SEIN	SEIN, a signal input to this LSI from the SSP, is output.
$AX	GFS	High when the regenerated frame sync is obtained with the correct timing.
$EX	$\overline{\text{OV64}}$	Low when the EFM signal, after passing through the sync detection filter, is lengthened by 64 channel clock pulses or more.
$7X, 8X, 9X, BX, DX, FX	"L"	SENS pin is fixed to low.
$CX	CNIN division	Calculates the number of tracks from the frequency division ratio set by $B.High when $C is latched; toggles each time CNIN is input the number of times set in register B.

Note that the SENS output can be read out from the SQSO pin when SOCT = 0, SL1 = 1 and SL0 = 0. (See the $BX commands.)

2. Subcode Interface

This section explains the subcode interface.
There are two methods for reading out a subcode externally.
The 8-bit subcodes P to W can be read from SBSO by inputting EXCK to the CXD3009Q.
Sub Q can be read out after checking the CRC of the 80bits in the subcode frame.
Sub Q can be read out from the SQSO pin by inputting 80 clock pulses to the SQCK pin when SCOR comes correctly and CRCF is high.

2-1. P to W Subcode Readout

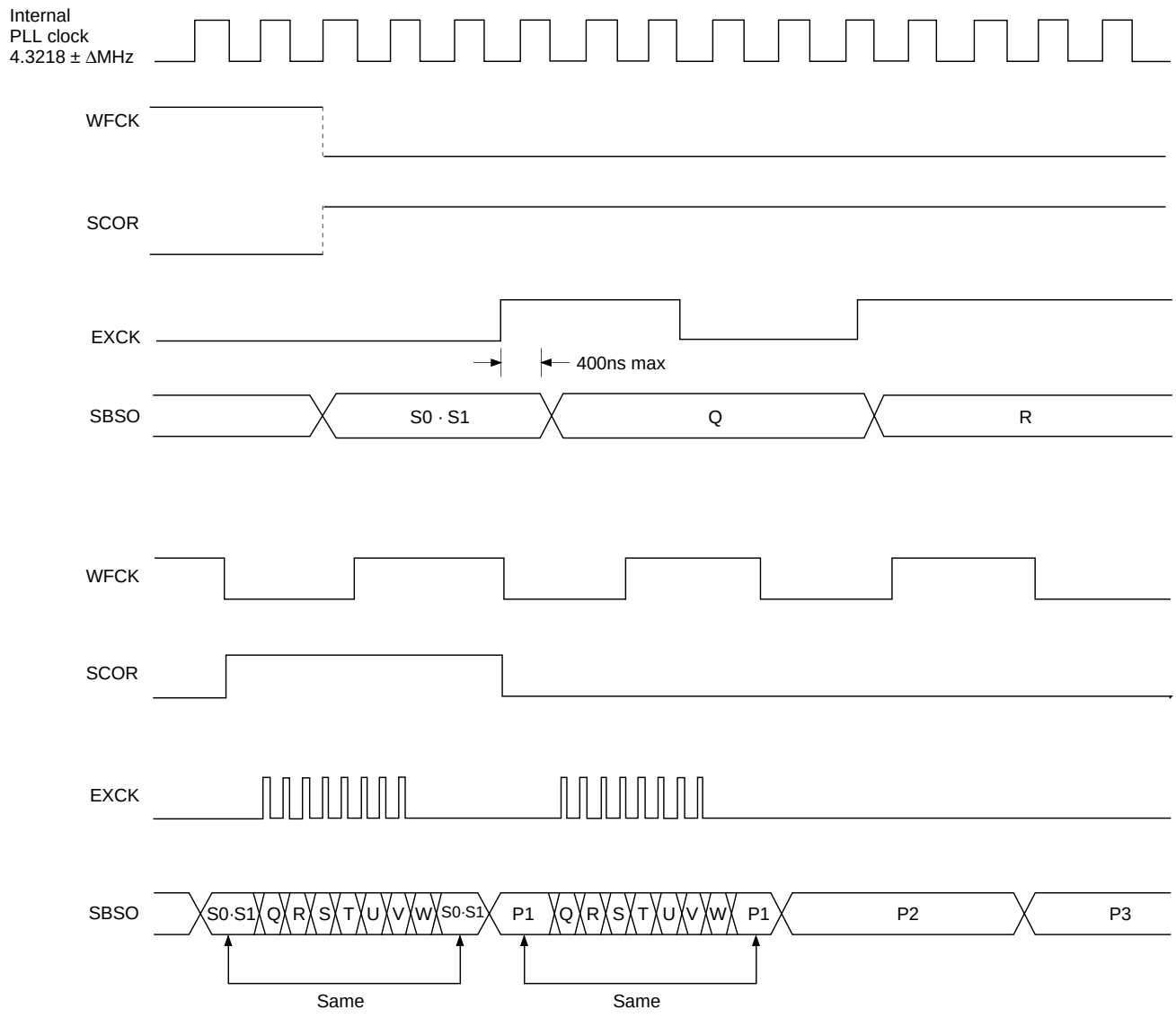
Data can be read out by inputting EXCK immediately after WFCK falls. (See Timing Chart 2-1.)

2-2. 80-bit Sub Q Readout

Fig. 2-1 shows the peripheral block of the 80-bit Sub Q register.

- First, Sub Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.
- 96-bit Sub Q is input, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, 80bits are loaded into the parallel/serial register.
  When SQSO goes high 400µs (monostable multivibrator time constant) or more after subcode readout, the CPU determines that new data (which passed the CRC check) has been loaded.
- When the 80-bit data is loaded, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of bytes is the same, the bits within the bytes are now ordered LSB first.
- Once the 80-bit data load is confirmed, SQCK is input so that the data can be read.
  The SQCK input is detected, and the retriggerable monostable multivibrator is reset while the input is low.
- The retriggerable monostable multivibrator has a time constant from 270µs to 400µs. When the duration when SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the serial/parallel register is not loaded into the parallel/serial register.
- While the monostable multivibrator is being reset, data cannot be loaded in the 80-bit parallel/serial register.
  In other words, while reading out with a clock cycle shorter than this time constant, the register will not be rewritten by CRCOK and others. (See Timing Chart 2-2.)
- The high and low intervals for SQCK should be between 750ns and 120µs.

Timing Chart 2-1



Sub Code P.Q.R.S.T.U.V.W Read Timing

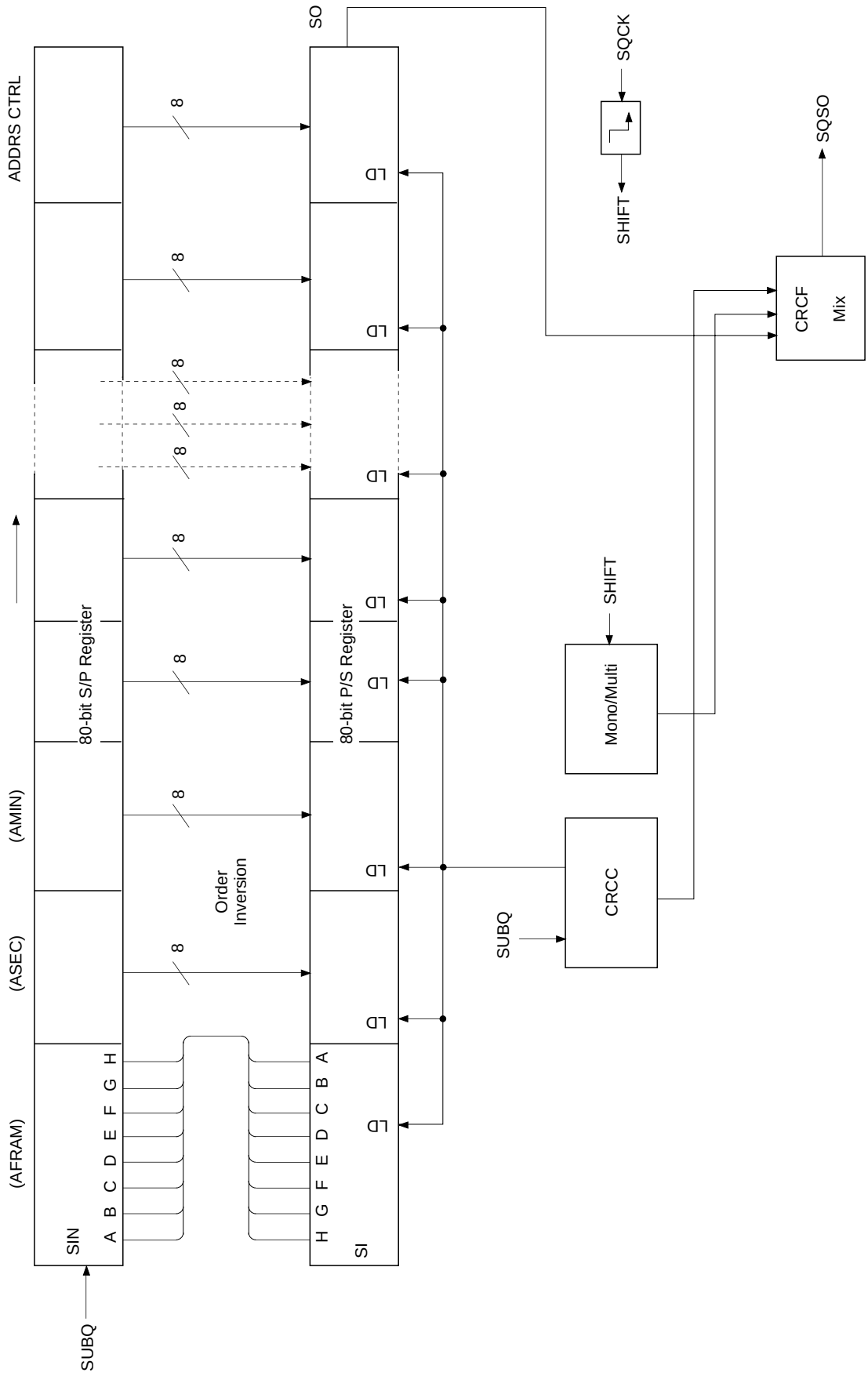
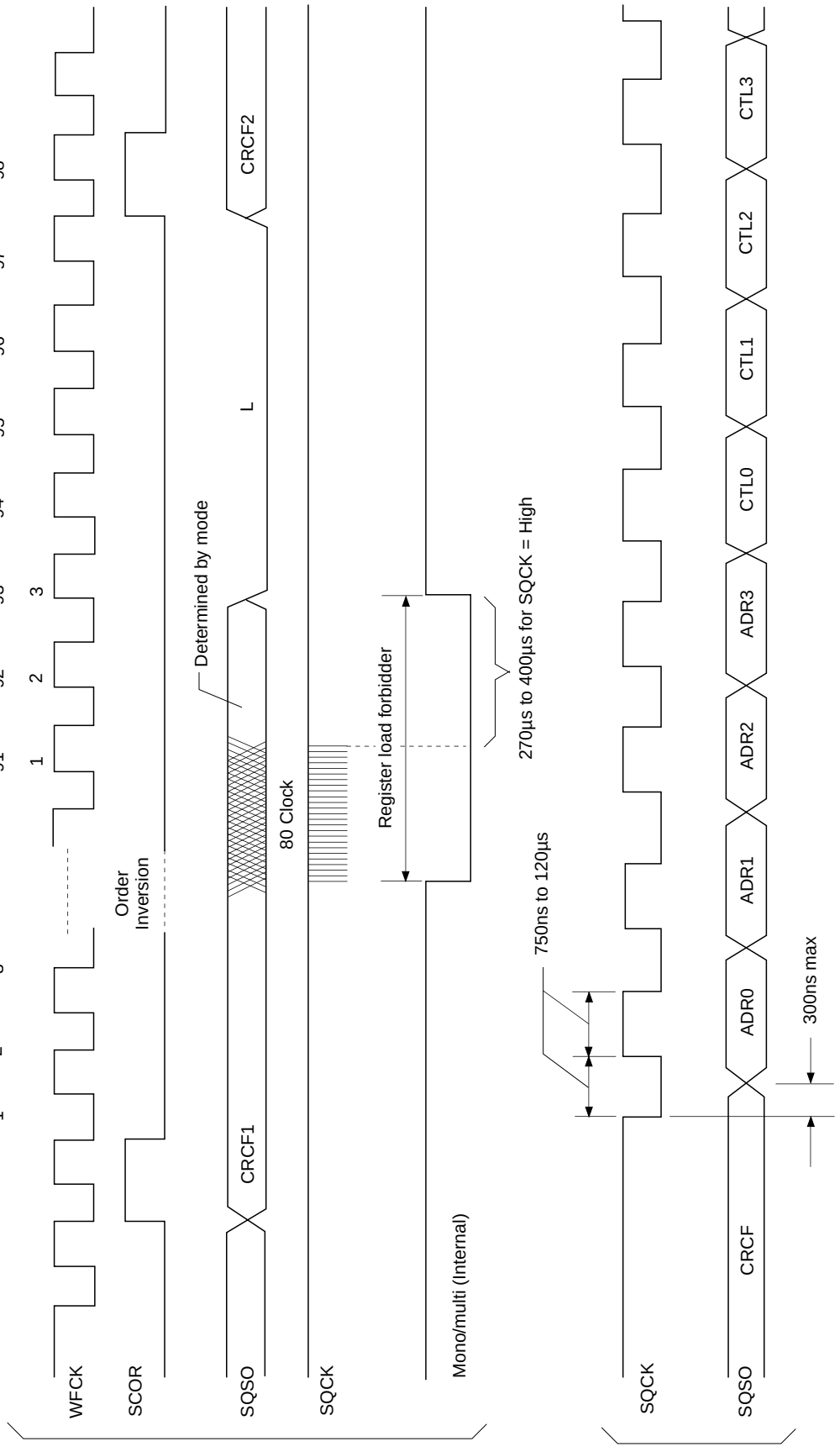
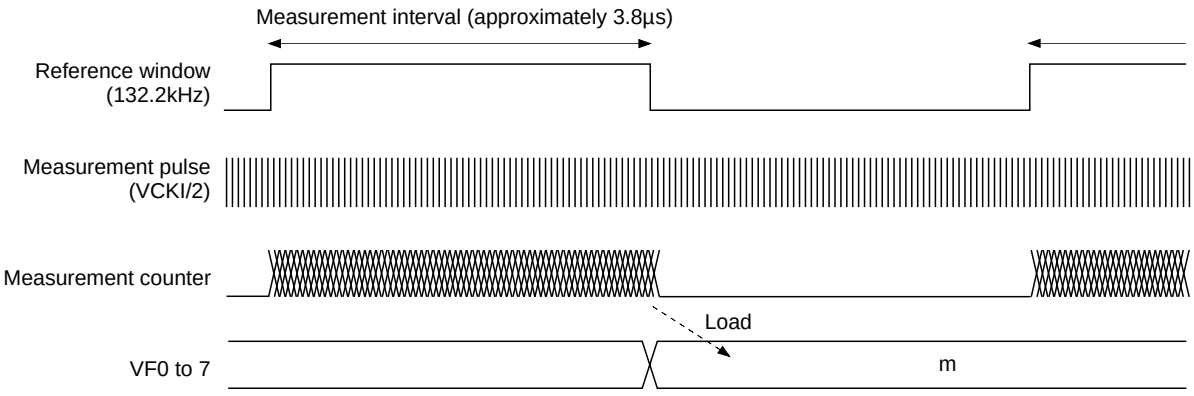


Fig. 2-1. Block Diagram

Timing Chart 2-2



Timing Chart 2-3



The relative velocity R of the disc can be expressed with the following equation.

$$R = \frac{m + 1}{32}$$ (R: Relative velocity, m: Measurement results)

VF0 to 7 is the result obtained by counting VCKI/2 pulses while the reference signal (132.2kHz) generated from the crystal (384Fs) is high. This count is 31 when the disc is rotating at normal speed and 63 when it is rotating at double speed (when DSPB is low).

3. Description of Modes

This LSI has three basic operating modes using a combination of spindle control and the PLL. The operations for each mode are described below.

3-1. CLV-N Mode

This mode is compatible with the CXD2507AQ, and operation is the same as for the conventional control. The PLL capture range is ±150kHz.

3-2. CLV-W Mode

This is the wide capture range mode. This mode allows the PLL to follow the rotational velocity of the disc. This rotational following control has two types: using the built-in VCO2 or providing an external VCO. The spindle is the same CLV servo as for the conventional series. Operation using the built-in VCO2 is described below. (When using an external VCO, input the signal from the VPCO pin to the low-pass filter, use the output from the low-pass filter as the control voltage for the external VCO, and input the oscillation output from the VCO to the VCKI pin.)

While starting to rotate a disc and/or speeding up to the lock range from the condition where the disc is stopped, CAV-W mode should be used. Specifically, first send $E6650 to set CAV-W mode and kick the disc, then send $E60C0 to set CLV-W mode if ALOCK is high, which can be read out serially from the SQSO pin. CLV-W mode can be used while ALOCK is high. The microcomputer monitors the serial data output, and must return the operation to the speed adjusting state (CAV-W mode) when ALOCK becomes low. The control flow according to the microcomputer software is shown in Fig. 3-2.

In CLV-W mode (normal), low power consumption is achieved by setting LPWR to high. Control was formerly performed by applying acceleration and deceleration pulses to the spindle motor. However, when LPWR is set to high, deceleration pulses are not output, thereby achieving low power consumption mode.

Note) The capture range for CLV-W mode has theoretically the range up to the signal processing limit.

3-3. CAV-W Mode

This is CAV mode. In this mode, the external clock is fixed and it is possible to control the spindle to the desired rotational velocity. The rotational velocity is determined by the VP0 to 7 setting values or the external PWM. When controlling the spindle with VP0 to 7, setting CAV-W mode with the $E6650 command and controlling VP0 to 7 with the $DX commands allows the rotational velocity to be varied from low-speed to double-speed. (See the $DX commands.) Also, when controlling the spindle with the external PWM, the PWMI pin is binary input which becomes KICK during high intervals and BRAKE during low intervals.

The microcomputer can know the rotational velocity using V16M. The reference for the velocity measurement is a signal of 132.2kHz obtained by dividing the crystal (384Fs) by 128. The velocity is obtained by counting V16M/2 pulses while the reference is high, and the result is output from the new CPU interface as 8 bits (VF0 to 7). These measurement results are 31 when the disc is rotating at normal speed or 63 when it is rotating at double speed. These values match those of the 256-n for control with VP0 to 7.

In CAV-W mode, the spindle is set to the desired rotational velocity and the operation speed for the entire system follows this rotational velocity. Therefore, the cycles for the Fs system clock, PCM data and all other output signals from this LSI change according to the rotational velocity of the disc (excluding DATO, CLKO and XLTO).

Note) The capture range for this mode is theoretically up to the signal processing limit.

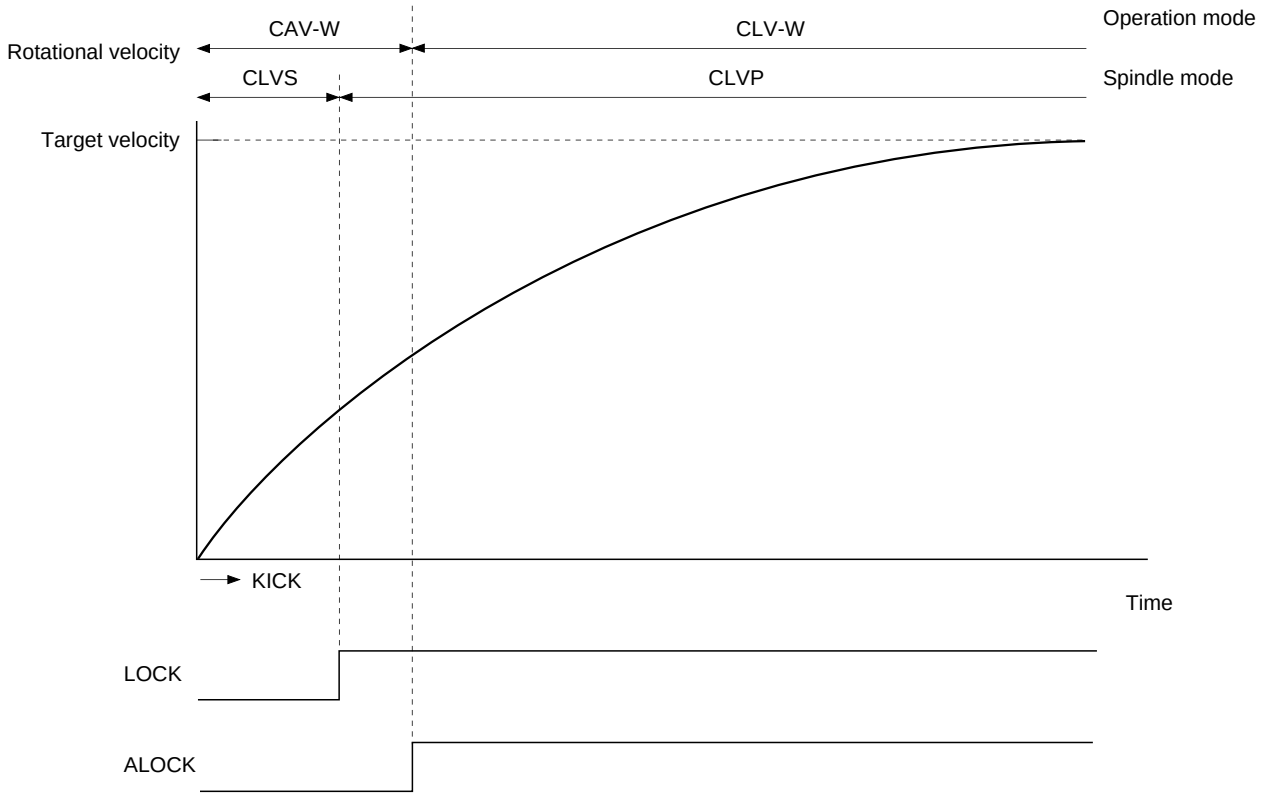


Fig. 3-1. Disc Stop to Normal Condition in CLV-W Mode

CLV-W Mode

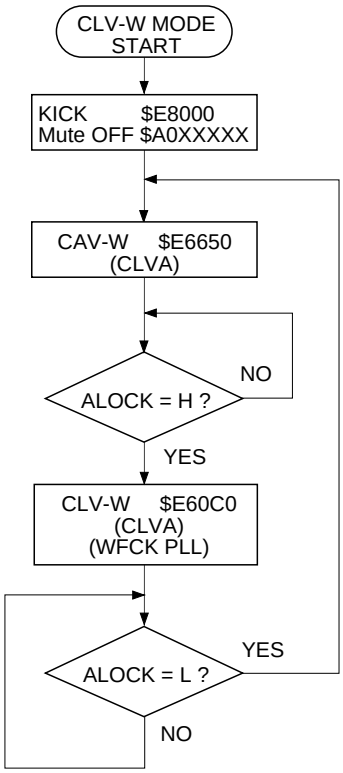


Fig. 3-2. CLV-W Mode Flow Chart

4. Description of Other Functions

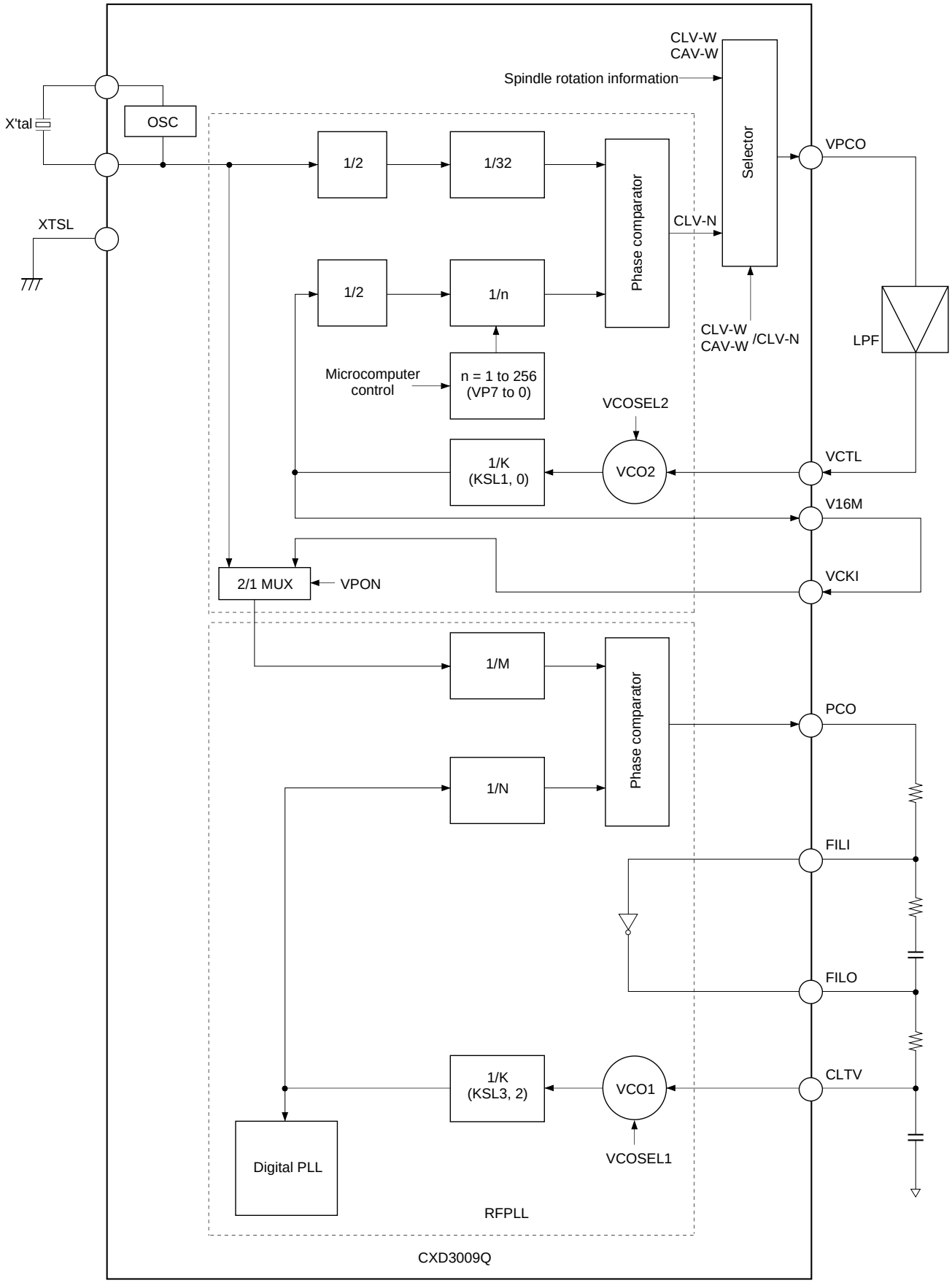
4-1. Channel Clock Regeneration by the Digital PLL Circuit

- The channel clock is necessary for demodulating the EFM signal regenerated by the optical system.
  Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from 3T to 11T. In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T, that is the channel clock, is necessary.
  In an actual player, a PLL is necessary to regenerate the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.

The block diagram of this PLL is shown in Fig. 4-1.
The CXD3009Q has a built-in three-stage PLL.

- The first-stage PLL is a wide-band PLL. When using the internal VCO2, an external LPF is necessary; when not using the internal VCO2, external LPF and VCO are necessary.
  The output of this first-stage PLL is used as a reference for all clocks within the LSI.
- The second-stage PLL generates the high-frequency clock needed by the third-stage digital PLL.
- The third-stage PLL is a digital PLL that regenerates the actual channel clock.
- A new digital PLL has been provided for CLV-W mode to follow the rotational velocity of the disc in addition to the conventional secondary loop.

Block Diagram 4-1



4-2. Frame Sync Protection

- In normal-speed playback, a frame sync is recorded approximately every 136µs (7.35kHz). This signal is used as a reference to recognize the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because the data cannot be recognized. As a result, recognizing the frame sync properly is extremely important for improving playability.

- In the CXD3009Q, window protection and forward protection/backward protection have been adopted for frame sync protection. These functions achieve very powerful frame sync protection. There are two window widths: one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is fixed to 13, and the backward protection counter to 3. Concretely, when the frame sync is being played back normally and then cannot be detected due to scratches, a maximum of 13 frames are inserted. If the frame sync cannot be detected for 13 frames or more, the window opens to resynchronize the frame sync.
  In addition, immediately after the window opens and the resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window opens immediately.

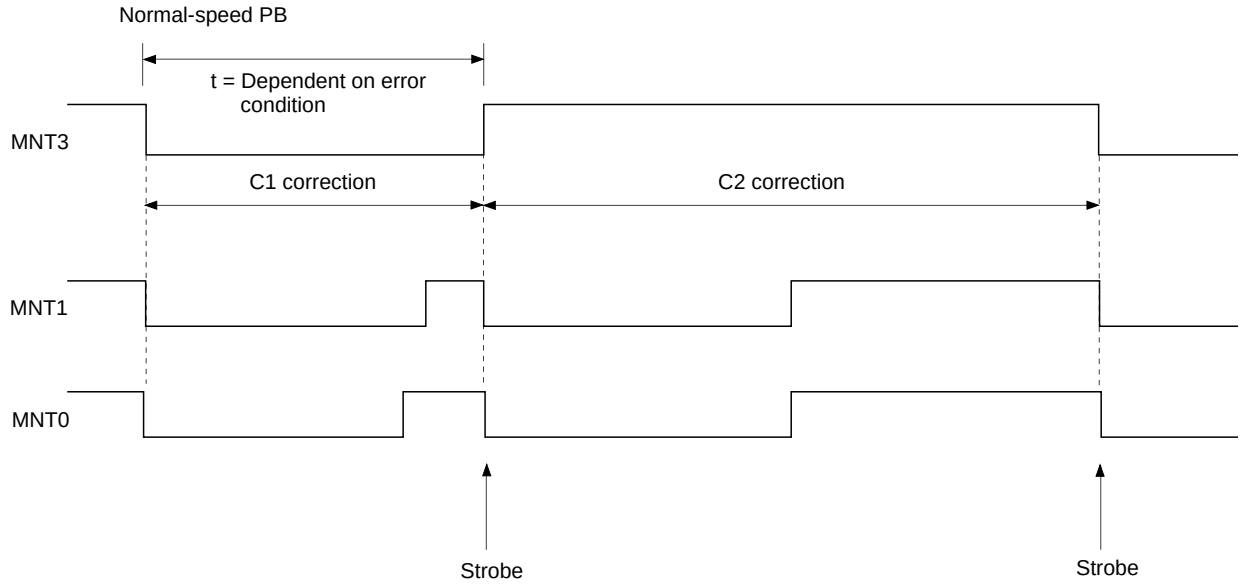
4-3. Error Correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.
  For C2 correction, the code is created with 24-byte information and 4-byte parity.
  Both C1 and C2 are Reed Solomon codes with a minimum distance of 5.
- The CXD3009Q's SEC strategy uses powerful frame sync protection and C1 and C2 error correction to achieve high playability.
- The correction status can be monitored externally.
  See Table 4-1.
- When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held or an average value interpolation was made for the data.

MNT3	MNT1	MNT0	Description
0	0	0	No C1 errors
0	0	1	One C1 error corrected
0	1	1	C1 correction impossible
1	0	0	No C2 errors
1	0	1	One C2 error corrected
1	1	1	C2 correction impossible

Table 4-1.

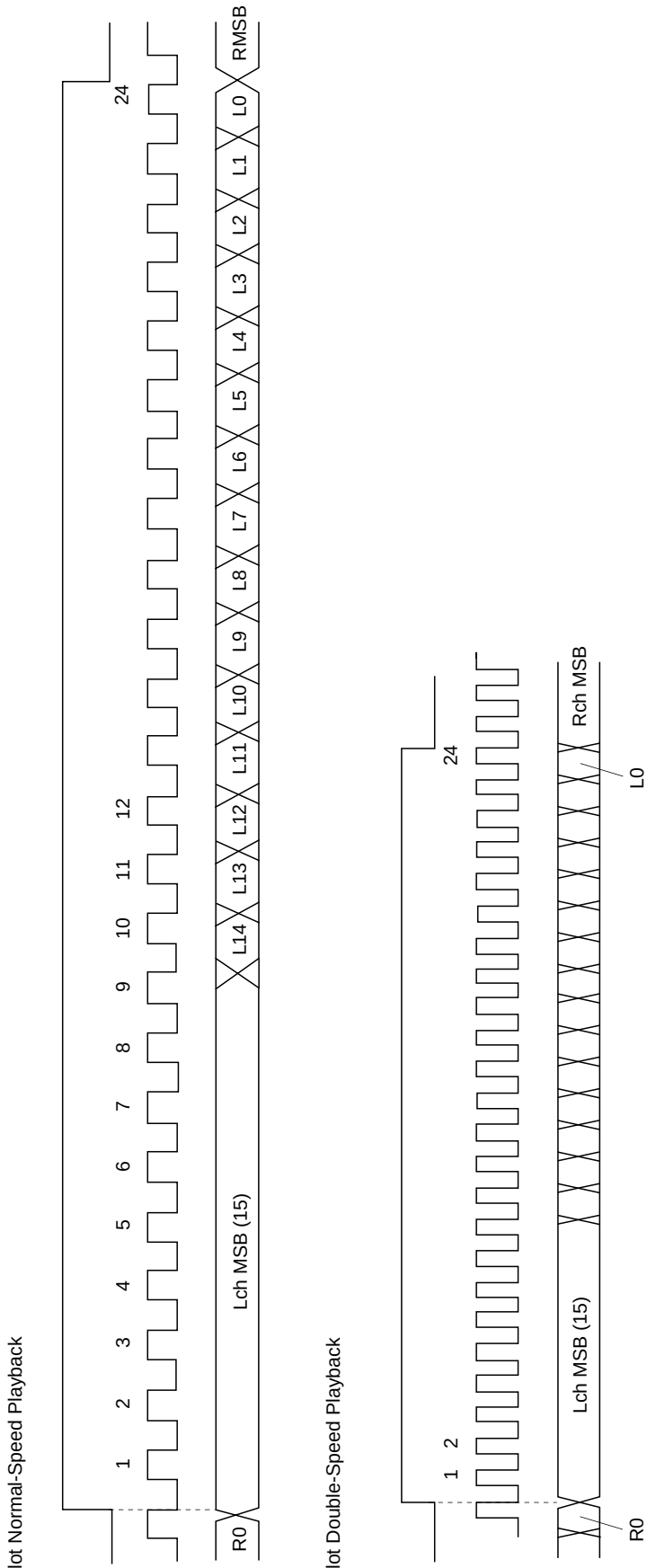
Timing Chart 4-1



4-4. DA Interface

- The CXD3009Q DA interface is as described below.
  This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first. When LRCK is high, the data is for the left channel.

Timing Chart 4-2



4-5. Digital Out

There are three Digital Out formats: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.

The CXD3009Q supports type 2 form 1.

Sub Q data which are matched twice in succession after a CRC check are input to the first four bits (bits 0 to 3) of the channel status.

Digital Out C bit

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub Q				0	0	0	0	1	0	0	0	0	0	0	0
	ID0	ID1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0
32																
48																
								0								
176																

Bits 0 to 3...Sub Q control bits that matched twice with CRCOK
Bit 29.....1 when VPON is 1

Table 4-2.

4-6. Servo Auto Sequence

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1-track jump, 2N-track jumps, and N-track move are executed automatically.

SSP (servo signal processor LSI) is used in an exclusive manner during the auto sequence execution (when XBUSY = low), so that commands from the CPU are not transferred to the SSP, but can be sent to the CXD3009Q.

Connect the CPU, RF and SSP as shown in Fig. 4-2.

When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point. This is to prevent the transfer of erroneous data to the SSP when XBUSY changes from low to high by the monostable multivibrator, which is reset by CLOK being low (when XBUSY is low).

(a) Auto Focus ($47)

Focus search-up is performed, FOK and FZC are checked, and the focus servo is turned on.

If $47 is received from the CPU, the focus servo is turned on according to Fig. 4-3. The auto focus starts with focus search-up, and the pickup should be lowered beforehand (focus search-down). In addition, blind E of register 5 is used to eliminate FZC chattering. In other words, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

Connection diagram for using auto sequencer (example)

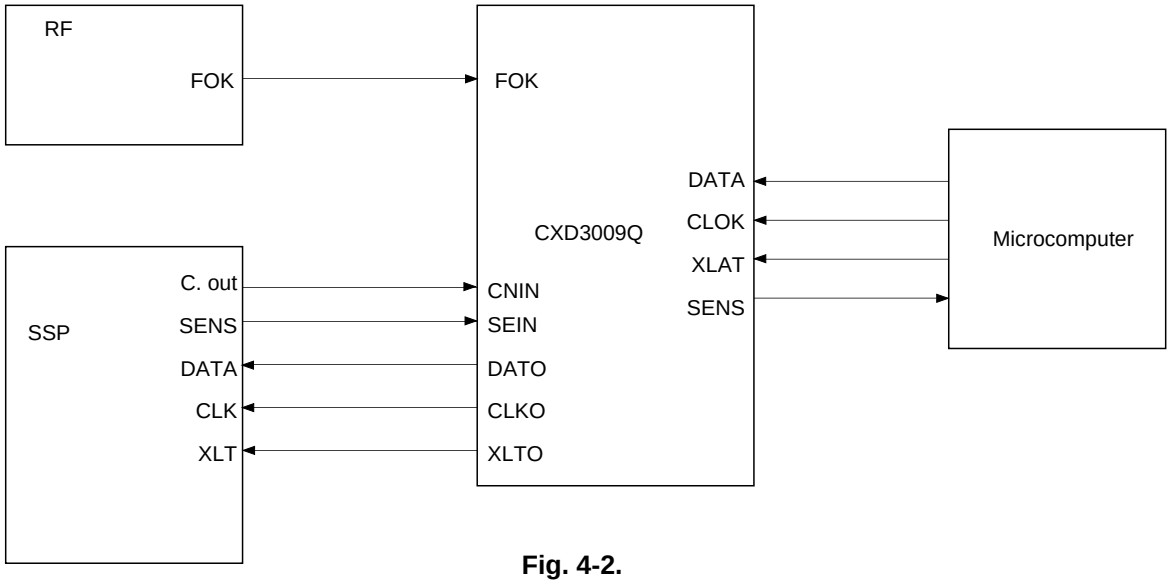


Fig. 4-2.

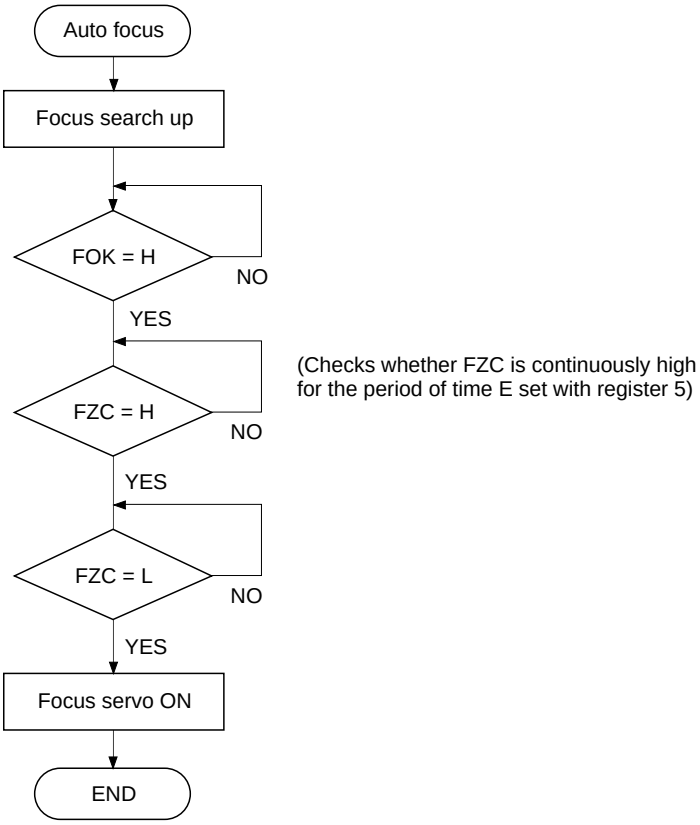


Fig. 4-3-(a). Auto Focus Flow Chart

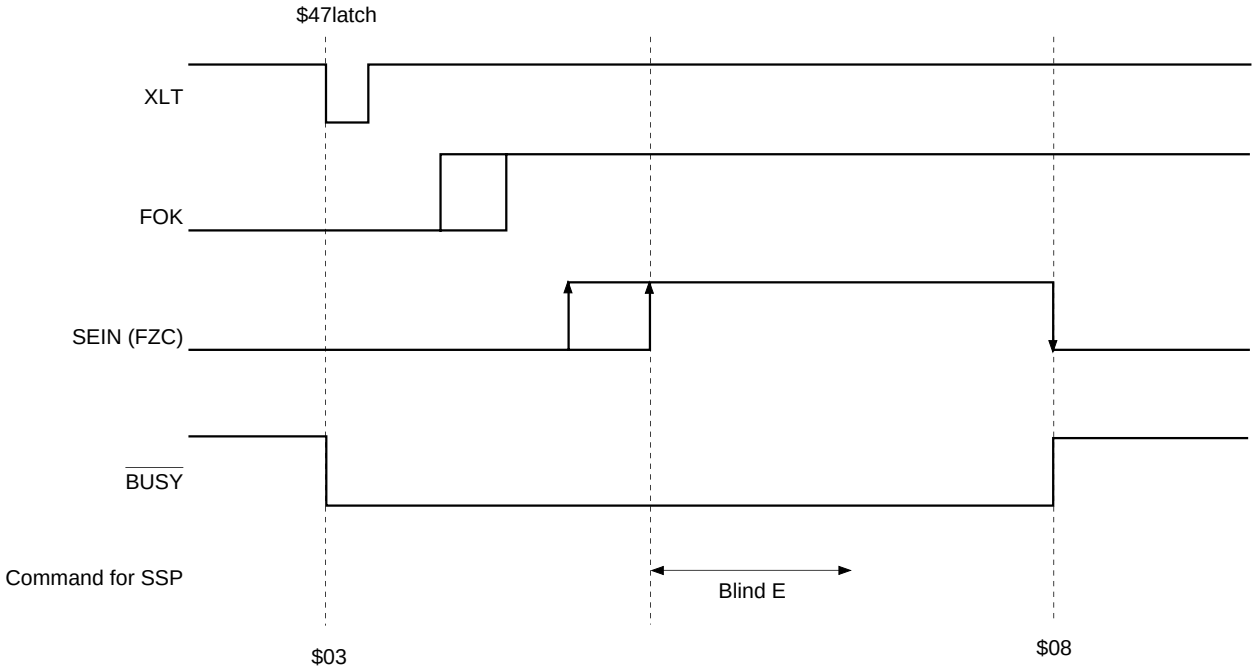


Fig. 4-3-(b). Auto Focus Timing Chart

(b) Track Jump

1, 10, and 2N-track jumps are performed respectively. Always use this when the focus, tracking, and sled servos are on. Note that tracking gain-up and braking-on should be sent beforehand because they are not involved in this sequence.

- 1-track jump
  When $48 ($49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 4-4. Set blind A and brake B with register 5.
- 10-track jump
  When $4A ($4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed in accordance with Fig. 4-5. The principal difference from the 1-track jump is to kick the sled. In addition, after kicking the actuator, when 5 tracks have been counted through CNIN, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the CNIN cycle becoming longer than the overflow C set with register 5), the tracking and sled servos are turned on.
- 2N-track jump
  When $4C ($4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 4-6. The track jump count N is set with register 7. Although N can be set to 2^{16} tracks, note that the setting is actually limited by the actuator. CNIN is used for counting the number of jumps.
  Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set with register 6.
- N-track move
  When $4E ($4F for REV) is received from the CPU, a FWD (REV) N-track move is performed in accordance with Fig. 4-7. N can be set to 216 tracks. CNIN is used for counting the number of jumps. This N-track move is executed only by moving the sled, and is therefore suited for moving across several thousand to several ten-thousand tracks.

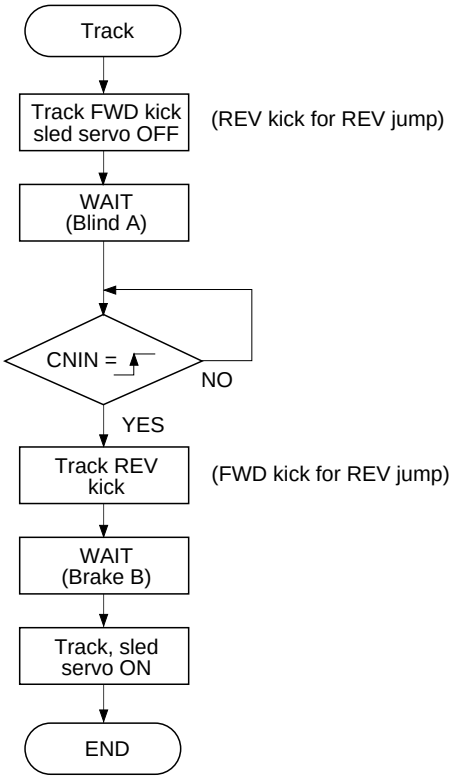


Fig. 4-4-(a). 1-Track Jump Flow Chart

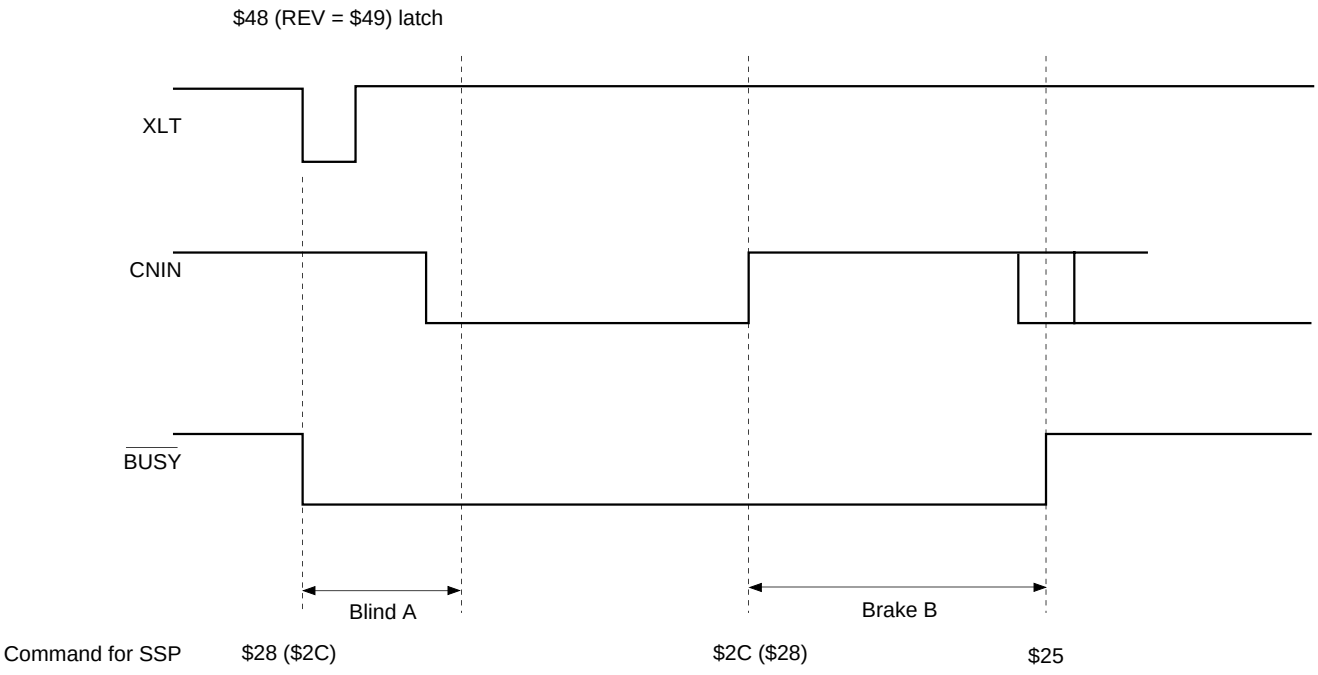


Fig. 4-4-(b). 1-Track Jump Timing Chart

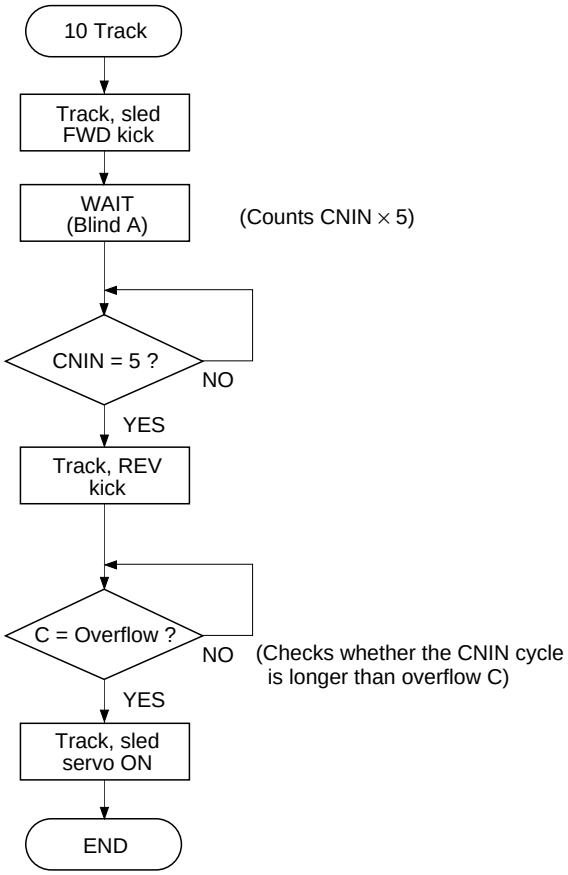


Fig. 4-5-(a). 10-Track Jump Flow Chart

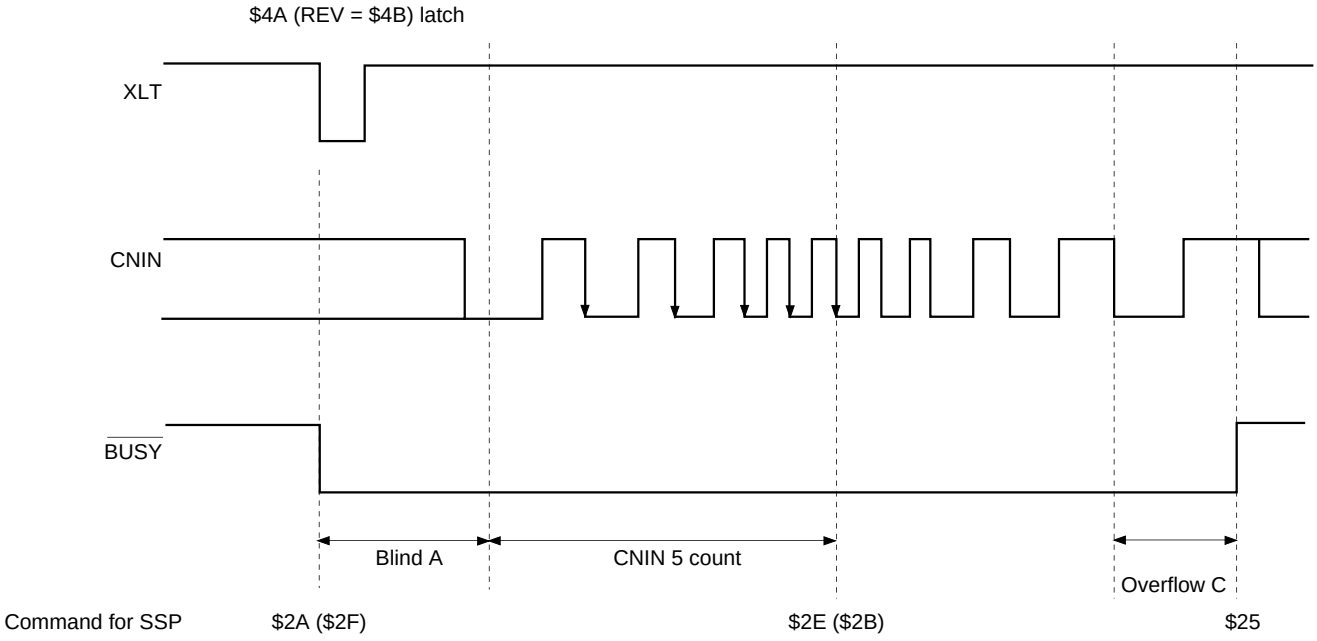


Fig. 4-5-(b). 10-Track Jump Timing Chart

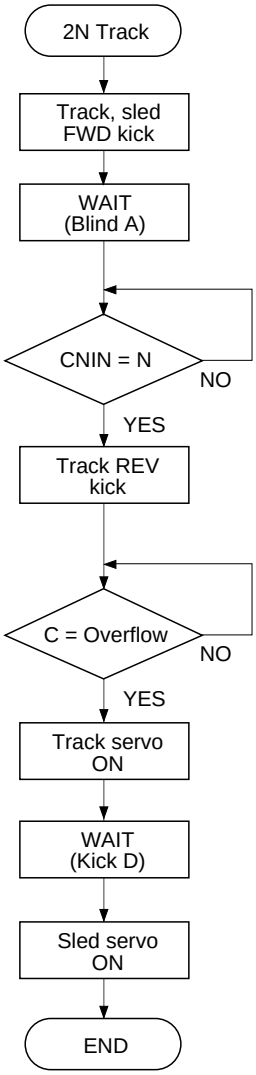


Fig. 4-6-(a). 2N-Track Jump Flow Chart

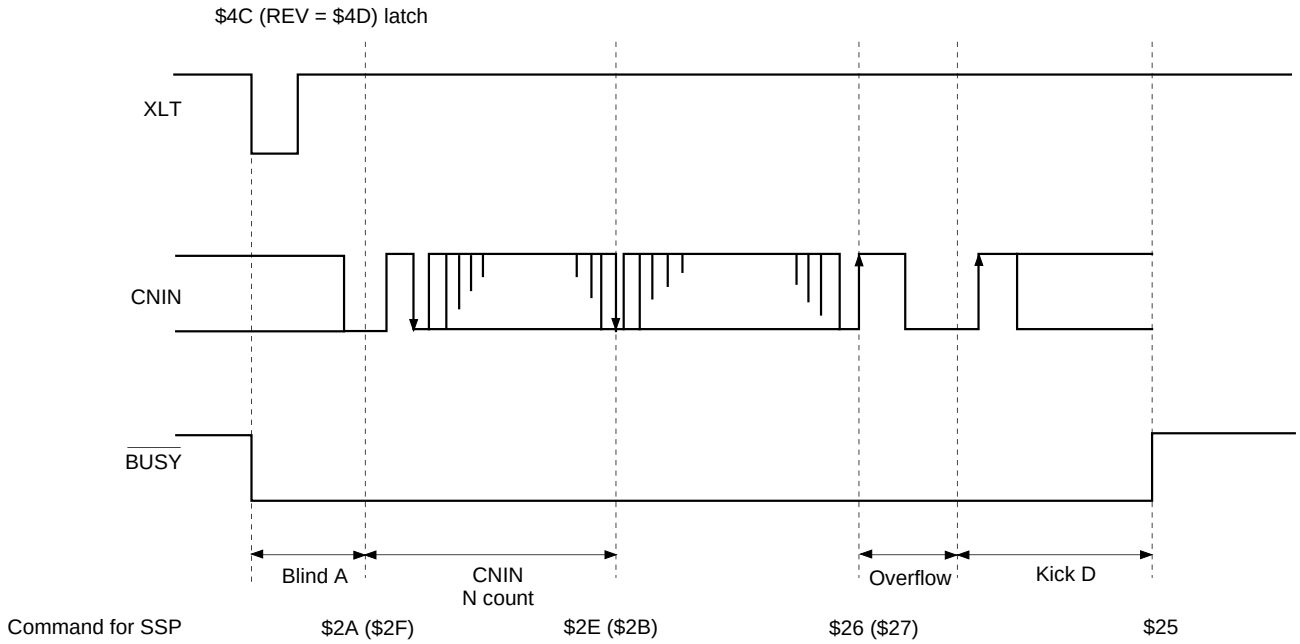


Fig. 4-6-(b). 2N-Track Jump Timing Chart

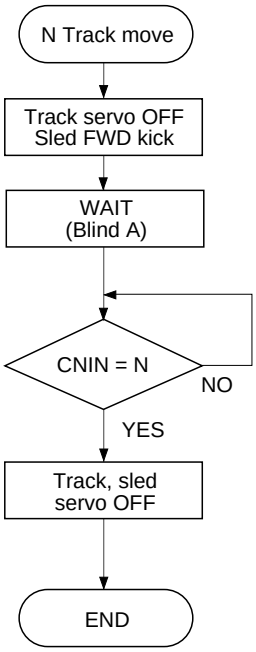


Fig. 4-7-(a). N-Track Move Flow Chart

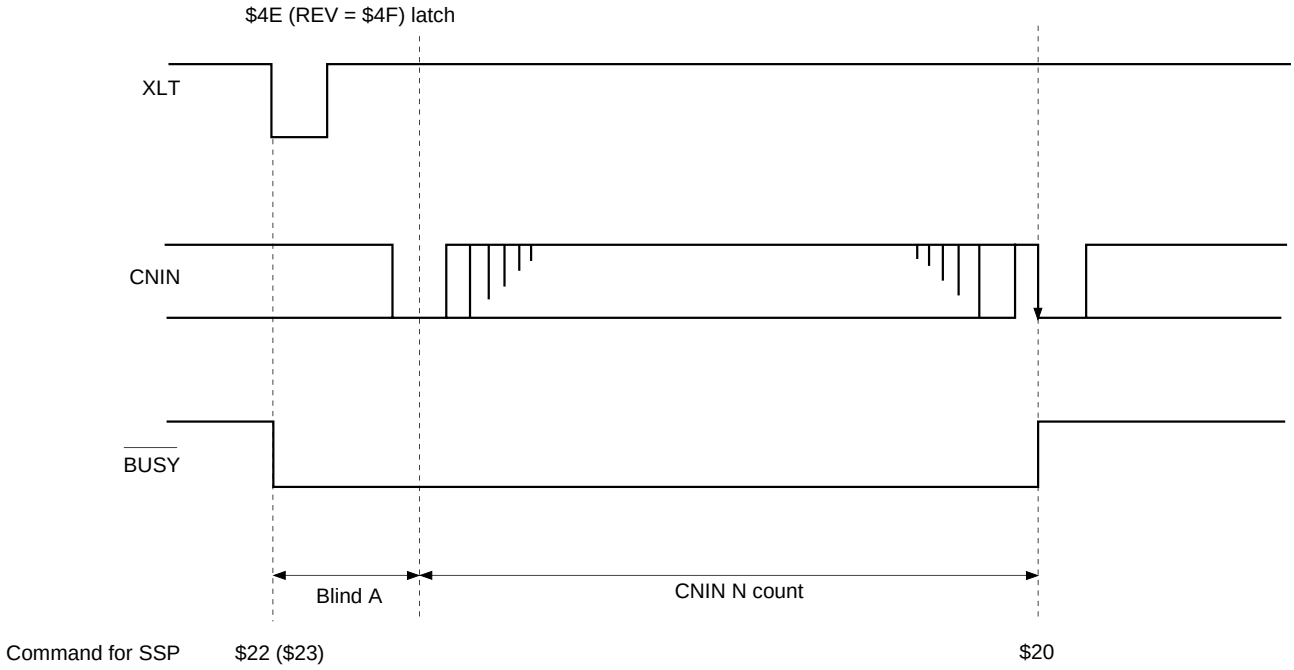
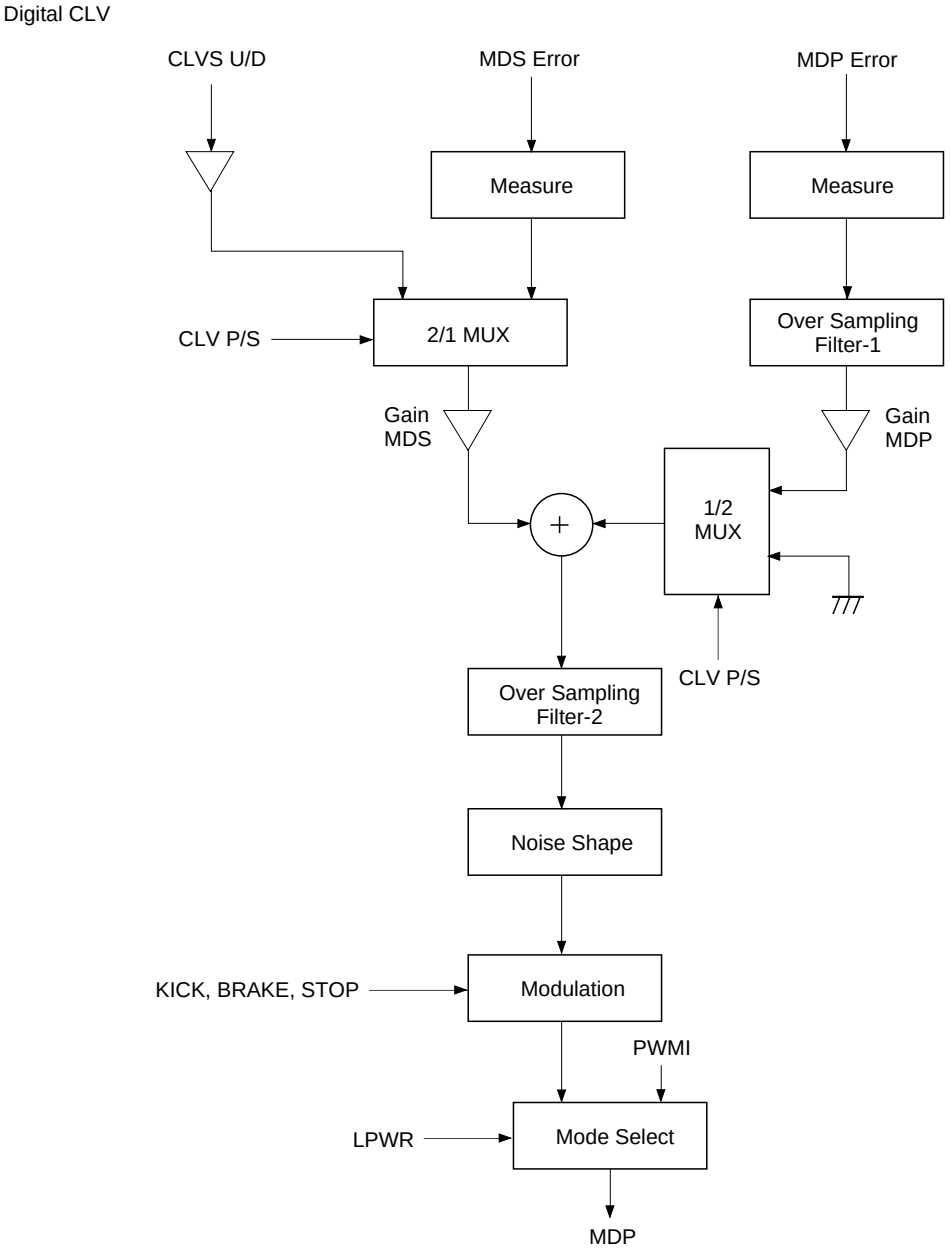


Fig. 4-7-(b). N-Track Move Timing Chart

4-7. Digital CLV

Fig. 4-8 shows the Block Diagram. Digital CLV outputs MDS error and MDP error signals with PWM, with the signal sampling frequency increased up to 130kHz during normal-speed playback in CLVS, CLVP and other modes.

In addition, the digital spindle servo gain is variable.



CLVS U/D: Up/down signal from CLVS servo
MDS error: Frequency error for CLVP servo
MDP error: Phase error for CLVP servo
PWMI: Spindle drive signal from the microcomputer for CAV servo

Fig. 4-8. Block Diagram

4-8. Asymmetry Compensation

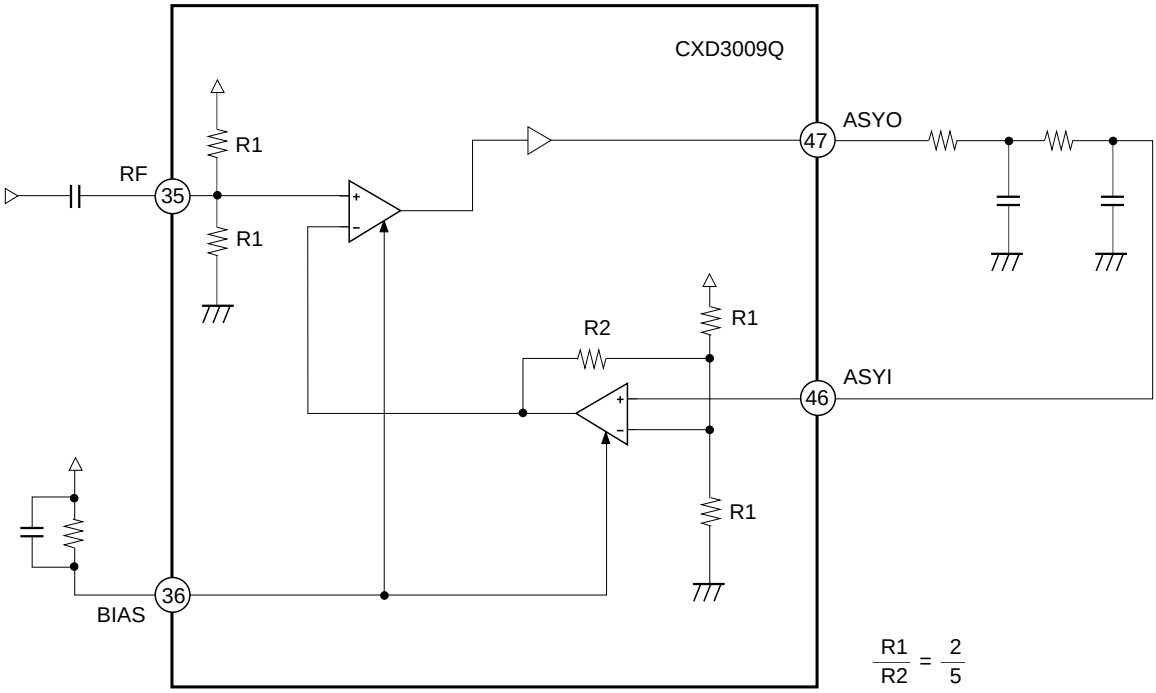


Fig. 4-9. Example of Asymmetry Compensation Application Circuit

4-9. CD-TEXT Data Demodulation

- In order to demodulate the CD-TEXT data, set Data 6 D3 TXON command of $8 to 1.
  During TXON = 1, the EXCK pin should be set to low and the SBSO output data should not be used because the CD-TEXT demodulation circuit uses EXCK and SBSO exclusively.
  It requires 26.7ms (max.) to demodulate the CD-TEXT data properly after TXON is set to 1.
- The CD-TEXT data is output after the SQSO pin is switched by the command. The CD-TEXT data can be output by setting Data 6 D2 TXOUT command of $8 to 1. The readout clock should be input to SQCK in order to read the data.
- The data which can be read out is the CRC calculation results for each pack (CRC), CD-TEXT data excluding CRC data (16 bytes).
- When the CD-TEXT data is read, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of bytes is the same, the bits within the bytes are now ordered LSB first.
- The data which can be stored in the IC is for 1 packet (4 packs).

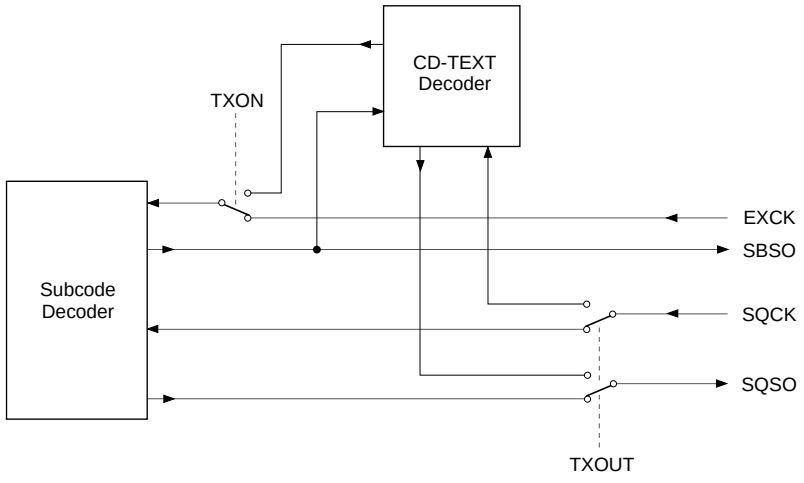


Fig. 4-10. CD-TEXT Demodulation Circuit Block Diagram

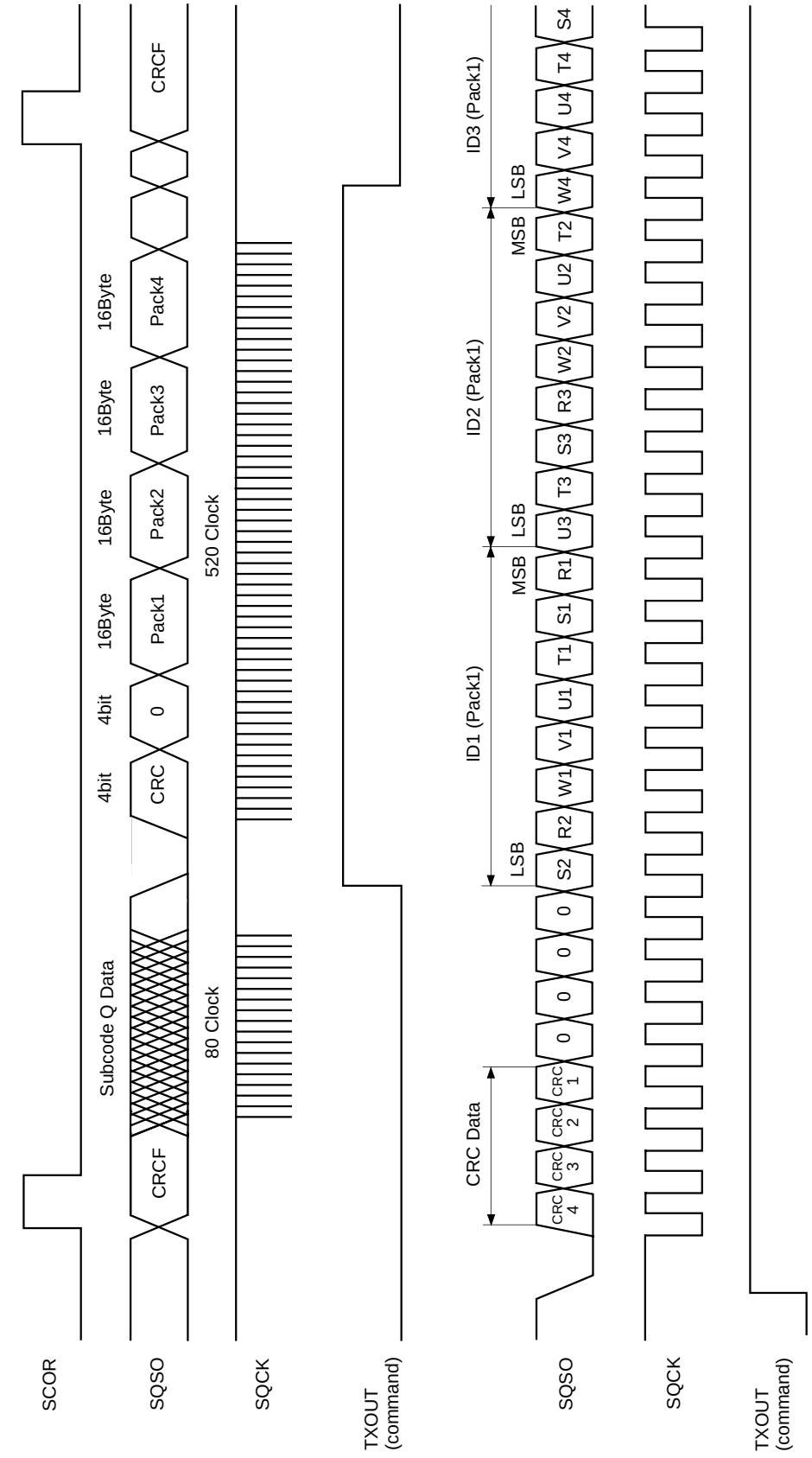


Fig. 4-11. CD-TEXT Data Timing Chart

5. 1bit DAC Block

5-1. DAC Block Input Timing

Timing Chart 5-1 shows the input timing for the DAC block.

The data from the CD signal processor block to the DAC block can be connected inside the IC by setting the OUTL command of $8X to 1. Set OUTL1 to 0 when the data is send to the DAC block via the audio DSP and the like.

5-2. Description of DAC Block Functions

Zero data detection

When the condition where the lower 4bits of the input data are DC and the remaining upper bits are all "0" or all "1" has continued for approximately 300ms, zero data is detected. Zero data detection is performed independently for the left and right channels.

Mute flag output

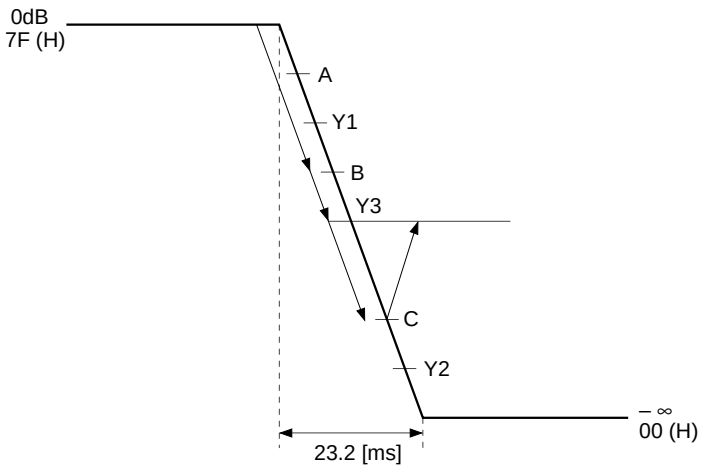
The LMUT and RMUT pins go active when any one of the following conditions is met.

The polarity can be selected by the ZDPL command of $9X.

- When zero data is detected
- When a high signal is input to the SYSM pin
- When the SMUT command of $AX is set

Attenuation operation

Assuming attenuation data X1, X2 and X3 (X1 > X3 > X2), the corresponding audio outputs are Y1, Y2 and Y3 (Y1 > Y3 > Y2). First, X1 is sent, followed by X2. If X2 is sent before X1 reaches Y1 (A in the figure), X1 continues approaching Y2. Next, if X3 is sent before X1 reaches Y2 (B or C in the figure), X1 then approaches Y3 from the value (B or C in the figure) at that point.

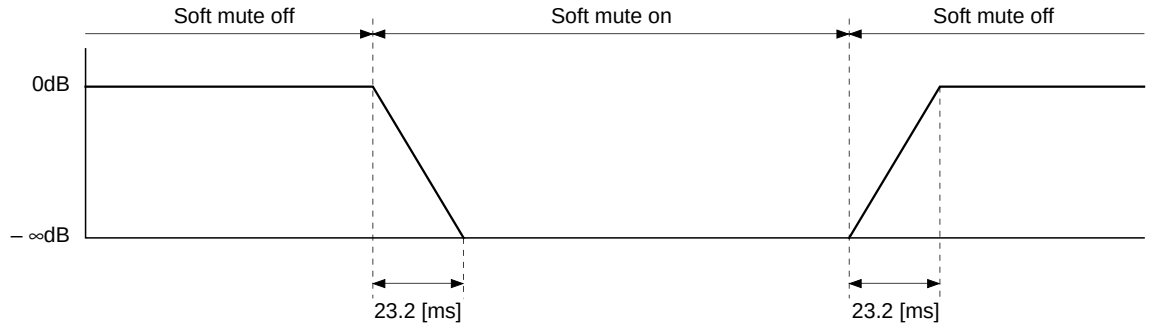


DAC block mute operation

Soft mute

Soft mute results and the input data is attenuated to zero when any one of the following conditions is met.

- When attenuation data of "000" (high) is set
- When the SMUT command of $AX is set to 1
- When a high signal is input to the SYSM input pin



Forced mute

Forced mute results when the FMUT command of $AX is set to 1.

Forced mute fixes the PWM output that is input to the LPF block to low.

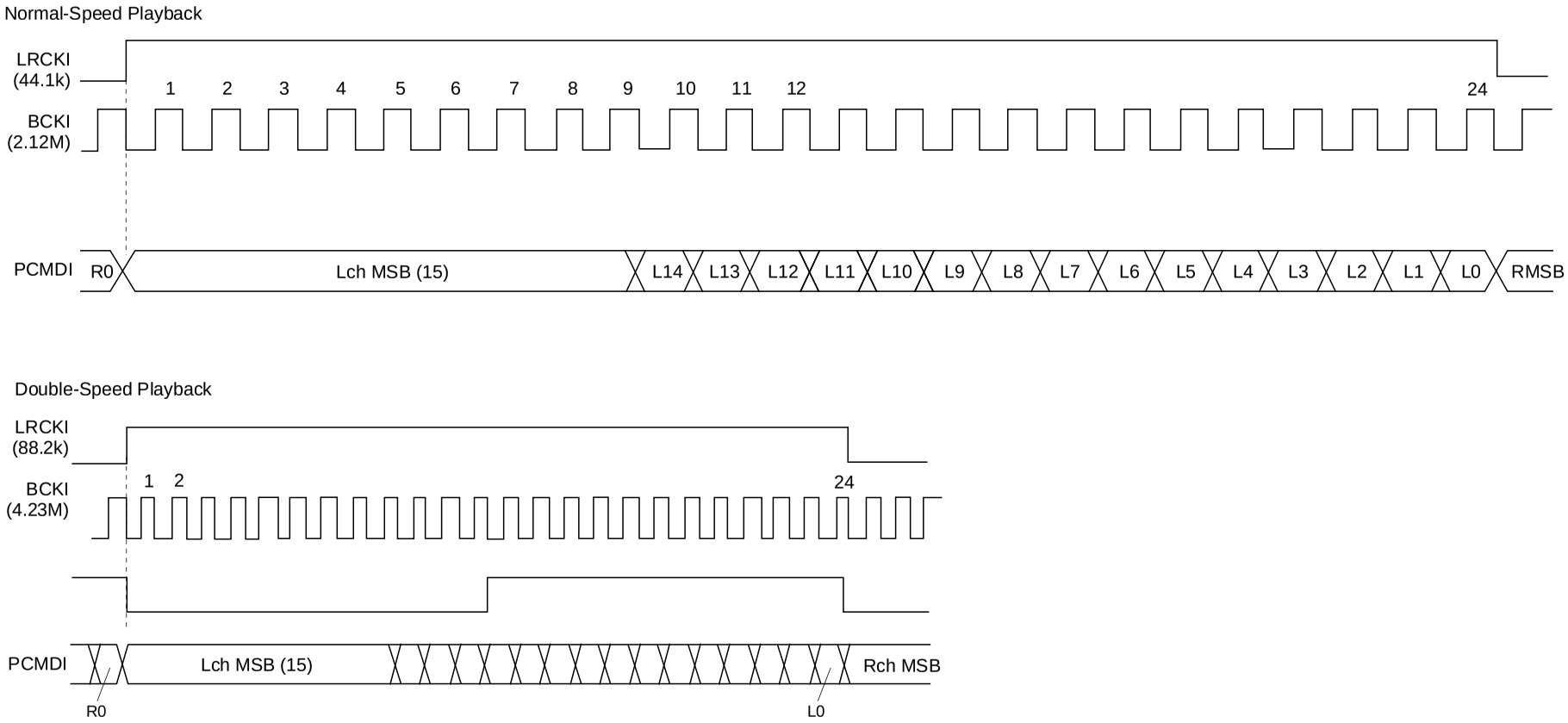
* When setting FMUT, set OPSL2 to 1. (See the $AX commands.)

Zero detection mute

Forced mute is applied when the ZMUT command of $9X is set to 1 and the zero data is detected for the left and right channels.

(See "Zero data detection".)

Timing Chart 5-1



Input Timing for DAC Block

LRCK Synchronization

Synchronization is performed at the first falling edge of the LRCK input during reset.

After that, synchronization is lost when the LRCK input frequency changes and resynchronization must be performed.

The LRCK input frequency changes when the master clock of the LSI is switched and the playback speed changes such as the following cases.

- When the XTSL pin switches between high and low
- When the DSPB command of $9X setting changes
- When the MCSL command of $9X setting changes

LRCK switching may also be performed if there are other ICs between the CD-DSP block and the DAC block. Resynchronization must be performed in this case as well.

For resynchronization, set the LRWO command of $AX to 1, wait for one LRCK cycle or more, and then set LRWO to 0.

* When setting LRWO, set OPSL2 to 1. (See the $AX commands.)

SYCOF

When LRCK, PCMD and BCK are connected directly with LRCKI, PCMDI and BCKI, respectively, playback can be performed easily in CAV-W mode by setting SYCOF of address 9 to 1.

Normally, the memory proof, etc., is used for playback in CAV-W mode.

In CAV-W mode, the LRCK output conforms not to the crystal but to the VCO. Therefore, synchronization is frequently lost.

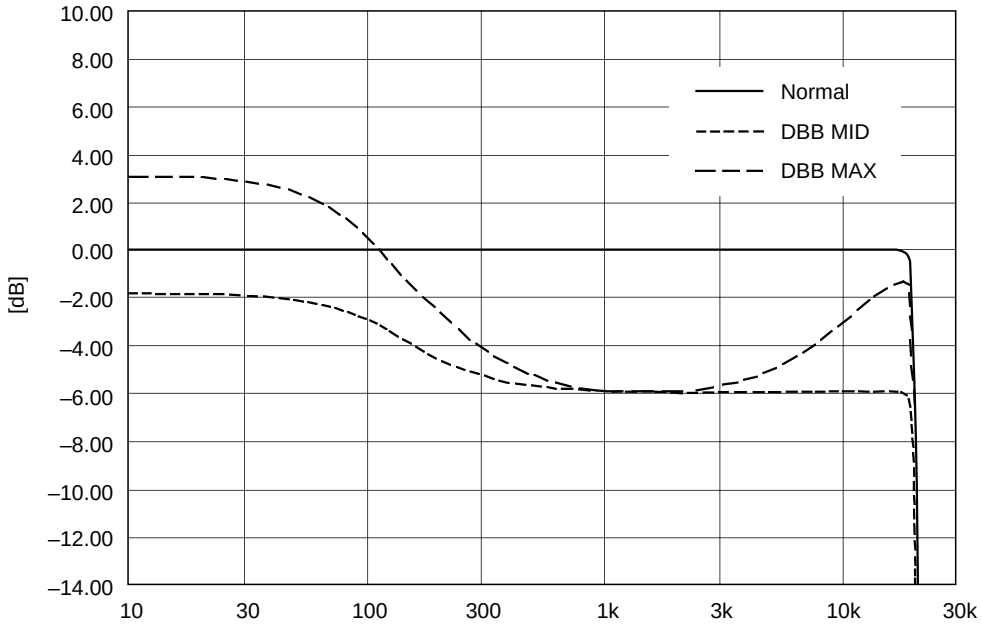
Setting SYCOF of address 9 to 1 ignores that the LRCKI input synchronization is lost, facilitating playback. However, the playback is not perfect because pre-value hold or data skip occurs due to the wow flutter in the LRCKI input.

* Set SYCOF to 0 except when connecting LRCK, PCMD and BCK directly with LRCKI, PCMDI and BCKI, respectively, and performing playback in CAV-W mode.
* Set SYCOF to 0 in advance when LRCK resynchronization is applied with LRWO=1.

Digital Bass Boost

Bass boost without external parts is possible using the built-in digital filter. The boost strength has two levels: Mid. and Max. BSBST and BBSL of address A are used for the setting.

See Graph 5-2 for the digital bass boost frequency response.



Digital Bass Boost Frequency Response [Hz]

Graph 5-2.

6. LPF Block

The CXD3009Q contains an initial-stage secondary active LPF with numerous resistors and capacitors and an operational amplifier with reference voltage.
The resistors and capacitors are attached externally, allowing the cut-off frequency fc to be determined flexibly.
The reference voltage (V_C) is (AV_{DD} – AV_{SS})/2.

The LPF block application circuit is shown below.
In this circuit, the cut-off frequency is fc ≈ 40kHz.

The external capacitors' values when fc = 30kHz and 50kHz are noted below as a reference.
The resistors' values do not change at this time.

- When fc ≈ 30kHz:
  C1 = 200pF, C2 = 910pF
- When fc ≈ 50kHz:
  C1 = 120pF, C2 = 560pF

LPF Block Application Circuit

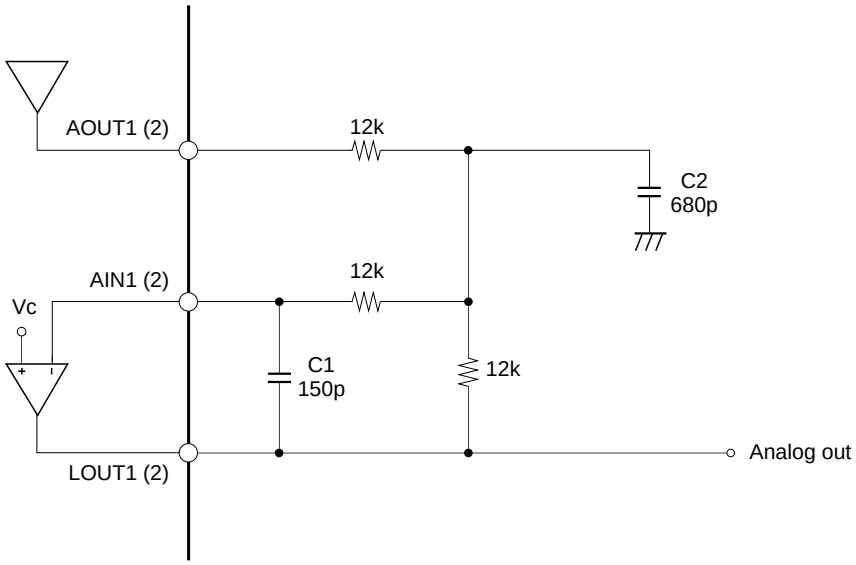


Fig. 6-1. LPF External Circuit

7. Setting Method of the CXD3009Q Playback Speed (in CLV-N mode)

(A) CD-DSP block

The playback modes shown below can be selected by the combination of the crystal, XTSL pin and DSPB command of $9X.

CD-DSP block playback speed

X'tal	XTSL	DSPB	CD-DSP block playback speed
768Fs	1	0	1×
768Fs	1	1	2×
384Fs	0	0	1×
384Fs	0	1	2×
384Fs	1	1	1×*1

Fs = 44.1kHz

*1 Low power consumption mode. The CD-DSP processing speed is halved, allowing the power consumption to be decreased.

(B) 1-bit DAC block

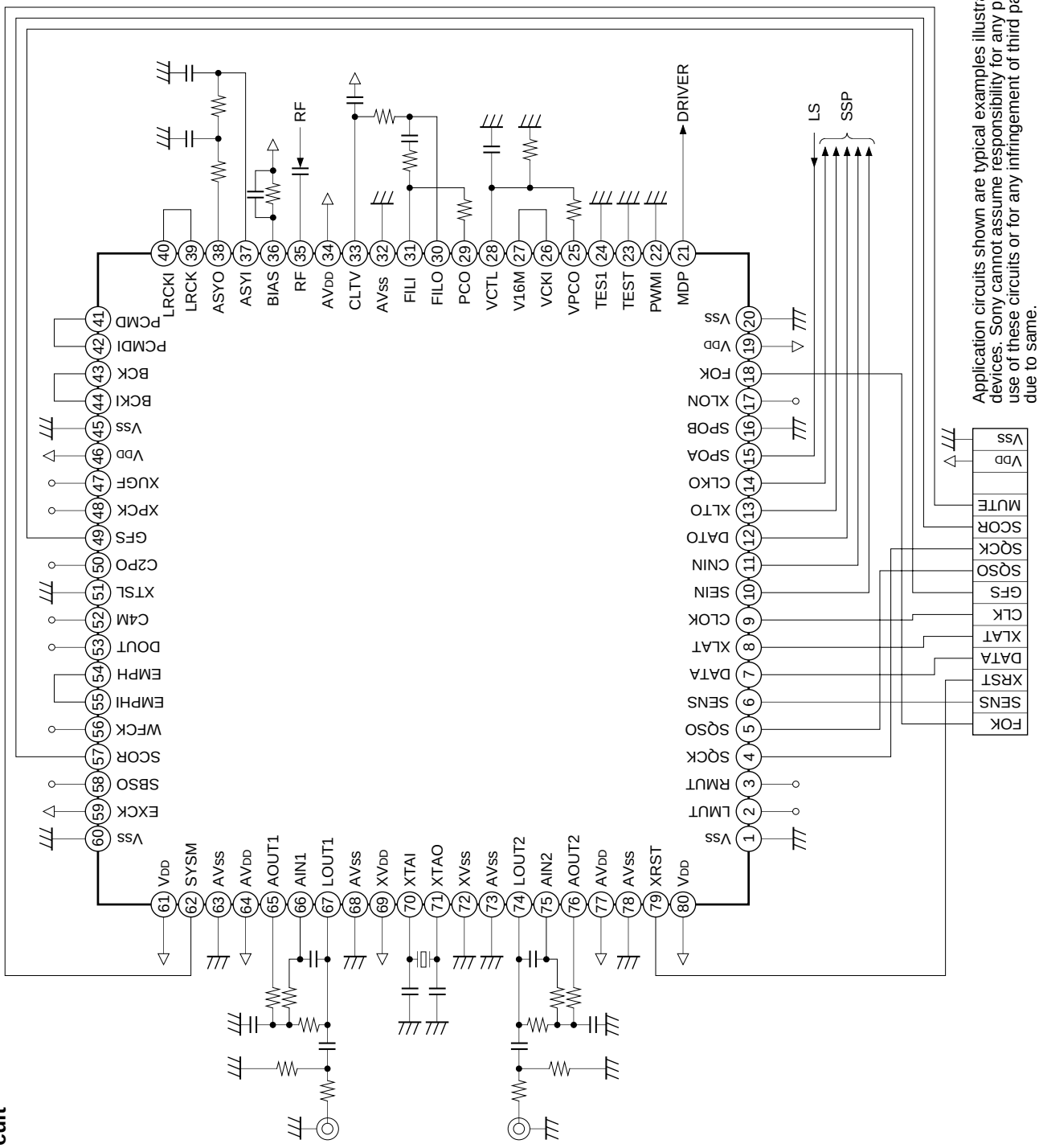
The operating speed of the DAC block is determined by the crystal and the MCSL command of $9X regardless of the operating conditions of the CD-DSP block mentioned above. This allows the playback mode for the DAC block and CD-DSP block to be set independently.

1-bit DAC block playback speed

X'tal	MCSL	DAC block playback speed
768Fs	1	1×
768Fs	0	2×
384Fs	0	1×

Fs = 44.1kHz

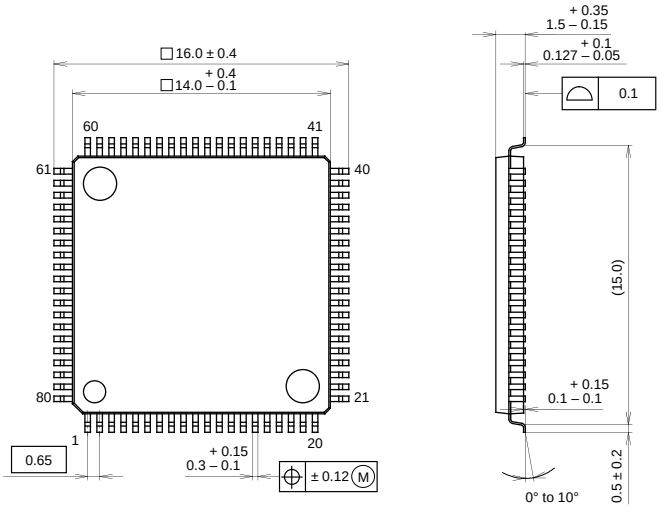
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

80PIN QFP (PLASTIC)

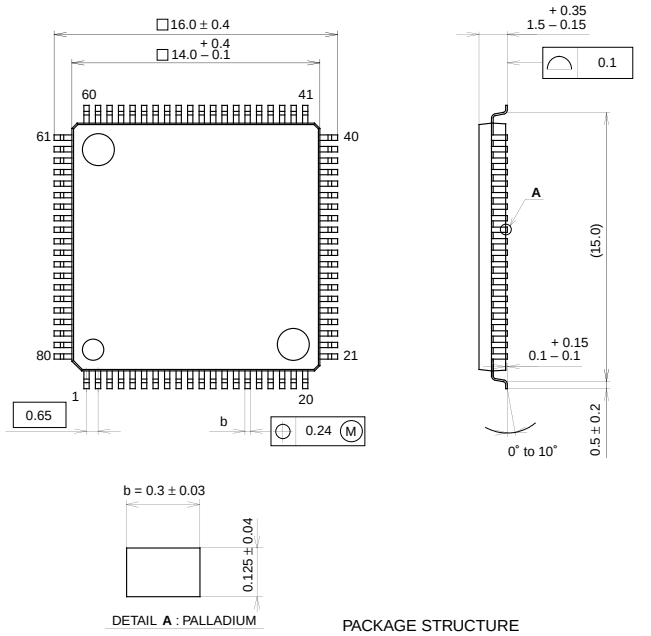


PACKAGE STRUCTURE

SONY CODE	QFP-80P-L03
EIAJ CODE	LQFP080-P-1414
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.6g

80PIN QFP (PLASTIC)

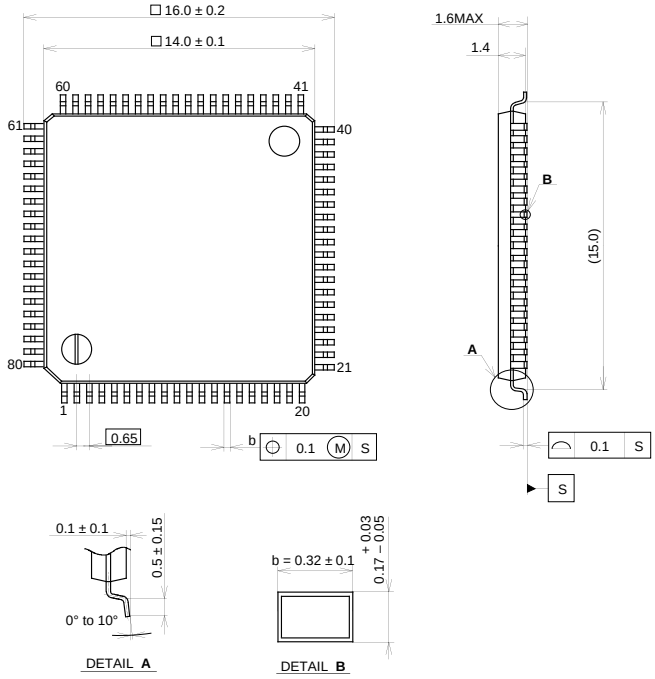


PACKAGE STRUCTURE

SONY CODE	QFP-80P-L03
EIAJ CODE	P-QFP80-14x14-0.65
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.6g

80PIN QFP (PLASTIC)



SONY CODE	QFP-80P-L052
EIAJ CODE	P-QFP80-14X14-0.65
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	1.6 g