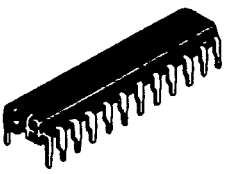
HM6207 Series

T-46-23-05

262144-word x 1-bit High Speed CMOS Static RAM

The Hitachi HM6207 is a high speed 256k static RAM organized as 256-kword x 1-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU. The HM6207, packaged in a 300 mil plastic DIP, is available for high density mounting.

Low power version retains the data with battery back up.



(DP-24NC)

Features

- High Speed: Fast Access Time 35/45 ns (max.)
- Low Power
  - Standby: 100 μW (typ.)/30 μW (typ.) (L-version)
  - Operation: 300 mW (typ.)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static Memory:
  - No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)

Ordering Information

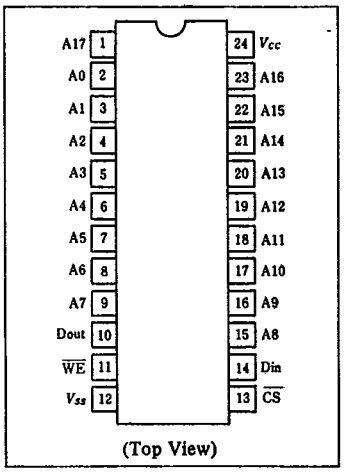
Type No.	Access Time	Package
HM6207P-35	35 ns	300-mil 24-pin Plastic DIP
HM6207P-45	45 ns	
HM6207LP-35	35 ns	
HM6207LP-45	45 ns	

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Storage Temperature under bias	Tbias	−10 to +85	°C

Note) *1. −2.5V for pulse width ≦ 10ns.

Pin Arrangement

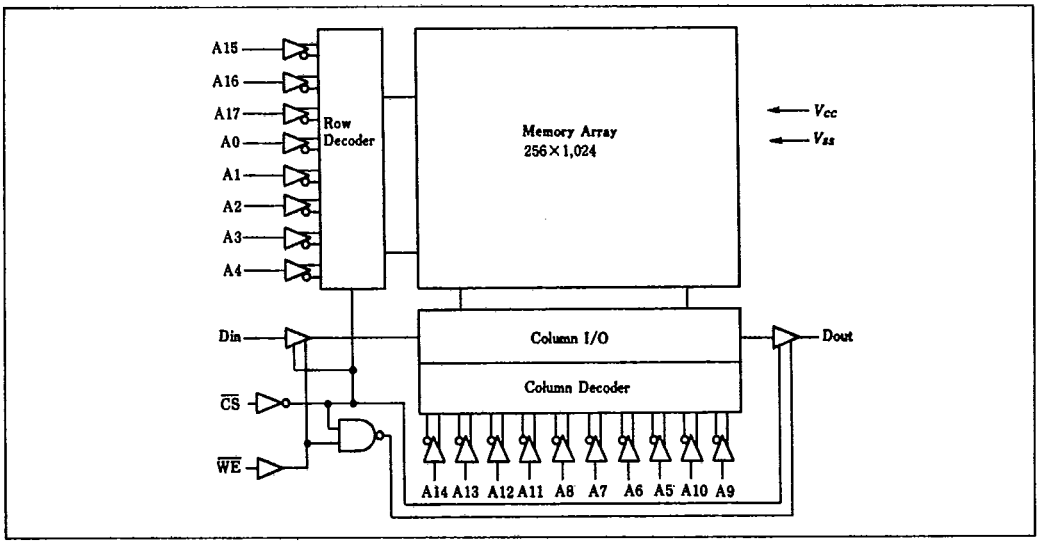


(Top View)

Pin Description

Pin Name	Function
A0 - A17	Address
Din	Data Input
Dout	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	X	NOT SELECTED	I_{SB}, I_{SB1}	HIGH-Z	---
L	H	READ	I_{CC}	Dout	READ CYCLE
L	L	WRITE	I_{CC}	HIGH-Z	WRITE CYCLE

Note) X means don't care.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −2.0V for pulse width ≦ 10 ns

DC and Operating Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	min	typ*1	max	Unit	Test Condition
Input Leakage Current	$\|I_{LI}\|$	–	–	2.0	μA	V_{CC} = MAX. V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10.0	μA	$\overline{CS}$ = V_{IH} Vout = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	60	100	mA	$\overline{CS}$ = V_{IL} Iout = 0mA, min. cycle
Standby Power Supply Current	I_{SB}	–	15	30	mA	$\overline{CS}$ = V_{IH}, min. cycle
Standby Power Supply Current (1)	I_{SB1}	–	0.02	2.0	mA	$\overline{CS}$ ≧ V_{CC}−0.2V, 0V≦ V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC}−0.2V
		–	0.006*2	0.1*2		
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4.0mA

Note) *1. Typical limits are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0MHz)

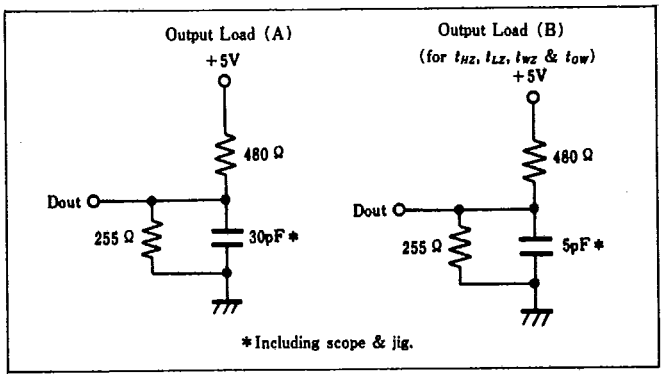
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Capacitance	Cin	–	–	6.0	pF	Vin = 0V
Output Capacitance	Cout	–	–	10	pF	Vout = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

AC Test Conditions

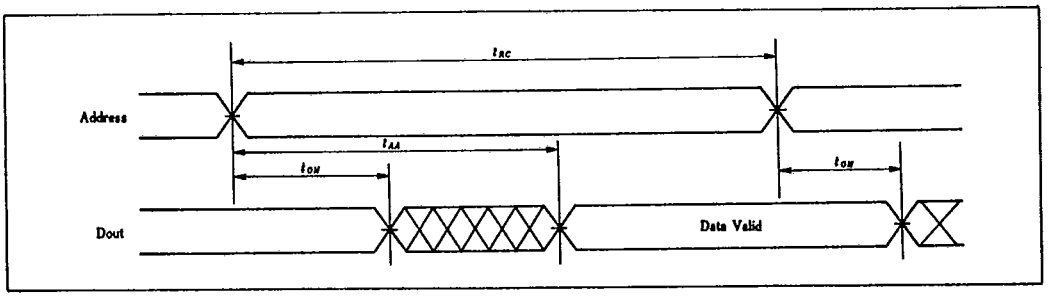
- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 5ns
- Input and Output timing reference levels: 1.5V
- Output load: See Figures.



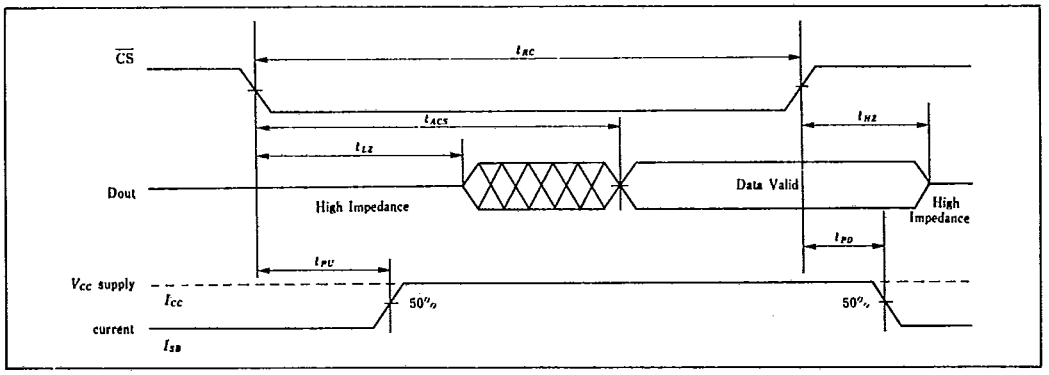
Read Cycle

Parameter	Symbol	HM6207-35		HM6207-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	35	–	45	–	ns	*1
Address Access Time	t_{AA}	–	35	–	45	ns	
Chip Select Access Time	t_{ACS}	–	35	–	45	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	*2, *3, *7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	*2, *3, *7
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	*7
Chip Deselection to Power Down Time	t_{PD}	–	30	–	40	ns	*7

Timing Waveform of Read Cycle No. 1 *4, *5



Timing Waveform of Read Cycle No. 2*4,*6

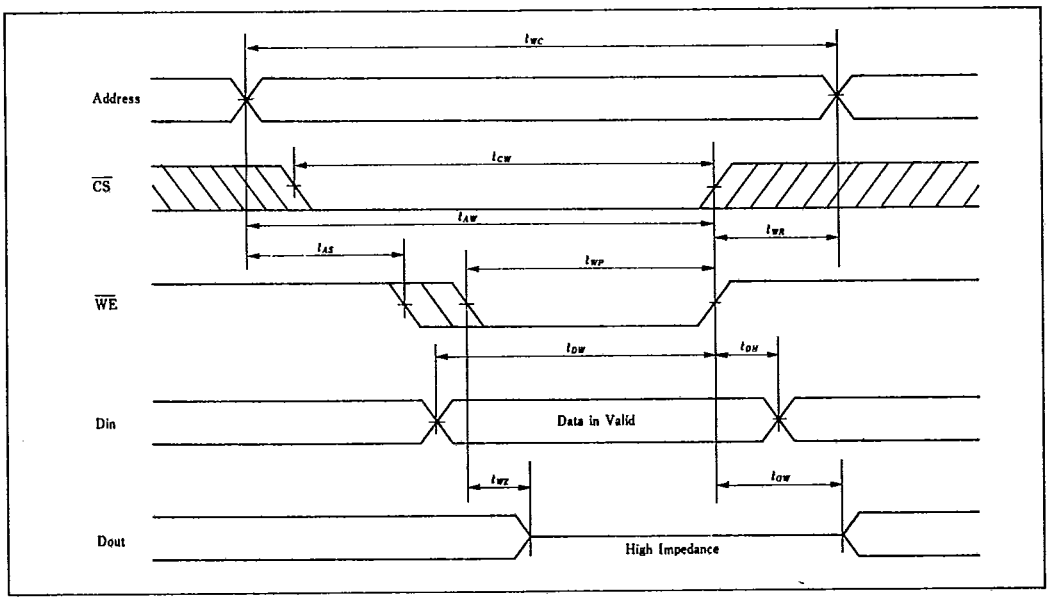


Notes) *1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
*2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
*3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
*4. $\overline{WE}$ is high for READ Cycle.
*5. Device is continuously selected, while $\overline{CS}$ = V_{IL}.
*6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
*7. This parameter is sampled and not 100% tested.

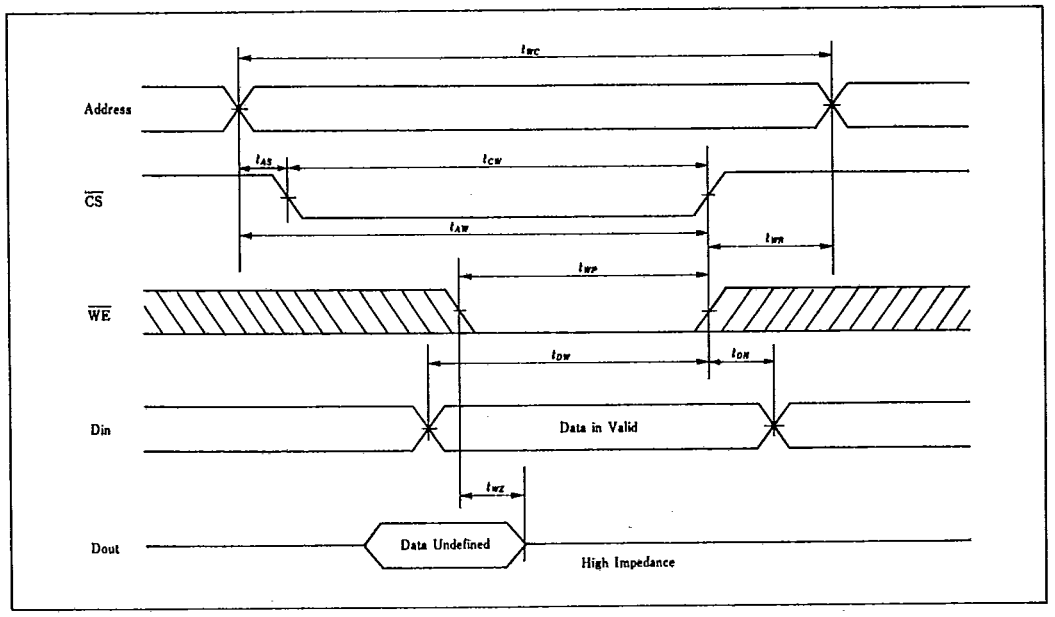
Write Cycle

Parameter	Symbol	HM6207-35		HM6207-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	–	45	–	ns	*2
Chip Selection to End of Write	t_{CW}	30	–	40	–	ns	
Address Valid to End of Write	t_{AW}	30	–	40	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	25	–	ns	
Write Recovery Time	t_{WR}	3	–	3	–	ns	
Data Valid to End of Write	t_{DW}	20	–	20	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	20	0	25	ns	*3, *4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	*3, *4

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes) *1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
*2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
*3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
*4. This parameter is sampled and not 100% tested.

T-46-23-05

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)
(This characteristics is guaranteed only for L-version)

Parameter	Symbol	min	typ.	max.	Unit	Test Condition
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geqq V_{CC} - 0.2V$, $V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$
Data Retention Current	I_{CCDR}	–	2	50*2	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	See retention waveform
Operation Recovery Time	t_R	t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time *2. V_{CC} = 3.0V

Low V_{CC} Data Retention Waveform