HIGH-PERFORMANCE CMOS BUS TRANSCEIVERS

IDT54/74FCT861-64B

FEATURES:

- **35% faster than AMD's Am29861-64 series**
- Equivalent to AMD's Am29861-64 bipolar registers in pinout/function and output drive over full temperature and voltage supply extremes
- High-speed symmetrical bidirectional transceivers
  — Non-inverting t_{PD} = 3.5ns typ.
  — Inverting t_{PD} = 4.0ns typ.
- 48mA commercial I_{OL}, 32mA military I_{OL}
- 200mV (typ.) hysteresis on T and R buses
- Clamp diodes on all inputs for ringing suppression
- ESD protection 5000V (typ.) — MIL-STD-883 Category B
- Low input/output capacitance
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

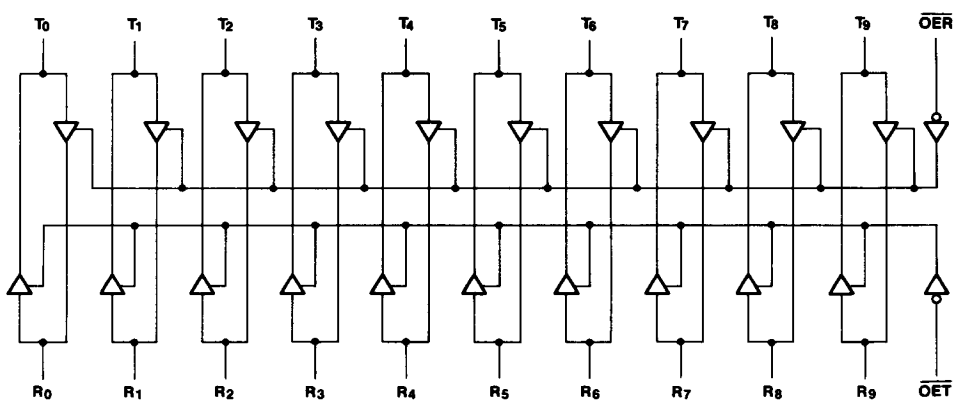
The IDT54/74FCT800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT860 Series bus transceivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The IDT54/74FCT863B and IDT54/74FCT864B 9-bit transceivers have NORed output enables for maximum control flexibility.

All of the IDT54/74FCT800B high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes, and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT861B/IDT54/74FCT862B 10-BIT TRANSCEIVERS



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PRODUCT SELECTOR GUIDE

	DEVICE	
	10-BIT	9-BIT
Non-inverting	IDT54/74FCT861B	IDT54/74FCT863B
Inverting	IDT54/74FCT862B	IDT54/74FCT864B

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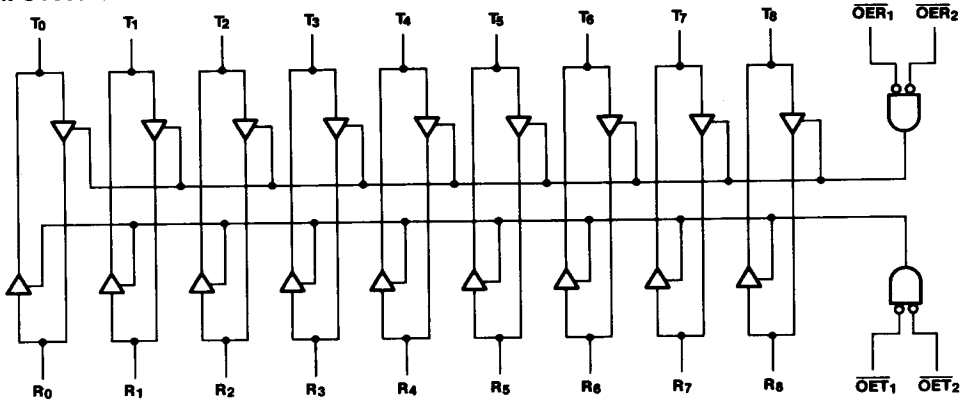
FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT863B/IDT54/74FCT864B 9-BIT TRANSCEIVERS



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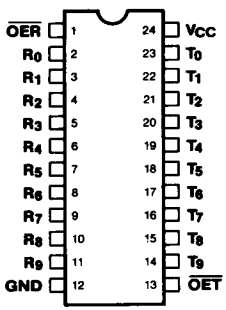
PIN CONFIGURATIONS

IDT54/74FCT861B/IDT54/74FCT862B 10-BIT TRANSCEIVERS



DIP
TOP VIEW

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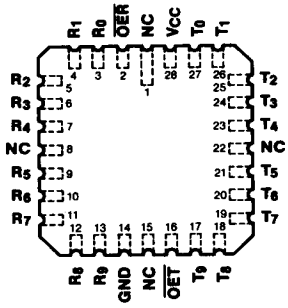

LCC
TOP VIEW

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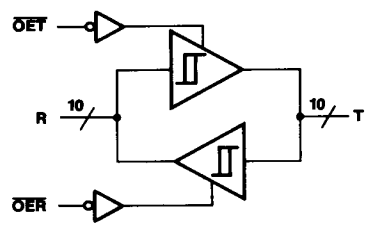
LOGIC SYMBOLS

IDT54/74FCT861B



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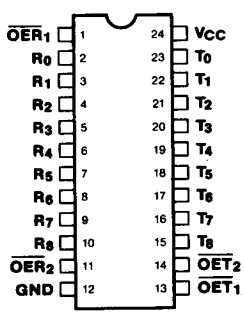
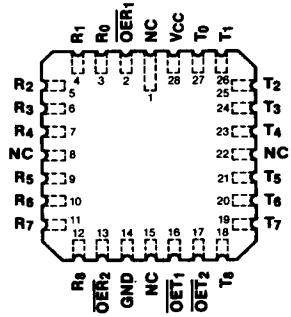
IDT54/74FCT863B/IDT54/74FCT864B 9-BIT TRANSCEIVERS



DIP
TOP VIEW

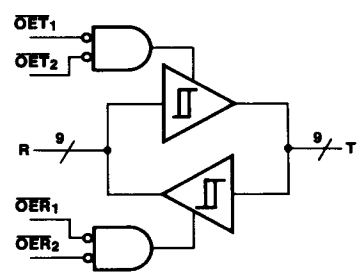
SSD39C861-007



LCC
TOP VIEW

SSD39C861-008

IDT54/74FCT863B



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PIN DESCRIPTION

NAME	I/O	DESCRIPTION
IDT54/74FCT861/62B		
$\overline{OER}$	I	When LOW in conjunction with $\overline{OET}$ HIGH activates the RECEIVE mode.
$\overline{OET}$	I	When LOW in conjunction with $\overline{OER}$ HIGH activates the TRANSMIT mode.
R_i	I/O	10-bit RECEIVE input/output.
T_i	I/O	10-bit TRANSMIT input/output.
IDT54/74FCT863/64B		
$\overline{OER}_i$	I	When LOW in conjunction with $\overline{OET}_i$ HIGH activates the RECEIVE mode.
$\overline{OET}_i$	I	When LOW in conjunction with $\overline{OER}_i$ HIGH activates the TRANSMIT mode.
R_i	I/O	9-bit RECEIVE input/output.
T_i	I/O	9-bit TRANSMIT input/output.

FUNCTION TABLES

IDT54/74FCT861B/IDT54/74FCT863B (Non-inverting)

INPUTS				OUTPUTS		FUNCTION
OER	OER	R_i	T_i	R_i	T_i	
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	Hi-Z

H = HIGH
L = LOW
Z = High Impedance
X = Don't Care
N/A = Not Applicable

IDT54/74FCT862B/IDT54/74FCT864B (Inverting)

INPUTS				OUTPUTS		FUNCTION
OER	OER	R_i	T_i	R_i	T_i	
L	H	L	N/A	N/A	H	Transmitting
L	H	H	N/A	N/A	L	Transmitting
H	L	N/A	L	H	N/A	Receiving
H	L	N/A	H	L	N/A	Receiving
H	H	X	X	Z	Z	Hi-Z

H = HIGH
L = LOW
Z = High Impedance
X = Don't Care
N/A = Not Applicable

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
V_I	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-75	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -250µA	V_{HC}	V_{CC}	—	
			I_{OH} = -15mA MIL.	2.4	4.0	—	
			I_{OH} = -24mA COM.	2.0	3.5	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	—	0.5	
			I_{OL} = 48mA COM.	—	—	0.5	
V_H	Input Hysteresis on R_i and T_i	—		—	200	—	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

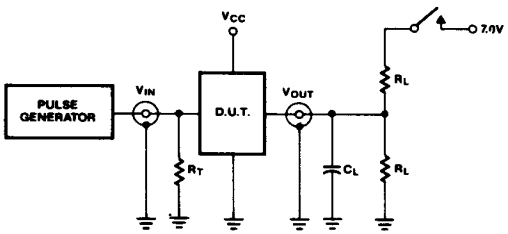
PARAMETERS	DESCRIPTION	TEST CONDITIONS[1]	COMMERCIAL		MILITARY		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay from R_i to T_i or T_i to R_i IDT54/74FCT861B/IDT54/74FCT863B (Non-inverting)	C_L = 50pF R_L = 500Ω	—	5.0	—	6.5	ns
t_{PLH} t_{PHL}		C_L = 300pF R_L = 500Ω	—	5.0	—	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay from R_i to T_i or T_i to R_i IDT54/74FCT862B/IDT54/74FCT863B (Inverting)	C_L = 50pF R_L = 500Ω	—	5.5	—	6.5	ns
t_{PLH} t_{PHL}		C_L = 300pF R_L = 500Ω	—	5.5	—	6.5	ns
t_{ZH} t_{ZL}	Output Enable Time OET to T_i or OER to R_i	C_L = 50pF R_L = 500Ω	—	8.0	—	9.0	ns
t_{ZH} t_{ZL}		C_L = 300pF R_L = 500Ω	—	8.0	—	9.0	ns
t_{ZH}[2] t_{ZL}	Output Enable Time OET to T_i or OER to R_i	C_L = 5pF R_L = 500Ω	—	7.0	—	8.0	ns
t_{ZH} t_{ZL}		C_L = 50pF R_L = 500Ω	—	7.0	—	8.0	ns

NOTE:

1. See test circuit and waveforms.
2. This parameter guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR THREE-STATE OUTPUTS



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SWITCH POSITION

TEST	SWITCH
t_{LZ}	Closed
t_{ZL}	Closed
All Other	Open

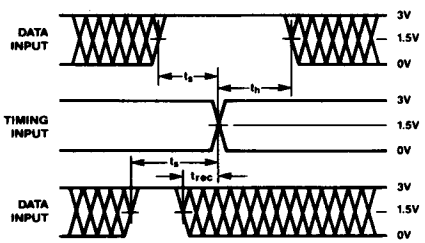
DEFINITIONS

R_L = Load resistor: see AC CHARACTERSICS for value.

C_L = Load capacitance includes jig and probe capacitance: see AC CHARACTERISTICS for value.

R_T = Termination should be equal to Z_{OUT} of pulse generators.

SET-UP, HOLD, AND RELEASE TIMES



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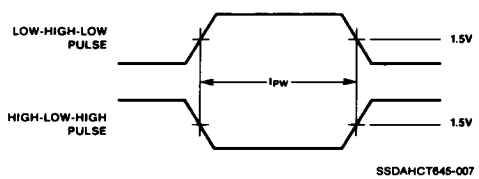
PULSE WIDTH



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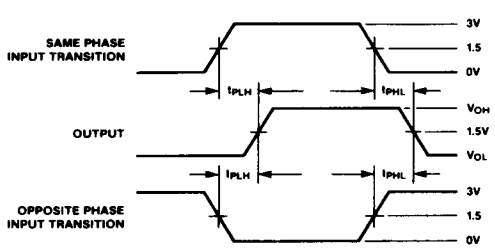
PROPAGATION DELAY



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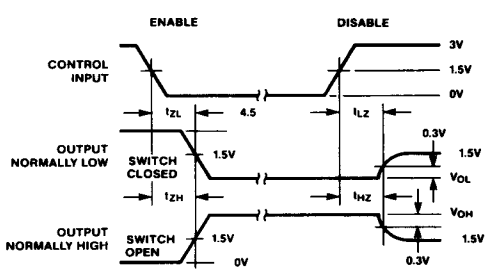
ENABLE AND DISABLE TIMES



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NOTES:

1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. Pulse Generator for ALl Pulses: $t_f \leq 2.5ns$; $t_r \leq 2.5ns$.