

^{May 2012} UniFET™

FDP5N50F / FDPF5N50FT N-Channel MOSFET, FRFET 500V, 4.5A, 1.55Ω

Features

- R_{DS(on)} = 1.25Ω (Typ.)@ V_{GS} = 10V, I_D = 2.25A
- Low gate charge (Typ. 11nC)
- Low C_{rss} (Typ. 5pF)
- · Fast switching
- 100% avalanche tested
- · Improved dv/dt capability
- RoHS compliant



Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pluse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power suppliesand active power factorcorrection.



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

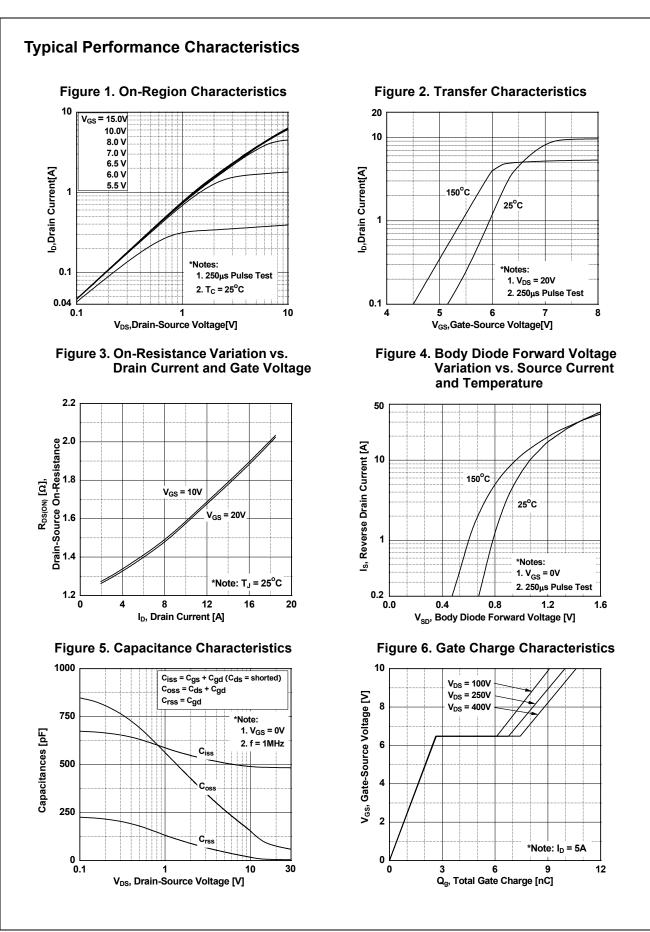
Symbol			FDP5N50F	FDPF5N50FT	Units	
V _{DSS}	Drain to Source Voltage			500		V
V _{GSS}	Gate to Source Voltage			±30		V
ID	Desig Current	-Continuous (T _C = 25 ^o C)	-Continuous ($T_C = 25^{\circ}C$) 4.5		4.5*	•
	Drain Current	-Continuous (T _C = 100 ^o C)		2.7	2.7*	A
I _{DM}	Drain Current	- Pulsed	- Pulsed (Note 1)		18*	А
E _{AS}	Single Pulsed Avalanche Energy (N		(Note 2)	233		mJ
I _{AR}	Avalanche Current		(Note 1)	4.5		А
E _{AR}	Repetitive Avalanche Energy		(Note 1)	8.5		mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5		V/ns
P _D	Devues Dissinction	(T _C = 25°C)		85	28	W
	Power Dissipation	- Derate above 25°C		0.67	0.22	W/ºC
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +150		°C
TL	Maximum Lead Temperature for Soldering Purpose, 300 1/8" from Case for 5 Seconds 300			00	°C	

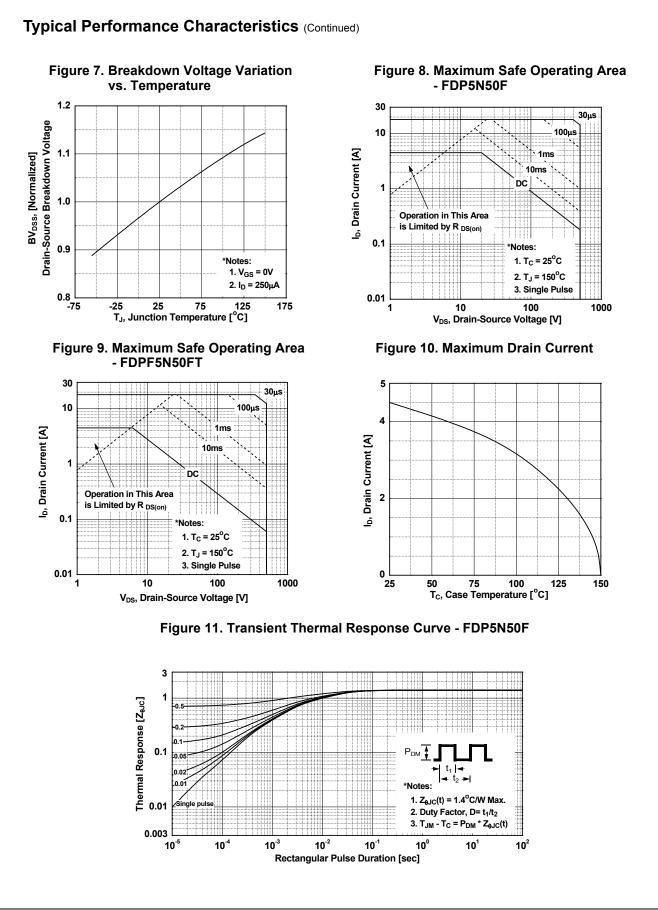
Thermal Characteristics

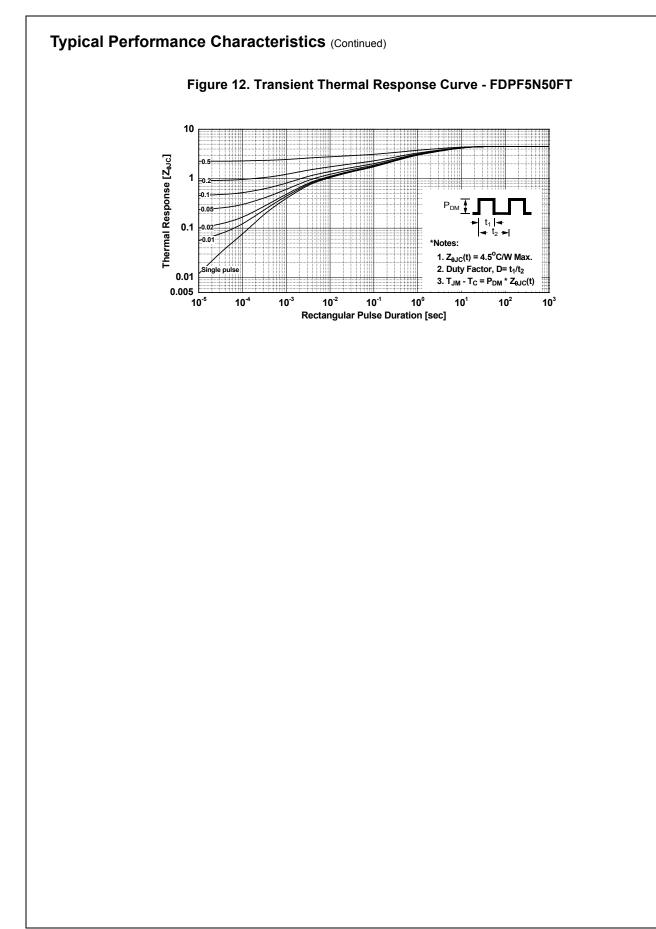
Symbol	Parameter	FDP5N50F	FDPF5N50FT	Units
$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case	1.4	4.5	
$R_{\theta CS}$	Thermal Resistance, Case to Sink Typ.	0.5	-	°C/W
$R_{ ext{ heta}JA}$	Thermal Resistance, Junction to Ambient	62.5	62.5	

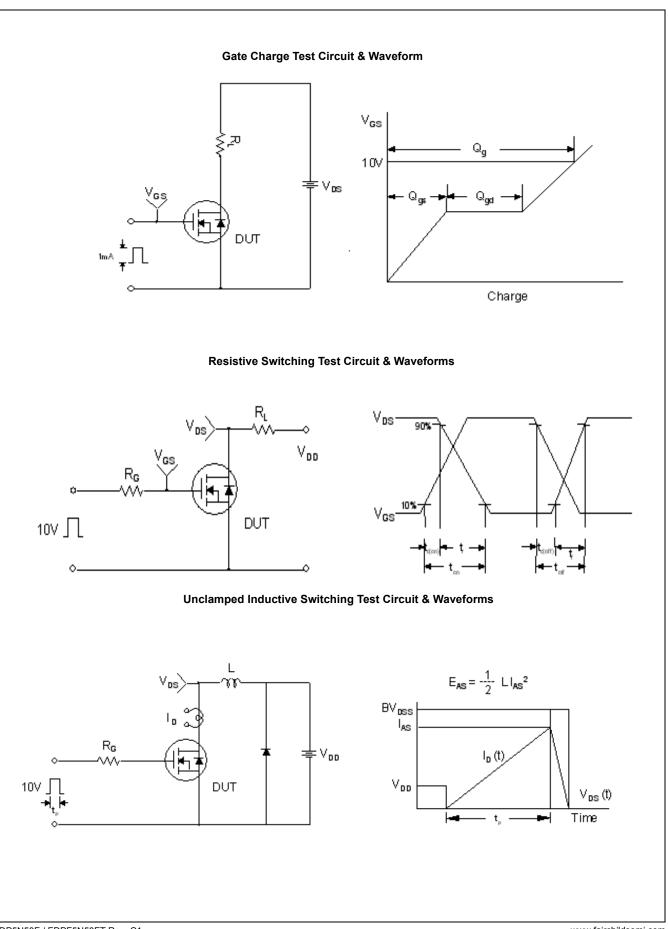
Device MarkingDeviceFDP5N50FFDP5N50FFDPF5N50FTFDPF5N50FT		Device	Packag	е	Reel Size	Таре	e Width		Quantit	у
		FDP5N50F	TO-220)	-		-		50 50	
		FDPF5N50FT	TO-220	F	-		-			
Electrica	l Char	racteristics				<u> </u>				
Symbol		Parameter		Test Conditions		Min.	Тур.	Max.	Units	
Off Charac	teristic	s				L	1		l.	
BV _{DSS}	Drain to	o Source Breakdown V	oltage	I _D = 250μA, V _{GS} = 0V, T _J = 25 ^o C			500	-	-	V
ΔBV_{DSS} $\Delta T_{,l}$		own Voltage Temperat	-	$I_D = 250 \mu$ A, Referenced to 25° C		-	0.6	-	V/ºC	
		ata Maltana Duain Cum		V _{DS} = 500V, V _{GS} = 0V			-	-	10	
IDSS	Zero Gate Voltage Drain Current		ent		$V, T_{C} = 125^{\circ}C$		-	-	100	μΑ
I _{GSS}	Gate to	Body Leakage Currer	nt	$V_{GS} = \pm 3$	0V, V _{DS} = 0V		-	-	±100	nA
On Charac	teristic	S								
V _{GS(th)}	Gate Threshold Voltage		V _{GS} = V _{DS} , I _D = 250μA		3.0	-	5.0	V		
R _{DS(on)}	Static D	Drain to Source On Res	sistance		$V_{\rm GS} = 10V, I_{\rm D} = 2.25A$		-	1.25	1.55	Ω
9FS	Forwar	d Transconductance		V, I _D = 2.25A	(Note 4)	-	4.3	-	S	
Dynamic C _{Ciss}	1	eristics apacitance		V - 25	V V = 0V		-	490	650	pF
C _{oss}	Output	Capacitance		−V _{DS} = 25V, V _{GS} = 0V – f = 1MHz		-	66	88	pF	
C _{rss}	Reverse Transfer Capacitance		1 110112			-	5	7.5	pF	
Q _{g(tot)}	Total G	Gate Charge at 10V to Source Gate Charge		$V_{DS} = 400V, I_D = 5A$		-	11	15	nC	
Q _{gs}	Gate to					-	3	-	nC	
Q _{gd}	Gate to	Drain "Miller" Charge		V _{GS} = 10V (Note 4, 5)		-	5	-	nC	
Switching	Charac	teristics								
t _{d(on)}	Turn-O	n Delay Time					-	13	36	ns
t _r	Turn-O	n Rise Time		V_{DD} = 250V, I_D = 5A R_G = 25 Ω			-	22	54	ns
t _{d(off)}	Turn-O	ff Delay Time				-	28	66	ns	
t _f	Turn-Off Fall Time		(Note 4, 5)		-	20	50	ns		
Drain-Sou	rce Dio	de Characteristic	S							
I _S	Maximum Continuous Drain to Source Diode			Forward	Current		-	-	4.5	Α
I _{SM}	Maximum Pulsed Drain to Source Diode For			rward Current			-	-	18	Α
V _{SD}	Drain to	Source Diode Forwar	d Voltage	V _{GS} = 0V, I _{SD} = 4.5A		-	-	1.5	V	
t _{rr}	Reverse	e Recovery Time		V _{GS} = 0V	, I _{SD} = 5A		-	65	-	ns
Q _{rr}	Reverse	e Recovery Charge	$dI_{F}/dt = 100A/\mu s \qquad (Note 4)$		-	120	-	nC		

 $\begin{array}{ll} 3: \ I_{SD} \leq 4.5A, \ di/dt \leq 200 A/\mu s, \ V_{DD} \leq BV_{DSS}, \ Starting \ T_{J} = 25^{\circ}C \\ 4: \ Pulse \ Test: \ Pulse \ width \leq 300 \mu s, \ Duty \ Cycle \leq 2\% \\ 5: \ Essentially \ Independent \ of \ Operating \ Temperature \ Typical \ Characteristics \\ \end{array}$



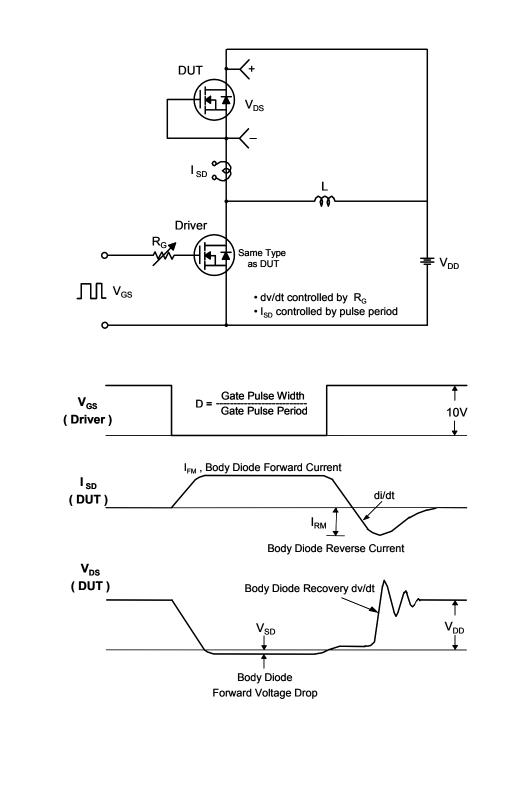


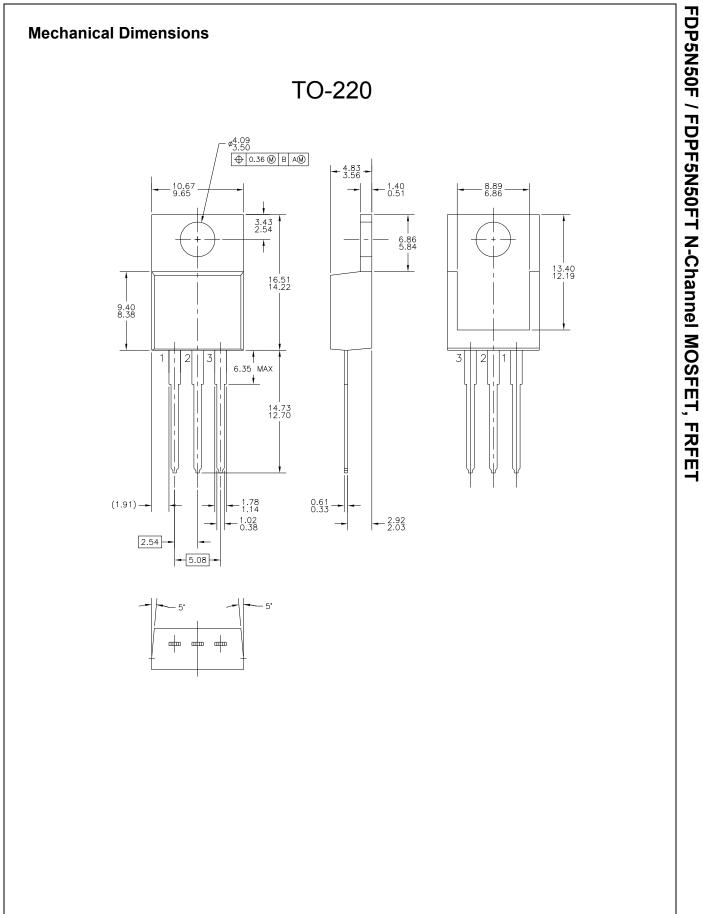


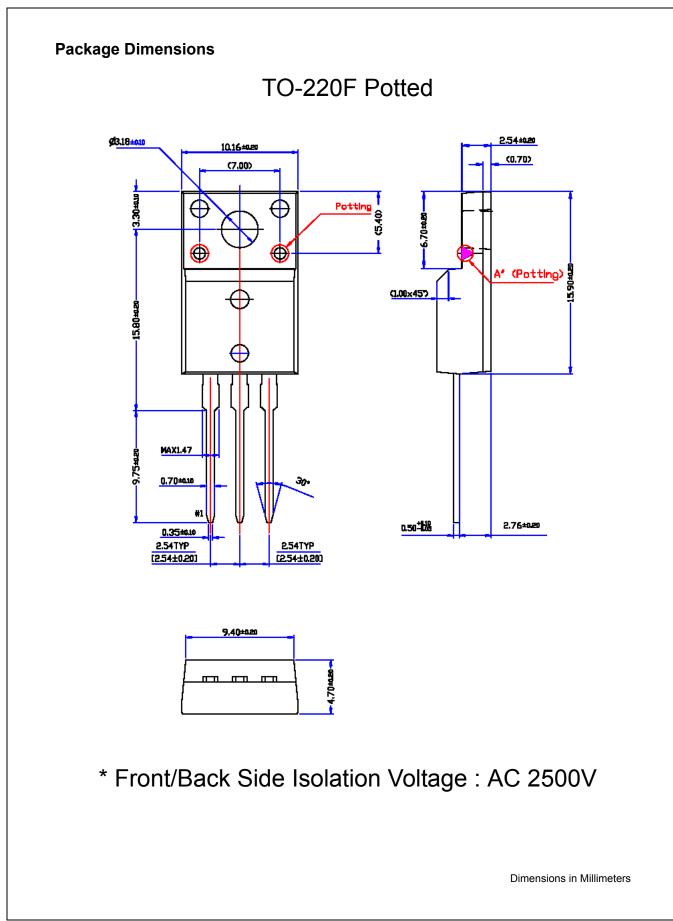


FDP5N50F / FDPF5N50FT N-Channel MOSFET, FRFET

Peak Diode Recovery dv/dt Test Circuit & Waveforms









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