RCC611

100BaseTX Transceiver

Features

- 100 Mbps/125 Mbaud data rates
- Low power 0.6 micron CMOS technology
- PLL Clock and data recovery
- Clock synthesizer
- Auto-negotiation
- 4b/5b Encode/Decode
- FDDI TP/PMD scrambling/descrambling
- Management Interface for control/status
- Link Pulse Signalling
- Conforming to MII interface of IEEE 100baseTX Fast Ethernet Standard(P802.3u/D3)
- Low Power Dissipation—600 mW typical
- Single power supply: +5V
- PECL compatible serial data inputs/outputs
- Support for external 10 Mbps PHY
- 100 pin PQFP (20mm x 14mm x 2.7 mm)

Applications

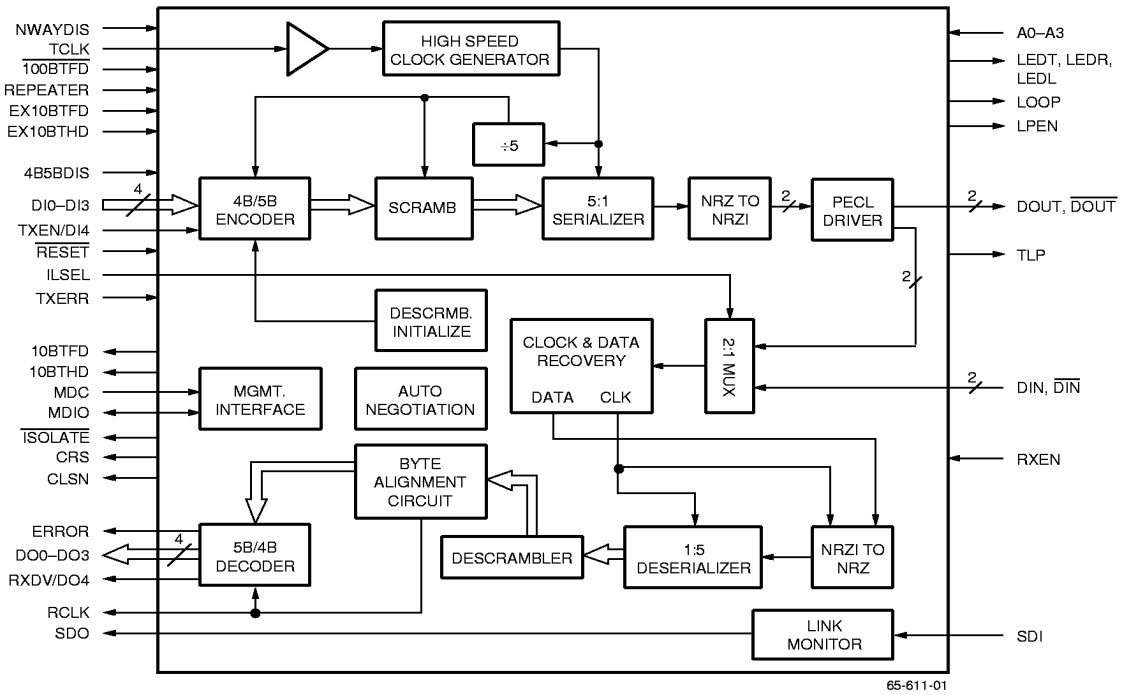
- Fast Ethernet Adapter/hub/switch
- FDDI Adapter/hub
- High Speed Point to Point Links
- Bus Extenders
- Multimedia
- High Resolution Graphic Displays
- Fast Ethernet test equipment
- FDDI Test Equipment

Description

The RCC611 is a monolithic 125 Megabaud CMOS transceiver chip. It integrates a complete phase-locked loop clock and data recovery, a phase locked loop clock synthesizer, a 5:1 Serializer, a 1:5 Deserializer, 4B/5B Encoder, 5B/4B Decoder, auto-negotiation and a management interface for link control and status. It also includes scrambler, descrambler for twisted pair copper applications in compliance with FDDI TP-PMD specifications. In conjunction with RCC613 twisted pair transceiver, the chipset can be used for driving with category 5 unshielded twisted pair cable and Type 1 shielded twisted pair cable. The chip meets the physical layer interface requirements of the 100 Base-X Fast Ethernet and FDDI standards. The RCC611 chip operates with a single, +5V power supply.

Advanced Information

Block Diagram



Rev. 0.5.0A

ADVANCED INFORMATION data sheets provide specification for products not yet complete or characterized. They provide design target information for customer planning purposes.

Advanced Information

Functional Description

Transmitter Section

The RCC611 transmitter section includes a phase locked loop synthesizer, 4B/5B encoder, scrambler and 5:1 serializer.

The RCC611 accepts a CMOS data nibble (DI0-DI3) and a control bit, TXEN. The data gets strobed on the positive transition of TCLK. The transmitter encodes the data, DI0-DI3 using 4b/5b coding (see Table 1). TXEN is used to denote the transmitter input being active or not. Whenever TXEN=0, IDLE symbol (11111) is encoded and transmitted. When TXEN transitions from 1 to 0, TR byte is sent before transmitting IDLE symbols. The order of transmission of the 4b/5b encoded output (E4..0)is that the most significant bit of the encoded symbol, E4 is transmitted first followed by E3,E2,E1 and E0.

When 4B5BDIS is HIGH, the 4b/5b encoder is bypassed. Under that case, TXEN is used as the fifth bit (DI4) of the encoded symbol. The order of transmission of the input when 4B5BDIS is HIGH is DI4 followed by DI3, DI2, DI1 and DI0.

The clock generator consists of a frequency multiplying Phase Locked Loop (PLL). The multiplying ratio is 5. The serial output goes through Non-Return-to-Zero (NRZ) to Non-Return-to-Zero Invert on Ones (NRZI) conversion. The NRZ to NRZI converter takes in the serial NRZ stream and puts out a transition for every 1 in the input stream. For zeros, there will be no transition. This will ensure that there is clocking information even when there is a long stream of 1s. The differential NRZI output is enabled to the output pins DOUT, $\overline{\text{DOUT}}$. The serial Data Stream (DOUT/ $\overline{\text{DOUT}}$) is transmitted at PECL levels (positive shifted ECL levels, Vth= +3.7 V). The input clock reference for the PLL Clock Generator, TCLK, typically comes from the CMOS protocol layer IC. TXERR=1 is used to force HALT symbol (00100) on the transmit output.

The encoded symbol is scrambled as per FDDI's TP-PMD standard. The scrambler used is a stream cipher scrambler. The scrambler polynomial is $1+x^{9}+x^{11}$.

Descrambler Initialization

The descrambler initialization timing is shown in the accompanying diagram. On powerup, TXEN=0. RCC611 automatically initializes the downstream descrambler by forcing IDLE symbols (11111) which gets scrambled and driven to the medium. Transmitting IDLE continues until TXEN=1.

The transmitter has the provision to loopback its output to the receiver input, when ILSEL=1. Under that case, a continuous logic LOW state is sent through the DOUT, $\overline{\text{DOUT}}$ pins.

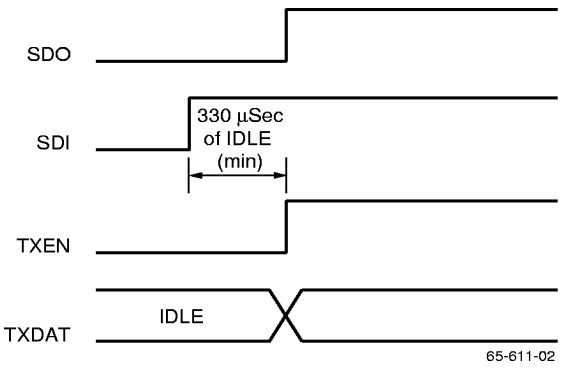


Figure 1.

There is also one more level of loopback provided through the external RCC613 chip. When control register Reg0 bit 14 is HIGH, LOOP output pin is HIGH and the the serial output, DOUT, $\overline{\text{DOUT}}$ goes through the RCC613 TXIP, TXIN inputs and loops back through the RXOP, RXON outputs back to the DIN, $\overline{\text{DIN}}$ of RCC611.

Table 1. 4B/5B Encoding

Symbol	TXEN	DI3–DI0	Encoded Output (E4-E0)
0	1	0000	11110
1	1	0001	01001
2	1	0010	10100
3	1	0011	10101
4	1	0100	01010
5	1	0101	01011
6	1	0110	01110
7	1	0111	01111
8	1	1000	10010
9	1	1001	10011
A	1	1010	10110
B	1	1011	10111
C	1	1100	11010
D	1	1101	11011
E	1	1110	11100
F	1	1111	11101
T	0	xxxx	01101
R	0	xxxx	00111
J	1	xxxx	11000
K	1	xxxx	10001
I (IDLE)	0	xxxx	11111
H (HALT)	1	xxxx	00100

Note:

1. All the symbols are encoded as per the state diagram provided in Chapter 28 of IEEE802.3.

Table 2. 5B/4B Decoding

Symbol	Encoded Output	DO3–0	ERROR
0	11110	0000	0
1	01001	0001	0
2	10100	0010	0
3	10101	0011	0
4	01010	0100	0
5	01011	0101	0
6	01110	0110	0
7	01111	0111	0
8	10010	1000	0
9	10011	1001	0
A	10110	1010	0
B	10111	1011	0
C	11010	1100	0
D	11011	1101	0
E	11100	1110	0
F	11101	1111	0
T	01101	xxxx	0
R	00111	xxxx	0
J	11000	xxxx	0
K	10001	xxxx	0
I	11111	xxxx	0
H	00100	xxxx	1
V	00000	xxxx	1
V	00001	xxxx	1
V	00010	xxxx	1
V	00011	xxxx	1
V	00101	xxxx	1
V	00110	xxxx	1
V	01000	xxxx	1
V	01100	xxxx	1
V	10000	xxxx	1
V	11011	xxxx	1

Note:

1. All the symbols are decoded as per the state diagram provided in Chapter 28 of IEEE802.3.

Receiver Section

The RCC611 Receiver section includes a 2 to 1 multiplexer, a complete phase-locked loop clock and data recovery, and decoder.

The 2 to 1 Mux is used to choose between the differential PECL receive input data (DIN, $\overline{\text{DIN}}$) or the transmit output for enabling to the clock and data recovery circuit. The choice of the inputs is made by the ILSEL pin. If ILSEL is HIGH, the transmit output is looped back to the input of the receiver. If ILSEL is LOW, the receive input is chosen.

The RCC611 recovers the clock and regenerates the encoded serial data. There is a PECL to CMOS converter for the SDI signal detect PECL input signal. If SDI goes LOW to HIGH, the SDO output goes HIGH after a minimum of 330 microseconds of continuous IDLE symbols to allow for the clock and data recovery and descrambler to synchronize.

The recovered encoded data is then converted to 5 parallel data lines via 1:5 De-Serializer.

The RCC611 contains a byte alignment circuitry. When the JK symbols are detected in the serial stream, the chip will automatically resynchronize the demultiplexer to byte align with the JK.

The data is then decoded into an 4-bit symbol via the 5b/4b decoder as per the 5b/4b Decoding table. The received data is checked during the 5b/4b decoding and violations are flagged by bringing the Error Flag (ERROR) to a level HIGH. The 5b/4b decoder is bypassed for FDDI.

The output from the 5b/4b decoder comes out as 4 bits of data, DO0–DO3 and one control bit output, RXDV. When 4B5BDIS is HIGH, the 5b/4b decoder is bypassed and the output come out as DO0-DO4 where DO4 replaces the RXDV signal.

The demultiplexed data goes through a descrambler. The descrambler descrambles the data as per the polynomial discussed in the transmit section.

CLSN signal is flagged if the chip is transmitting and receiving data as per the IEEE802.3 transmit and receive state diagram in Chapter 24. CRS is flagged if either the chip is transmitting data or receiving data as per the IEEE802.3 transmit and receive state diagram in Chapter 24. Both CLSN and CRS are asynchronous signals.

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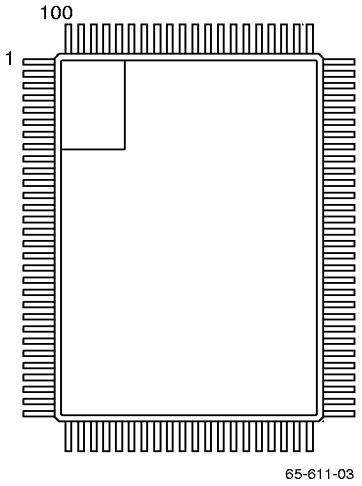
Pin Assignments



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DGND	26	DVCC	51	LPEN	76	DVCC
2	DGND	27	$\overline{\text{RESET}}$	52	RXEN	77	NC
3	DVCC	28	LEDT	53	DGND	78	NC
4	DVCC	29	$\overline{\text{ISOLATE}}$	54	DGND	79	NC
5	NC	30	LEDR	55	DO3	80	NC
6	AGND	31	LEDL	56	DO2	81	DIN
7	DGND	32	DVCC	57	DO1	82	$\overline{\text{DIN}}$
8	4B5BDIS	33	DGND	58	DO0	83	NC
9	DI0	34	A0	59	DVCC	84	SDI
10	DI1	35	A1	60	DVCC	85	DGND
11	DI2	36	A2	61	RXDV/DO4	86	AGND
12	DI3	37	A3	62	ERROR	87	RXAVCC
13	TXEN/DI4	38	DGND	63	DGND	88	AGND
14	TXERR	39	DGND	64	RCLK	89	RXAVCC
15	DGND	40	10BTFD	65	SDO	90	TXAVCC
16	TCLK	41	10BTHD	66	AGND	91	AGND
17	DVCC	42	EX10BTHD	67	DGND	92	DGND
18	REPEATER	43	EX10BTFD	68	DVCC	93	DVCC
19	NC	44	CLSN	69	DGND	94	TXAVCC
20	MDC	45	CRS	70	DGND	95	TXAVCC
21	MDIO	46	$\overline{\text{100BTFD}}$	71	DVCC	96	AGND
22	LOOP	47	TLP	72	DVCC	97	AGND
23	NC	48	DVCC	73	DGND	98	ILSEL
24	NC	49	DVCC	74	DGND	99	$\overline{\text{DOUT}}$
25	DGND	50	NWAYDIS	75	DVCC	100	DOUT

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Pin Descriptions

Pin Name	Pin Number	Type	Description
10BTFD	40	CMOS O/P	**10BaseT Full Duplex.**10BTFD is used to enable or disable a local 10BaseT Full duplex device.
10BTHD	41	CMOS O/P	**10BaseT Half Duplex.** 10BTHD is used to enable or disable a local 10BaseT half duplex physical layer device.
4B5BDIS	8	TTL I/P	**4b/5b disable.** This pin is used to disable the 4b/5b encoder and 5b/4b decoder.
A0–A3	34–37	TTL I/P	**Address 0–3.** A0–A3 pins are used to denote the physical address of the chip for writing or reading of the internal control/ status registers. During reset, if the PHY address are all zeroes (0000) then the MII interface will be tri-stated.
AGND	6, 66, 86, 88, 91, 96, 97		**Chip ground for Analog circuitry.** AGND pins should be connected to the printed circuit board's ground plane at the pins.
CLSN	44	CMOS O/P	**Collision.** This output is HIGH if the chip is receiving data and at the same time it is transmitting packet data. It is an asynchronous output. CLSN is LOW during Full duplex mode of operation.
CRS	45	CMOS O/P	**Carrier Sense.** This output is HIGH if the chip is either receiving data or transmitting packet data. It is an asynchronous output. CRS is determined by receive activity during Full duplex mode.
DGND	1, 2,7,15, 25, 33, 38, 39, 53, 54, 63, 67, 69, 70, 73, 74, 85, 92		**Chip ground for digital circuitry.** DGND should be connected to the printed circuit board's ground plane at the pins.

Pin Descriptions (continued)

Pin Name	Pin Number	Type	Description
DIN, $\overline{DIN}$	81, 82	PECL I/P	**Receiver differential input data.**
DO0–DO3	58-55	CMOS O/P	**Receiver output data.**
DOUT, $\overline{DOUT}$	100, 99	PECL O/P	**Transmit differential output data.**
DVCC	3, 4, 17, 26, 32, 48, 49, 59, 60, 68, 71, 72, 75, 76, 93		**Positive supply for Digital circuitry.** The nominal value is 5V ±5%. VCC should be bypassed to the ground plane with a 0.1µF chip capacitor placed as close to the pin as possible.
DI0–DI3	9-12	TTL I/P	**Transmitter Input data.**
ERROR	62	CMOS O/P	**Error Flag.** ERROR goes HIGH to flag 5B/4B decoding violations. It also indicates transition to idle condition from active without end of frame delimiters.
$\overline{100BTFD}$	46	CMOS O/P	**100BaseT Full Duplex.** $\overline{100BTFD}$ when low is used to activate a LED and indicates that the RCC611 is operating in the 100BaseT Full Duplex mode.
EX10BTFD	43	TTL I/P	**10BaseT Full Duplex.** When EX10BTFD is high, it indicates that there is available an external 10BaseT Physical layer device capable of full duplex operation. This input goes directly to Reg1 bit12.
EX10BTHD	42	TTL I/P	**10BaseT Half Duplex**. When EX10BTHD is high, it indicates that there is available an external 10BT physical layer device with half duplex capability. This input goes directly to Reg1 bit11.
$\overline{ISOLATE}$	29	CMOS O/P	**Isolate.** $\overline{ISOLATE}$ is used to indicate that the chip is in the isolate mode. When activated (low), all the MII interfaces will be tri-stated. Software can be used to override the the $\overline{ISOLATE}$ bit (Reg0 bit10). Note that the polarity of $\overline{ISOLATE}$ and Reg0 bit10 are the opposite to each other. See page 10 for more details.
LEDL	31	CMOS O/P	**LED Link OK.** It is used as an active LOW output to indicate that the link is OK as indicated by the FLG signal from the arbitration state machine.
LEDR	30	CMOS O/P	**LED Receive.** It is used as an active LOW output to indicate that the receive is active. It will be LOW if CRS = 1.
LEDT	28	CMOS O/P	**LED Transmit.** It is used as an active LOW output to indicate that the transmit is active. It will be LOW if TXEN = 1.
LOOP	22	CMOS O/P	**Loop.** LOOP is used to enable the loopback input of RCC613 chip. LOOP is active if the control register Reg0 bit 14 is HIGH .
LPEN	51	CMOS O/P	**Link Pulse Enable.** It provides an enable signal to the RCC613 for the transmit link pulse.
ILSEL	98	TTL I/P	**Loop Select.** ILSEL is used for differential loopback for “on-board” diagnostic of the device. When ILSEL is HIGH, the receiver accepts the serial output data from the transmitter section. Connect to GND or leave open when not used.
MDIO	21	TTL/CMOS I/O	**Management Data Input/Output.** MDIO is a bidirectional signal between RCC611 and the station management entity. It is used to transfer control and status information. All the read and write transactions are done synchronously with MDC.
MDC	20	TTL I/P	**Management Data Clock.** MDC is sourced by the station management entity to RCC611 as a timing reference for transfer of information on MDIO signal. MDC is an aperiodic signal whose minimum high and low times are 200 ns.

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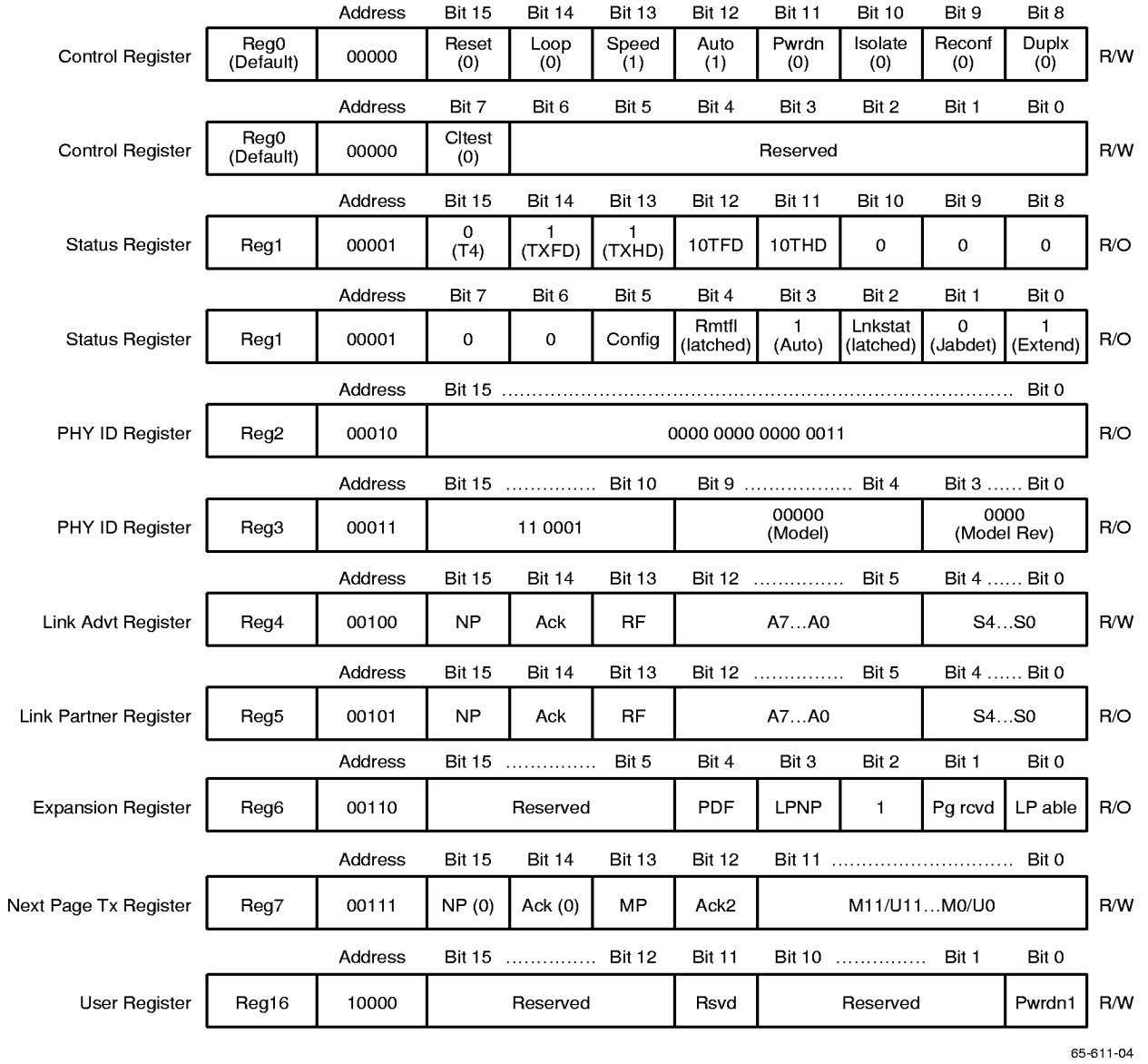
Pin Descriptions (continued)

Pin Name	Pin Number	Type	Description
NWAYDIS	50	TTL I/P	**Nway Disable.** When NWAYDIS is high, the auto-negotiation state machines are disabled and AUTO bit (Reg0 bit12) is set to 0. Software can be used to override the AUTO bit. see page 10 for more details. For manual setting, see Table 3.
RCLK	64	CMOS O/P	**Receive Clock.** It is the recovered byte clock derived from the byte alignment circuitry. It provides timing to DO0–DO3, RXDV and ERROR.
REPEATER	18	TTL I/P	**Repeater/Node Mode.** When in the Repeater (high) mode as in the Full Duplex mode, CRS output is asserted due to activity from the receiver only. When in the Node (low) mode and not Full Duplex mode, CRS is asserted due to either receive or transmit activity.
$\overline{\text{RESET}}$	27	TTL I/P	**Reset.** RESET is an asynchronous input which when LOW is used to reset the state machines inside the chip. RESET needs to be LOW for at least one byte clock.
RXEN	52	TTL I/P	**Receive Enable.** When activated (high), it enables the outputs D0-D3, CRS, ERROR, RXDV, CLSN and RCLK. When low these outputs are tri-stated.
RXAVCC	87,89		**Positive Supply for Receive Analog Circuitry.** The nominal value is 5V±5%. RXAVCC should be bypassed to the ground plane with a 0.1µF chip capacitor placed as close to the pin as possible.
RXDV/DO4	61	CMOS O/P	**Receive Data Valid.** RXDV when HIGH indicates the receive output data being active. When 4B5BDIS is HIGH, this pin is used as DO4, the fifth data output.
SDI	84	PECL I/P	**Signal Detect Input.** It is converted to CMOS output level through a PECL to CMOS converter.
SDO	65	CMOS O/P	**Signal Detect Output.** SDO is the output from the PECL to CMOS converter for the signal detect signal. The signal is asserted 330 microseconds after SDIN goes HIGH. SDO output is made synchronous to RCLK and has the same timing as the DO0–3.
TCLK	16	TTL I/P	**Transmit Clock.** TCLK is the 25 MHz input reference for the internal high speed bit clock generator. It provides the timing for the input data, DI0..DI3, TXEN and TXERR.
TLP	47	CMOS O/P	**Transmit Link Pulse.** TLP is HIGH when a link pulse needs to be transmitted.
TXAVCC	90, 94, 95		**Positive supply for Transmit Analog circuity.** The nominal value is 5V ±5%. TXAVCC should be bypassed to the ground plane with a 0.1µF chip capacitor placed as close to the pin as possible.
TXEN/DI4	13	TTL I/P	**Transmit Enable .** WhenTXEN is HIGH, it indicates that the input data is active. When 4B5BDIS is HIGH, this pin is used as DI4, the fifth data input.
TXERR	14	TLL I/P	**Transmit Error.** TXERR is used to transmit VIOLATION symbols (00100) on the transmit output.

Advanced Information

Management Interface



		Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
Control Register	Reg0 (Default)	00000	Reset (0)	Loop (0)	Speed (1)	Auto (1)	Pwrdn (0)	Isolate (0)	Reconf (0)	Duplx (0)	R/W
		Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Control Register	Reg0 (Default)	00000	CItest (0)	Reserved							R/W
		Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
Status Register	Reg1	00001	0 (T4)	1 (TXFD)	1 (TXHD)	10TFD	10THD	0	0	0	R/O
		Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Status Register	Reg1	00001	0	0	Config	Rmtfl (latched)	1 (Auto)	Lnkstat (latched)	0 (Jabdet)	1 (Extend)	R/O
		Address	Bit 15 ..... Bit 0								
PHY ID Register	Reg2	00010	0000 0000 0000 0011								R/O
		Address	Bit 15 ..... Bit 10			Bit 9 ..... Bit 4			Bit 3 ..... Bit 0		
PHY ID Register	Reg3	00011	11 0001			00000 (Model)			0000 (Model Rev)		R/O
		Address	Bit 15	Bit 14	Bit 13	Bit 12 ..... Bit 5			Bit 4 ..... Bit 0		
Link Advt Register	Reg4	00100	NP	Ack	RF	A7...A0			S4...S0		R/W
		Address	Bit 15	Bit 14	Bit 13	Bit 12 ..... Bit 5			Bit 4 ..... Bit 0		
Link Partner Register	Reg5	00101	NP	Ack	RF	A7...A0			S4...S0		R/O
		Address	Bit 15 ..... Bit 5			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Expansion Register	Reg6	00110	Reserved			PDF	LPNP	1	Pg rcvd	LP able	R/O
		Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11 ..... Bit 0				
Next Page Tx Register	Reg7	00111	NP (0)	Ack (0)	MP	Ack2	M11/U11...M0/U0				R/W
		Address	Bit 15 ..... Bit 12			Bit 11	Bit 10 ..... Bit 1			Bit 0	
User Register	Reg16	10000	Reserved			Rsvd	Reserved			Pwrdn1	R/W

65-611-04

Register Description

The management interface provides a simple, two wire, serial inteface (MDIO, MDC) to connect the station management entity to the PHY for control and status gathering. MDC is sourced by the station management entity to the PHY as a timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal with a minimum high and low times of 200 ns. MDIO is a bidirectional signal between PHY and the station management entity. Control information is driven by the station management entity synchronously to MDC and sampled synchronously by PHY. Status information is driven synchronously by PHY and sampled synchronously by the station management. As shown in the figure, there are a total of 9 sixteen bit registers: Reg0, Reg1, through Reg7 and Reg16. Their functions are detailed in the register definitions section. The default values for the registers where applicable are shown in parenthesis. All the status and control transistions occur synchronous to the local clock, TCLK.

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	Idle	SOF	OpCd	PHY Addr	Reg Addr	Fill	Data
Read:	Idle	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD
Write:	Idle	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD

Management Frame Structure

Management Frame Structure

The management frame structure is as shown in the figure. In between the frames is an Idle condition. The Idle condition on the two wire interface is a logic one through the internal pullup resistor. The open drain driver for MDIO will be disabled. Prior to initiating any transaction, the station management entity will send a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the chip with a pattern that it can use to establish synchronization.

The frame begins with an SOF field. SOF is indicated by a 01 pattern. The next field is Opcode. The Opcode for a read transaction is 10 and for a write transaction is 01. Next to Opcode is the PHY Address field. The PHY address is 5 bits. The first bit is the most significant bit of the PHY address. The chip will recognize 00000 as its own address. The next field is the register address. The register address is 5 bits. The register accessed at register address zero (00000) is the Register 0 (Reg0) and so on.

Next to the Register address is the Turnaround field. An idle bit time during which no device actively drives the MDIO signal is inserted between the Register address field and the Data field of the frame during a Read transaction in order to avoid contention. During a Read transaction, the chip will drive a zero bit onto MDIO for the bit time following the idle bit and preceding the Data field. During a write transaction, the station management entity will fill this idle time with a one bit followed by a zero bit. The data field is 16 bits. The first data bit transmitted and received is the MSB of the data payload.

Auto-Negotiation Signalling

The chip has the provision to advertise its mode of operation to the remote end of a link segment and detect corresponding operational modes that the other device may be advertising. The auto-negotiation algorithm is performed out of band using a modified 10baseT link integrity pulse sequence. The algorithm allows the devices at both ends of a link segment to request and acknowledge use of the commom modes of operation that both devices share and to reject the use of operational modes that are not shared by both devices. When more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution table.

The information is encapsulated within a burst of closely separated link integrity test pulses that meet 10baseT transmitter waveform for Link test pulses. This burst of pulses is referred to as a Fast Link Pulse (FLP) burst. The chip issues FLP bursts at powerup. The burst consists of alternating clock/data sequence.

To maintain interoperability with existing 10baseT devices, the alogrithm also supports the transmission of 10baseT compliant link integrity test pulses. 10baseT pulse is referred to as the Normal Link Pulse (NLP). A device which fails to respond to the FLP sequence and returns only the NLP indication is treated as a 10baseT compatible device.

Transmit Function

The FLP burst shall contain the Link Code Word (Reg4). FLP bursts consists of 33 pulse positions. The 17 odd numbered pulse positions are always present and represent clock information. The 16 even numbered positions represent data information. A link pulse present in an even numbered position represents a logic one and a link pulse absent from an even numbered pulse position represents a logic zero. The first pulse is a clock pulse. Clock pulses are evenly spaced apart by 125±30 microseconds. The data ONE pulse occurs 62.5±15 microseconds after the clock pulse. The first bit in consecutive FLP bursts shall occur at 16±8 msec interval. The pulses are sent through the TLP pin. A link pulse enable signal, LPEN, is also provided for convenience.

Receive Function

The receive function detects NLP sequence. In addition, the receive function shall detect FLP bursts and decode the information contained.

Arbitration Function

Arbitration function ensures proper sequencing of the autonegotiation algorithm through the transmit and receive function. The arbitration function enables the transmit function to advertise abilities and upon consistent and consecutive reception of the received link code word, advertises acknowledgement. Upon reception of 4 to 6 link code words with acknowledge bit set, the arbitration function determines the highest common denominator using the priority resolution table.

If SDO goes active before autonegotiation is complete, a test window timer will be started and at the expiration of the timer, the arbitration function shall indicate that a valid link has been established.

Advanced Information

Table 3. Manual Setting for Non-Auto-Negotiation

Function	AUTO Bit (Reg0 Bit12)	Speed Bit (Reg0 Bit13)	Duplex Bit (Reg0 Bit8)
Auto-negotiation	1	X	X
100BaseT Full Duplex	0	1	1
100BaseT Half Duplex	0	1	0
10BaseT Full Duplex	0	0	1
10BaseT Half Duplex	0	0	0

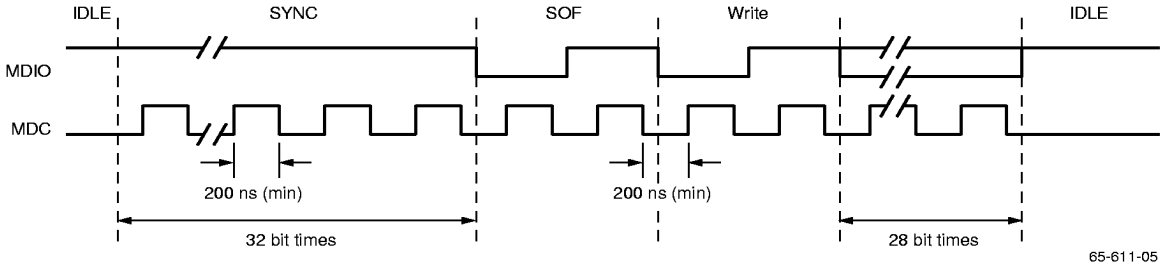


Figure 2. Management Interface Timing during Write to Registers

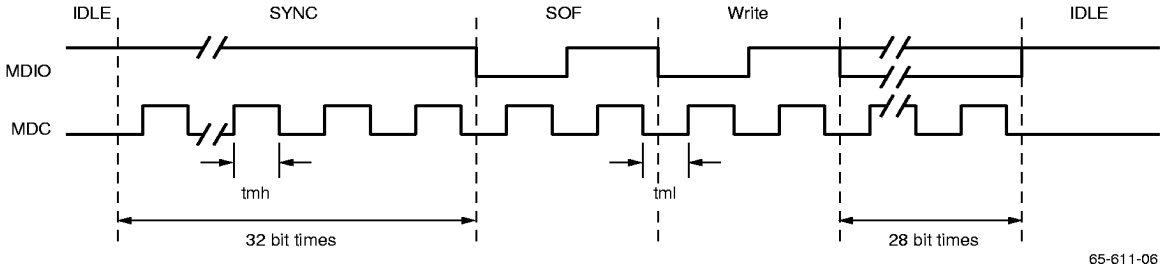


Figure 3. Management Interface Timing during Read from Registers

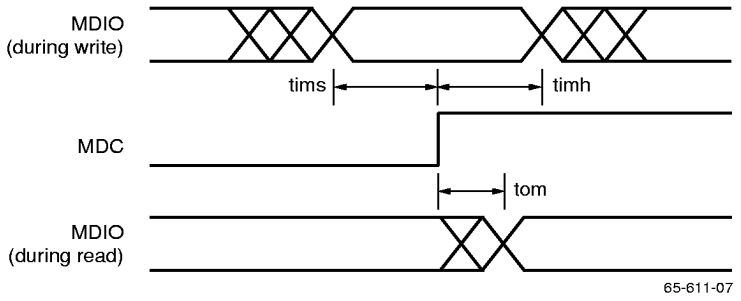


Figure 4.

Advanced Information

Register Definitions

Control Register (Read/Write) – Address 00000 (Register 0)

15	14	13	12	11	10	9	8
Reset	Loop	Speed	Auto	Pwrdn	Isolate	Reconfig	Duplex

7	6	5	4	3	2	1	0
Cltest	Reserved						

All of the control register bits (0 through 15) are read/write.

The functions within the Reg0 are as follows: speed, full/half duplex, Isolate, Automatic speed selection, Loopback, Collision test. The individual bit descriptions and the default values are as follows:

Reg	Bit	Name	Default	Description
0	15	Reset	O	Reset = 1 resets the PHY, i.e. all the control and status registers are reset to their default states. This function is self-clearing. The default value is zero. Writes to other bits of control register has no effect until the reset process is completed.
0	14	Loop	O	Loop = 1. This bit is used to enable the LOOP output pin HIGH and thereby enable the local loopback of the RCC611 through the RCC613. The default value is zero.
0	13	Speed	I	This bit is used to manually set the speed of operation. Speed=1 denotes 100 Mbps mode of operation. Speed=0 denotes 10 Mbps mode of operation. This bit is used to manually set the speed of operation. This bit is effective only if Auto (Reg0, bit 12)=0 (ie. manual speed selection). The default value is one. If bit12 (Auto) of Reg0=0, and Speed=0, 10Mbps operation is enabled and determined by Reg 1 bit 12 and bit 11. If bit12 (Auto) of Reg0=0 and Speed=1, 100 Mbps operation is enabled.
0	12	Auto	I	Auto = 1 denotes automatic speed selection. Auto=0 denotes manual speed selection. Auto speed selection enables PHY's auto selection algorithm. The default value = 1.
0	11	Pwrdn	O	Pwrdn = 1 shuts off the power to the chip except the portions involving the management transactions. The default value=0. Both Pwrdn & Pwrdn1 cannot be HIGH at the same time. If so, there will not be any power down.
0	10	Isolate	O	The chip isolates its data path from the parallel (MII) interface when Isolate=1. When Isolate=1, the chip will tristate the CMOS outputs: RXCLK, RXDV, ERROR, RXD3..RXD0, CLSN, & CRS. Also, the TTL inputs (DI0..DI3, TXEN, TXERR, TCLK) are ignored. The default value=0. If A(3..0)=0000, the default value=1. This bit is brought out as ISOLATE pin. This can be used to enable or disable an external additional PHY connected to the same controller.
0	9	Reconfig	O	Autolink configuration process will be initiated when Reconfig=1. This bit is self-clearing.
0	8	Duplex	O	When auto-configuration is disabled (Auto=0), Duplex=1 sets the chip for full duplex operation. In this mode, CRS signal is determined by receive activity. Duplex=0 sets the chip for half duplex operation. The default value of Duplex=0.
0	7	Cltest	O	When Cltest=1, CLSN is asserted in response to TXEN. The default value of Cltest=0.
0	6–0	Reserved	O	These bits are reserved for future definition. They are set equal to zero.

Advanced Information

Register Definitions (continued)

Status Register (Read Only) – Address 00001 (Register 1)

15	14	13	12	11	10	9	8
0 (T4)	1 (TXFD)	1 (TXHD)	10TFD	10THD	0	0	0

7	6	5	4	3	2	1	0
0	0	Config	Rmtflt	1 (Auto)	Lnkstat	0 (Jabdet)	Extend

The status functions are as follows: information about all the modes of operation supported by the local PHY, the status of auto-negotiation, and if auto-negotiation is supported by the local PHY or not.

Reg	Bit	Name	Default	Description
1	15	T4	0	T4=1 indicates the mode is 100 base T4 capable. T4 is set to 0 for RCC611
1	14	TXFD	1	TXFD=1 indicates the mode is capable of full duplex transmission at 100 base TX. TXFD is set to 1 for RCC611
1	13	TXHD	1	TXHD=1 indicates the mode is capable of half duplex transmission at 100 base TX. TXHD is set to 1 for RCC611
1	12	10TFD	—	10TFD=1 indicates the local PHY has the ability to perform full duplex link transmission and reception using the 10baseT signalling specification. 10TFD=1 if the input pin EX10BTFD is equal to 1.
1	11	10THD	—	10THD=1 indicates the local PHY has the ability to perform half duplex link transmission and reception using the 100baseTX signalling specification. 10THD=1 if the input pin EX10BTHD is equal to 1.
1	10–6	Reserved	0	Bits10–6 are reserved for future definition. These bits are set to zero.
1	5	Config		When Config=1, it indicates that the auto link configuration has been completed and the Registers Reg4, Reg5 and Reg6 are valid. When Config=0, it indicates that the auto link configuration has not been completed. If control register bit 12 (Auto) =0, Config is set to zero.
1	4	Rmtflt		When Rmtflt=1, it indicates that a remote fault condition has been detected. This bit is set to 1 if Reg5 bit 13=1. This bit will remain set until read.
1	3	Auto	1	Auto=1 constitutes the ability of RCC611 to perform auto link detection and configuration. It is set to 1 to indicate that the local PHY has the ability to perform auto link detection and configuration.
1	2	Lnkstat		Lnkstat=1 indicates that the link is active. SDO going HIGH sets Lnkstat HIGH and SDO going HIGH to LOW causes Lnkstat to go HIGH to LOW. Lnkstat=0 indicates that the link is not valid. The occurance of a link failure condition will cause Lnkstat=0 and will remain equal to zero until read. It is set to 1 after read and remains set until the next occurence of SDO going HIGH to LOW.
1	1	Jabdet	0	This bit is set to 0 since jabber detect function is not supported.
1	0	Extend	1	Extend=1 indicates that the PHY provides extended set of capabilities which may be accessed through the extended register set, Reg2 through Reg6. The Extend bit is set to 1 for RCC611.

Advanced Information

Register Definitions (continued)

PHY ID Register (Read Only) – Address 00010 (Register 2)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000 0000 0000 0011															

PHY ID Register (Read Only) – Address 00011 (Register 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11 0001						00 0000 (Model)						0000 (Model Rev)			

Register 2 and Register 3 provide a 32-bit value which shall constitute a unique identifier for the PHY. Bits 15–0 of Register 2 and Bits 15–10 of Register 3 constitute the manufacturer ID (OUI). Bits 9–4 of Register 3 constitutes the vendor model and is set to zero. Bits 3–0 of Register 3 constitutes the vendor model version and is set to zero.

Link Advertisement Register (Read/Write) – Address 00100 (Register 4)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Ack	RF	A7–A0								S4–S0				

Register 4 provides a 16-bit value used by the auto link configuration process. Bit 0 is the first bit to be transmitted followed by Bit 1, Bit 2–Bit 15.

Reg	Bit	Name	Default	Description
4	15	NP	0	Next Page (NP) bit is set to 1 to indicate that this node intends to advertise another Link code word. Otherwise, this bit is set to 0. This bit is set through the management interface. The default value is 0.
4	14	Ack	0	Acknowledge (ACK) field is used by the auto-negotiation algorithm to indicate that a station has successfully received its link partner's code word. If no next page (Reg4 bit15=0), this bit is set to 1 after the station has successfully received at least 3 consecutive and consistent Fast Link Pulse Bursts. If next page is to be sent as indicated by the NP bit, this bit is set to 1 after the node has successfully received at least 3 consecutive and consistent FLP bursts and read the current Link Code Word. When the ACK bit is set to 1, the Link Code Word shall be sent 6 times. Initially on powerup, before the auto-negotiation starts, ACK=0.
4	13	RF	0	Remote Fault (RF) is set to 1 to indicate to the link partner the presence of a fault. Otherwise, this bit shall be set to 0. This bit is set to 1 through the management interface. The default value is 0.
4	12–5	A7–A0	0	A7–A0 indicate the technological ability field. This field is used to indicate the supported technologies for each selector field value. The default value is 0. The bit assignments for various technologies are as follows: A0 10baseT A1 10baseT full-duplex A2 100baseTX A3 100baseTX full-duplex A4 100baseT4 A5–7 Reserved
4	4–0	S4–S0		S4–S0 is the selector field. It indicates the type of message that is being sent. For IEEE802.3, S4–S0=00001.

Register Definitions (continued)

Link Partner Register (Read Only) – Address 00101 (Register 5)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Ack	RF	A7–A0								S4–S0				

Register 5 is the link partner's advertised capability register. The fields are same as those of Register 4. Upon successful completion of the auto-negotiation as indicated by Register 1/Bit 5 set to 1, Register 5 has valid information about the advertised ability of the link partner's PHY.

Expansion Register (Read Only) – Address 00110 (Register 6)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											PDF	LPNP	1	Pg Rcvd	LP Able

Reg	Bit	Name	Description
6	15–5	Reserved	Bits 5 through 15 of Register 6 are reserved for future expansion.
6	4	PDF	PDF = 1 indicates a fault has been detected via the Parallel Detection function. Default = 0.
6	3	LPNP	LPNP indicates that the link partner supports the Next Page function.
6	2	NP Able	NP Able indicates local device is Next Page able. It is set to 1.
6	1	Pg Rcvd	Pg rcvd bit is a status bit and indicates that 3 identical and consecutive link code words have been received. This bit is auto clear on read.
6	0	LP Able	LP Able indicates that the Link Partner is able to participate in the auto-negotiation algorithm.

Advanced Information

Register Definitions (continued)

Next Page Register (Read/Write) – Address 00111 (Register 7)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Ack	MP	Ack2	M11/U11–M0/U0											

This next page register is a control register used to convey information beyond that of the base page. All the bits except Ack are written through the management interface.

Reg	Bit	Name	Description
7	15	NP	It is set to 1 to indicate that this node intends to advertise another next page. Otherwise, this bit is set to 0. The default value is 0.
7	14	Ack	Acknowledge (Ack) field is used by the auto-negotiation algorithm to indicate that a station has successfully received the link partner's next page. If no next page (Register 7, Bit 15=0), this bit is set to 1 after the station has successfully received at least 3 consecutive and consistent Fast Link Pulse Bursts. If next page is to be sent as indicated by the NP bit, this bit is set to 1 after the node has successfully received at least 3 consecutive and consistent FLP bursts and read the current Link Code Word. When the ACK bit is set to 1, the Link Code Word shall be sent 6 times. Initially on powerup, before the auto-negotiation starts, Ack=0.
7	13	MP	Message Page (MP). This field is used to differentiate the next page to be message page or the unformatted page. If MP=1, the next page is a message page. If MP=0, the message page is unformatted. Any unformatted page shall be preceded by a message page.
7	12	Ack2	Acknowledge2 (Ack2). If Ack2=1, the station has the ability to comply with the received next page. If Ack2=0, the station will not comply with the message.
7	11–0	M11/U11–M0/U0	This is the 12 bit encoded message or unformatted message depending on MP being 1 or 0 respectively.

User Control/Status Register (Read/Write) – Address 10000 (Register 16)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Rsvd	Reserved										Pwrdn1

This register is used for additional control & status which are user specific. The additional functions are as follows:

Reg	Bit	Name	Description
16	15–12	Reserved	Bits 12 through 15 are reserved for future use.
16	11	Reserved	Flow Control Enable. This bit is used to enable flow control signalling mechanism inside the chip.
16	10–1	Reserved	Flow Control Symbols. This is a user-assigned symbol pair that is used to communicate the flow control information to the other communicating node. Do not write JK code combination (1100010001) into this set of bits.
16	0	Pwrdn1	In this mode, link signalling is enabled during powerdown.

Advanced Information

Absolute Maximum Ratings[1]

Parameter	Min	Max	Unit
Storage Temperature Range	-65	150	°C
Junction Temperature Range	-55	150	°C
Lead Temperature Range (soldering, 10 seconds)		300	°C
Positive Power Supply, VCC, ATXVCC, ARXVCC	0	6	V
Voltage applied to any TTL inputs	-1	6	V
Voltage applied to any PECL inputs	-1	6	V
Voltage applied to any CMOS outputs	-1	6	V
Voltage applied to any PECL outputs	-1	6	V
Current from any CMOS outputs	-50	50	mA
Current from any PECL outputs	-50	50	mA

Note:

1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Operating Conditions

Parameter		Min	Typ	Max	Units
Ta	Ambient Operating Temperature	0		70	°C
VCC	Positive Supply Voltage (DVCC and AVCC)	4.75	5.0	5.25	V
RI	PECL Differential Load Resistance (Note 1)	80	100	120	Ω

Note:

1. Differential load resistance of 100 Ω equals 50 Ω to AC ground on each of DOUT, $\overline{\text{DOUT}}$.

Advanced Information

DC Electrical Characteristics

AVCC, DVCC = 5V±5%, GND=0V, unless otherwise indicated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Transmitter Section						
Vihc	TTL input Voltage HIGH		2.0		VCC+0.5	V
Vilc	TTL input Voltage LOW		0		0.8	V
Iinc	TTL Input Current		-1		100	µA
Ci	Input Capacitance			4	10	pF
Vohp	PECL Output Voltage HIGH	Rdiff=100Ω, VCC=5V	3.5	3.8	4.2	V
Volp	PECL Output Voltage LOW	Rdiff=100Ω, VCC=5V	2.6	3.0	3.4	V
Vop	PECL Output Voltage amplitude	Vohp-Volp, VCC=5V	0.6	0.8	1.0	V
Iolp	PECL Output Current HIGH			8		mA
Receiver Section						
Vihc	TTL input Voltage HIGH		2.0		+5.5	V
Vilc	TTL input Voltage LOW		0		0.8	V
Iinc	TTL Input Current		-1		1	µA
Vcm	Com. Mode Range (DIN,$\overline{\text{DIN}}$)		2		5	V
Vdiff	Diff. Input Voltage (DIN, $\overline{\text{DIN}}$)		0.2		5.5	V
Iip	PECL Input Current		-1		1	µA
Vohc	Output Voltage HIGH		3.5		VCC	V
Volc	Output Voltage LOW		0		0.5	V
Iolc	Output Current LOW		4			mA
Iohc	Output Current HIGH		4			mA
ICC	Power Supply Current			120		mA
PD	Power Dissipation			600		mW

Advanced Information

AC Electrical Characteristics

AVCC, DVCC = 5V±5%, GND = 0V, unless otherwise indicated

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Transmitter Section						
Tt1	TCLK Period			40		ns
Tch	TCLK Pulse Width HIGH		15			ns
Tcl	TCLK Pulse Width LOW		15			ns
tids	DIN0–DIN7,TXEN,TXERR to TCLK ↑ setup time		4			ns
tidh	TCLK ↑ to DIN0–3, TXEN,TXERR hold time		4			ns
tr, tf	DOUT, $\overline{\text{DOUT}}$ rise and fall times	10% to 90% points			2	ns
ttj	DOUT, $\overline{\text{DOUT}}$ total pk-pk jitter				1.4	ns
tdj	DOUT, $\overline{\text{DOUT}}$ pk-pk duty cycle distortion				500	ps
Receiver Section						
fcc	Input Data Rate Variation				±1000	ppm
D	Input Data Transition Density to Acquire and Maintain Lock		0.1			ppm
n	Maximum run length of consective 1's or 0's before loss of lock		60			bits
tacq	Loop Acquisition Time for 10E-12 BER				1000	bits
tri, tfi	DIN, $\overline{\text{DIN}}$ input rise and fall time				1	ns
tj	DIN, $\overline{\text{DIN}}$ input peak to peak jitter tolerance				0.075T	ns
tod	RCLK ↓ to DO0–DO3, RXDV valid				10	ns
Tr1	RCLK period			40		ns
Trh	RCLK pulse width HIGH		0.35Tr1	0.4Tr1	0.45Tr1	ns
Management Section						
Tmh	MDC pulse width HIGH		200			ns
Tml	MDC pulse width LOW		200			ns
tims	MDIO to MDC ↑ setup		5			ns
timh	MDIO to MDC ↑ hold		5			ns
tom	MDC ↑ to MDIO				15	ns

Note:

1. Test conditions (unless otherwise indicated:) PECL Input rise and fall times ≤1ns, RL = 100Ω (differential), RL = 50Ω (single-ended). TTL Input rise and fall times ≤15ns. Transition density ≥ 0.1.

Advanced Information

TIming Diagrams

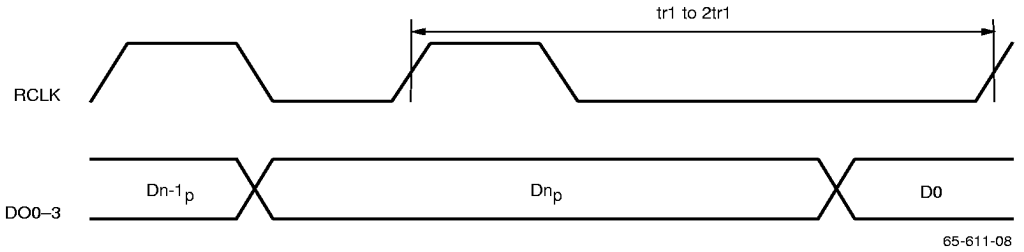


Figure 5. Receiver Timing—New Alignment

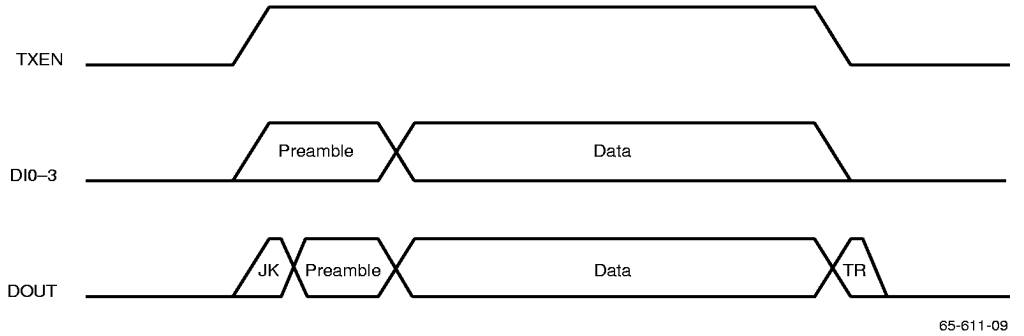


Figure 6. Frame Sequence—Transmit

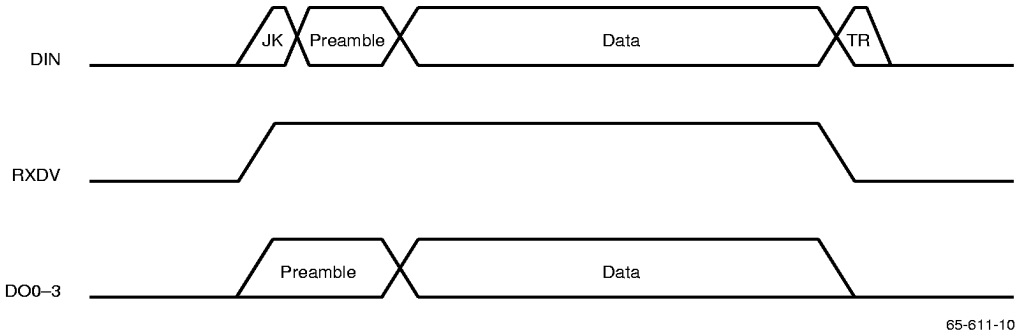


Figure 7. Frame Sequence—Receive

Advanced Information

Timing Diagrams (continued)

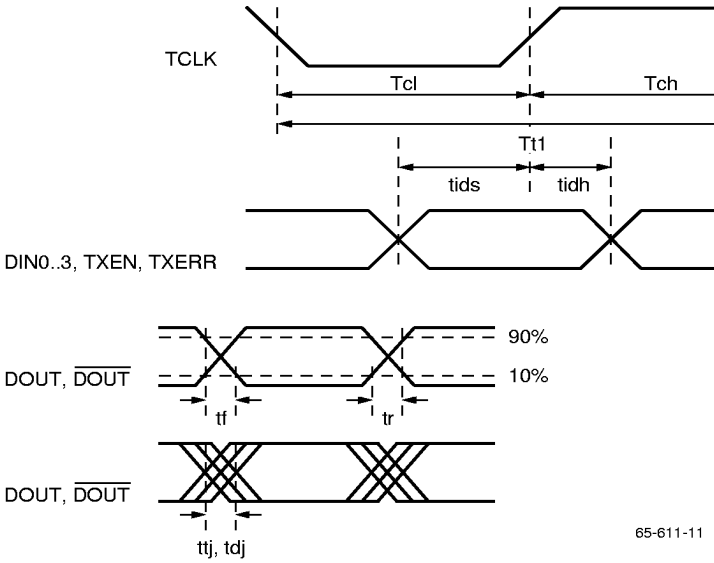


Figure 8. Transmitter Timing

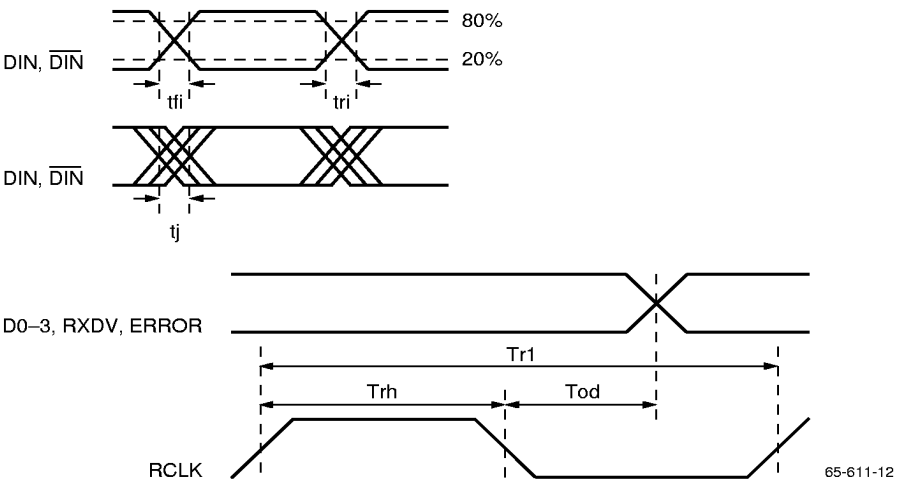


Figure 9. Receiver Timing

Advanced Information

Applications Discussion

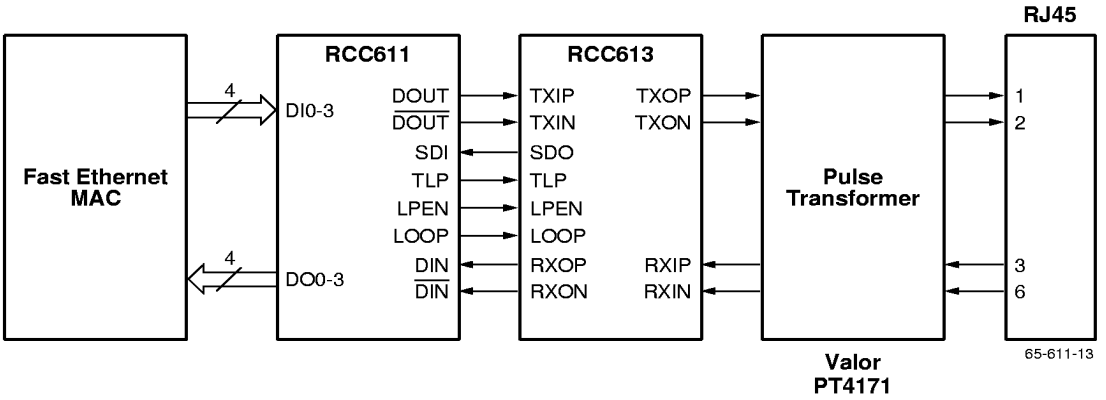


Figure 10. Typical Application

Advanced Information

Notes:

Notes:

Advanced Information

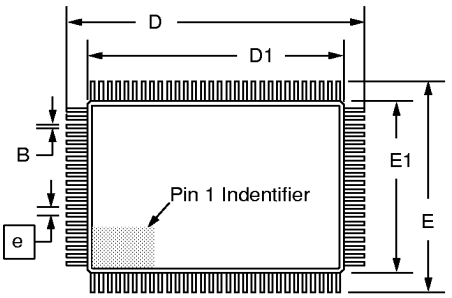
Mechanical Dimensions

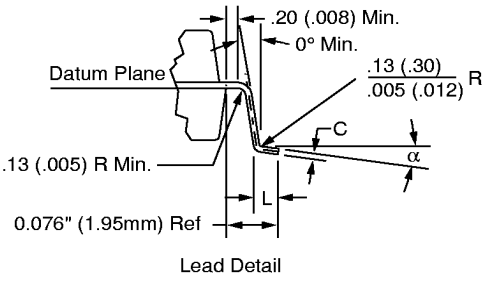
100 Lead MQFP 14x20mm Package—3.9mm Footprint

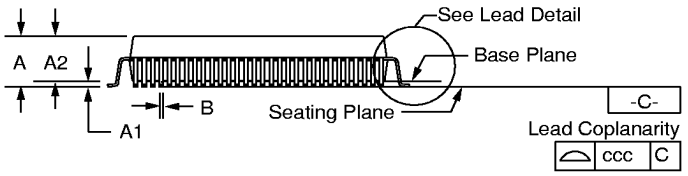
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.134	—	3.40	
A1	.010	—	.25	—	
A2	.100	.120	2.55	3.05	
B	.008	.015	.22	.38	3, 5
C	.005	.009	.13	.23	5
D	.922	.942	23.65	24.15	
D1	.783	.791	19.90	20.10	
E	.688	.708	17.65	18.15	
E1	.547	.555	13.90	14.10	
e	.0256 BSC		.65 BSC		
L	.028	.040	.73	1.03	4
N	100		100		
ND	30		30		
NE	20		20		
α	0°	7°	0°	7°	
ccc	—	.005	—	.12	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.







Advanced Information

Ordering Information

Product Number	Package
RCC611KR	100 Lead MQFP

Advanced Information

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Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel:1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Center, 5 Canto Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel:+852 2737-7200
Fax:+852 2314-0061

National Semiconductor Japan Ltd.
Tel:81-3-5620-6175
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