IBM11M8735C
IBM11M8735CB

8M x 72 DRAM MODULE

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 8Mx72 Dual Bank Extended Data Out Mode DIMM
- Performance:

		-50	-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	50ns	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	18ns	20ns	25ns
t_{AA}	Access Time From Address	30ns	35ns	40ns
t_{RC}	Cycle Time	89ns	104ns	124ns
t_{HPC}	EDO Mode Cycle Time	20ns	25ns	30ns

- All inputs and outputs are LVTTL (3.3V) or TTL (5.0V) compatible
- Single 3.3V ± 0.3V or 5.0V ± 0.5V Power Supply
- Au contacts
- Optimized for ECC applications
- System Performance Benefits:

  -Buffered inputs (except $\overline{RAS}$, Data)
  -Reduced noise (32 V_{SS}/V_{CC} pins)
  -4 Byte Interleave enabled
  -Buffered PDs
- Extended Data Out (EDO) Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only, CBR and Hidden Refresh
- 4096 refresh cycles distributed across 64ms
- 12/10 addressing (Row/Column)
- Card size: 5.25" x 1.5" x 0.354"
- DRAMs in SOJ Package

Description

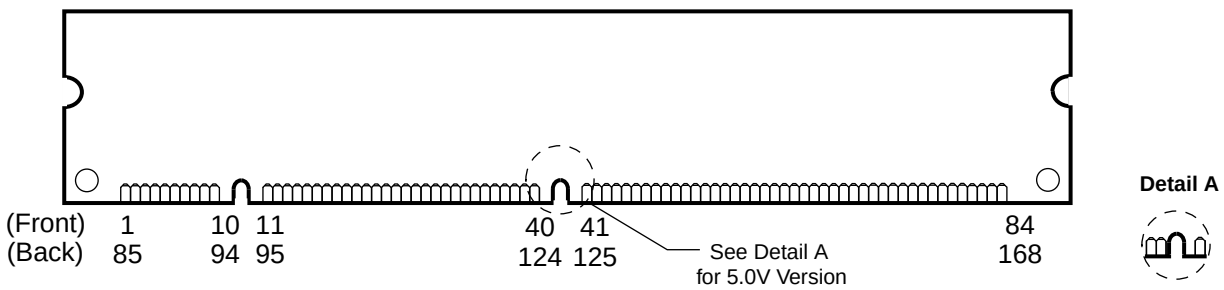
IBM11M8735C is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as an 8Mx72 high speed memory array, designed with EDO DRAMs for ECC applications, and is configured as 2 4Mx72 banks. The DIMM uses 36 4Mx4 EDO DRAMs in SOJ packages. The use of EDO DRAMS allows for a reduction in Page Mode Cycle time from 40ns (Fast Page) to 25ns for 60ns DRAM modules.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 50ns, 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, the system will determine that ECC DIMMs are installed if PD8 is low (0). ID0 need not be sensed since both x72 and x80 ECC DIMMs will function in a x72 bank.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

Card Outline (3.3V)



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Pin Description

$\overline{RAS}0$, $\overline{RAS}1$, $\overline{RAS}2$, $\overline{RAS}3$	Row Address Strobe	V_{CC}	Power (3.3V or 5.0V)
$\overline{CAS}0$, $\overline{CAS}1$, $\overline{CAS}4$, $\overline{CAS}5$	Column Address Strobe (Buffered)	V_{SS}	Ground
$\overline{WE}0$, $\overline{WE}2$	Read/write Input (Buffered)	NC	No Connect
$\overline{OE}0$, $\overline{OE}2$	Output Enable (Buffered)	PD1 - PD8	Presence Detects (Buffered)
A0, B0, A1 - A11	Address Inputs (Buffered)	$\overline{PDE}$	Presence Detect Enable
DQx	Data Input/Output	ID0 - ID1	ID Bits

Pinout

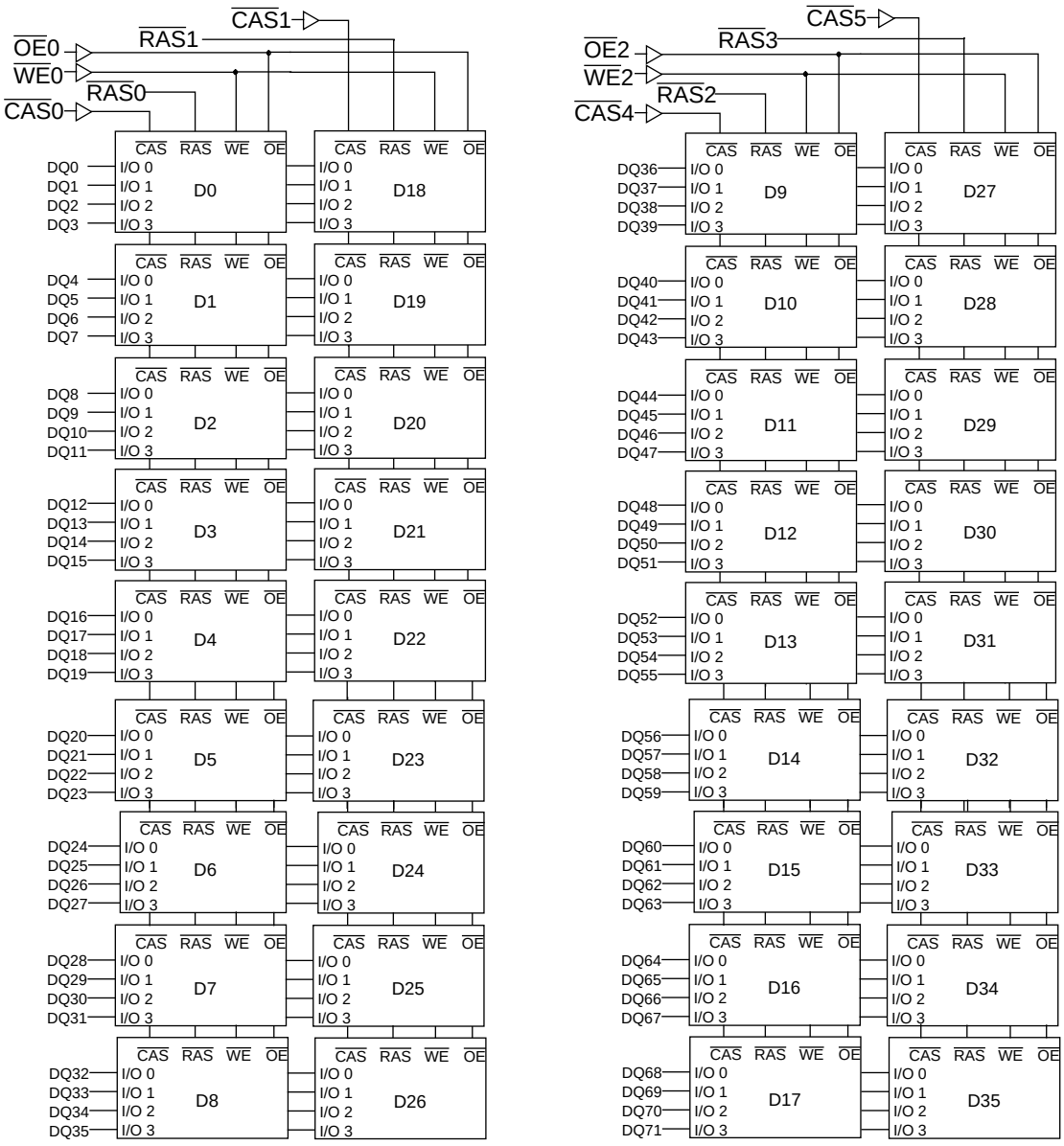
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	22	DQ17	106	DQ53	43	V_{SS}	127	V_{SS}	64	NC	148	NC
2	DQ0	86	DQ36	23	V_{SS}	107	V_{SS}	44	$\overline{OE}2$	128	NC	65	DQ25	149	DQ61
3	DQ1	87	DQ37	24	NC	108	NC	45	$\overline{RAS}2$	129	$\overline{RAS}3$	66	DQ26	150	DQ62
4	DQ2	88	DQ38	25	NC	109	NC	46	$\overline{CAS}4$	130	$\overline{CAS}5$	67	DQ27	151	DQ63
5	DQ3	89	DQ39	26	V_{CC}	110	V_{CC}	47	NC	131	NC	68	V_{SS}	152	V_{SS}
6	V_{CC}	90	V_{CC}	27	$\overline{WE}0$	111	NC	48	$\overline{WE}2$	132	$\overline{PDE}$	69	DQ28	153	DQ64
7	DQ4	91	DQ40	28	$\overline{CAS}0$	112	$\overline{CAS}1$	49	V_{CC}	133	V_{CC}	70	DQ29	154	DQ65
8	DQ5	92	DQ41	29	NC	113	NC	50	NC	134	NC	71	DQ30	155	DQ66
9	DQ6	93	DQ42	30	$\overline{RAS}0$	114	$\overline{RAS}1$	51	NC	135	NC	72	DQ31	156	DQ67
10	DQ7	94	DQ43	31	$\overline{OE}0$	115	NC	52	DQ18	136	DQ54	73	V_{CC}	157	V_{CC}
11	DQ8	95	DQ44	32	V_{SS}	116	V_{SS}	53	DQ19	137	DQ55	74	DQ32	158	DQ68
12	V_{SS}	96	V_{SS}	33	A0	117	A1	54	V_{SS}	138	V_{SS}	75	DQ33	159	DQ69
13	DQ9	97	DQ45	34	A2	118	A3	55	DQ20	139	DQ56	76	DQ34	160	DQ70
14	DQ10	98	DQ46	35	A4	119	A5	56	DQ21	140	DQ57	77	DQ35	161	DQ71
15	DQ11	99	DQ47	36	A6	120	A7	57	DQ22	141	DQ58	78	V_{SS}	162	V_{SS}
16	DQ12	100	DQ48	37	A8	121	A9	58	DQ23	142	DQ59	79	PD1	163	PD2
17	DQ13	101	DQ49	38	A10	122	A11	59	V_{CC}	143	V_{CC}	80	PD3	164	PD4
18	V_{CC}	102	V_{CC}	39	NC	123	NC	60	DQ24	144	DQ60	81	PD5	165	PD6
19	DQ14	103	DQ50	40	V_{CC}	124	V_{CC}	61	NC	145	NC	82	PD7	166	PD8
20	DQ15	104	DQ51	41	NC	125	NC	62	NC	146	NC	83	ID0	167	ID1
21	DQ16	105	DQ52	42	NC	126	B0	63	NC	147	NC	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Addr.	Leads	Dimension	Power	Notes
IBM11M8735C-60J	8Mx72	60ns	12/10	Au	5.25”x1.5”x 0.354”	5.0V	
IBM11M8735C-70J		70ns					
IBM11M8735CB-50J		50ns				3.3V	
IBM11M8735CB-60J		60ns					
IBM11M8735CB-70J		70ns					

Block Diagram



Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby		H	H→X	X	X	X	X	X	High Impedance
Read		L	L	H	L	Row	Col	X	Valid Data Out
Early-Write		L	L	L	X	Row	Col	X	Valid Data In
Late-Write		L	L	H→L	H	Row	Col	X	Valid Data In
RMW		L	L	H→L	L→H	Row	Col	X	Valid Data Out, Valid Data In
EDO Page Mode - Read 1st Cycle		L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles		L	H→L	H	L	N/A	Col	X	Valid Data Out
EDO Page Mode - Write 1st Cycle		L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles		L	H→L	L	X	N/A	Col	X	Valid Data In
EDO Page Mode - RMW 1st Cycle		L	H→L	H→L	L→H	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles		L	H→L	H→L	L→H	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh		L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	X	X	X	High Impedance
Hidden Refresh	Read	L→H→L	L	H	L	Row	Col	X	Data Out
	Write	L→H→L	L	H	X	Row	Col	X	Data In
Read Presence Detects		X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-50	-60	-70
PD1 (PD1 - PD4: Addressing/Density)	0	0	0
PD2	0	0	0
PD3	1	1	1
PD4	1	1	1
PD5 (EDO Detection)	1	1	1
PD6 (PD6 - PD7: Speed)	0	1	0
PD7	0	1	1
PD8 (Parity/ECC Designator)	0	0	0
ID0 (DIMM Type/Width)	0	0	0
ID1 (Refresh Mode)	0	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)
3. $\overline{PDE}$ should be tied high or low at system level if not used

Absolute Maximum Ratings

Symbol	Parameter	Rating (3.3V)	Rating (5.0V)	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +4.6	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C	1
P_D	Power Dissipation	11.0	16.8	W	1, 2
I_{OUT}	Short Circuit Output Current	50	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.
2. Maximum power occurs when all banks are active (refresh cycle).

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3V			5.0V			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 1.2V for pulse widths of ≤ 4.0ns with 3.3 Volt, or V_{CC} + 2.0V for pulse widths of ≤ 4.0ns (or V_{CC} + 1.0V for ≤ 8.0ns) with 5.0 Volt. Additionally, V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns (or -1.0V for ≤ 8.0ns). Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3V ± 0.3V or 5.0V ± 0.5V)

Symbol	Parameter		Max	Units
C_{I1}	Input Capacitance	A0, B0	13	pF
		A1 - A11	18	
C_{I2}	Input Capacitance ($\overline{RAS}$)		80	pF
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)		18	pF
C_{I4}	Input Capacitance ($\overline{PDE}$)		18	pF
C_{IO1}	Input/Output Capacitance (DQx)		22	pF
C_{O1}	Output Capacitance (PD)		15	pF
C_{O2}	Output Capacitance (ID)		5	pF

DC Electrical Characteristics (T_A= 0 to +70˚C, V_{CC}= 3.3V ± 0.3V or V_{CC}= 5.0V ± 0.5V)

Symbol	Parameter		Min.	Max.	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min.)	-50	—	1566	mA	1, 2, 3
		-60	—	1386		
		-70	—	1206		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		—	72	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min)	-50	—	1566	mA	1, 3, 4
		-60	—	1386		
		-70	—	1206		
I_{CC4}	EDO Page Mode Current Average Power Supply Current, EDO Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{HPC} = t_{HPC} min)	-50	—	1566	mA	1, 2, 3
		-60	—	1206		
		-70	—	1026		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	36	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-50	—	1566	mA	1, 3, 4
		-60	—	1386		
		-70	—	1206		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} + 0.3V)), All Other Pins Not Under Test = 0V	$\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0, B0	-10	+10	µA	
		A1 - A11, DQ	-20	+20		
		$\overline{RAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output Level (TTL) Output “H” Level Voltage (I_{OUT} = -2.5mA for 3.3V, or I_{OUT} = -5mA for 5.0V)		2.4	V_{CC}	V	
V_{OL}	Output Level (TTL) Output “L” Level Voltage (I_{OUT} = +2.1mA for 3.3V, or I_{OUT} = +4.2mA for 5.0V)		0.0	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ =V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ =V_{IH}.
4. Refresh current is specified for 1 bank active and 1 bank standby.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3V ± 0.3V or 5.0V ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns maximum delay, no pulse shrinkage to the DRAM device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAMs access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 2ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-50		-60		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	89	—	104	—	124	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	35	—	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	8	—	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10K	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	8	10K	10	10K	12	10K	ns	
t_{ASR}	Row Address Setup Time	5	—	5	—	5	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	2	—	2	—	2	—	ns	
t_{CAH}	Column Address Hold Time	10	—	10	—	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	12	32	12	40	12	45	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	20	10	25	10	30	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	13	—	15	—	17	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	43	—	48	—	53	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	18	—	20	—	25	—	ns	3
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	-2	—	ns	4
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	-2	—	ns	4
t_T	Transition Time (Rise and Fall)	2	30	2	30	2	30	ns	

1. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
3. Either t_{CDD} or t_{ODD} must be satisfied.
4. Either t_{DZC} or t_{DZO} must be satisfied.

Write Cycle

Symbol	Parameter	-50		-60		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	2	—	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	9	—	12	—	14	—	ns	
t_{WP}	Write Command Pulse Width	7	—	10	—	12	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	12	—	15	—	17	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	9	—	12	—	14	—	ns	
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	-2	—	ns	2
t_{DH}	D_{IN} Hold Time	12	—	15	—	17	—	ns	2

1. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.)and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-50		-60		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	50	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	18	—	20	—	25	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	—	40	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	18	—	20	—	25	ns	1, 2
t_{RCS}	Read Command Setup Time	2	—	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	2	—	ns	
t_{OES}	$\overline{OE}$ setup time prior to $\overline{CAS}$	7	—	10	—	10	—	ns	
t_{ORD}	$\overline{OE}$ setup time prior to $\overline{RAS}$ (Hidden Refresh)	2	—	5	—	5	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	18	—	20	—	20	—	ns	5
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	18	2	20	2	20	ns	4
t_{OFF}	Output Buffer Turn-off Delay	2	18	2	20	2	20	ns	4, 6

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, $t_{AA,}$ t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
5. Either t_{CDD} or t_{ODD} must be satisfied.
6. t_{OFF} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever is last.

Read-Modify-Write Cycle

Symbol	Parameter	-50		-60		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	123	—	143	—	170	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	70	—	82	—	97	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40	—	44	—	54	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50	—	57	—	67	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	7	—	10	—	12	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.)and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

EDO Mode Cycle

Symbol	Parameter	-50		-60		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{HCAS}	$\overline{CAS}$ Pulse Width (EDO Page Mode)	8	10K	10	10K	12	10K	ns	
t_{HPC}	EDO Page Mode Cycle Time (Read/Write)	20	—	25	—	30	—	ns	
t_{HPRWC}	EDO Page Mode Read Modify Write Cycle Time	63	—	72	—	84	—	ns	
t_{DOH}	Data-out Hold Time from $\overline{CAS}$	10	—	10	—	10	—	ns	
t_{WHZ}	Output buffer Turn-Off Delay from $\overline{WE}$	2	15	2	15	2	20	ns	
t_{WPZ}	$\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High	7	—	10	—	10	—	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	—	45	ns	1
t_{RASP}	EDO Page Mode $\overline{RAS}$ Pulse Width	50	125K	60	125K	70	125K	ns	
t_{OEP}	$\overline{OE}$ High Pulse Width	10	—	10	—	10	—	ns	
t_{OEHC}	$\overline{OE}$ High Hold Time from $\overline{CAS}$ High	10	—	10	—	10	—	ns	

1. Measured with the specified current load and 100pF at V_{OL} = 0.8V and V_{OH} = 2.0V.

Refresh Cycle

Symbol	Parameter	-50		-60		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	8	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	3	—	ns	
t_{REF}	Refresh Period	—	64	—	64	—	64	ms	1

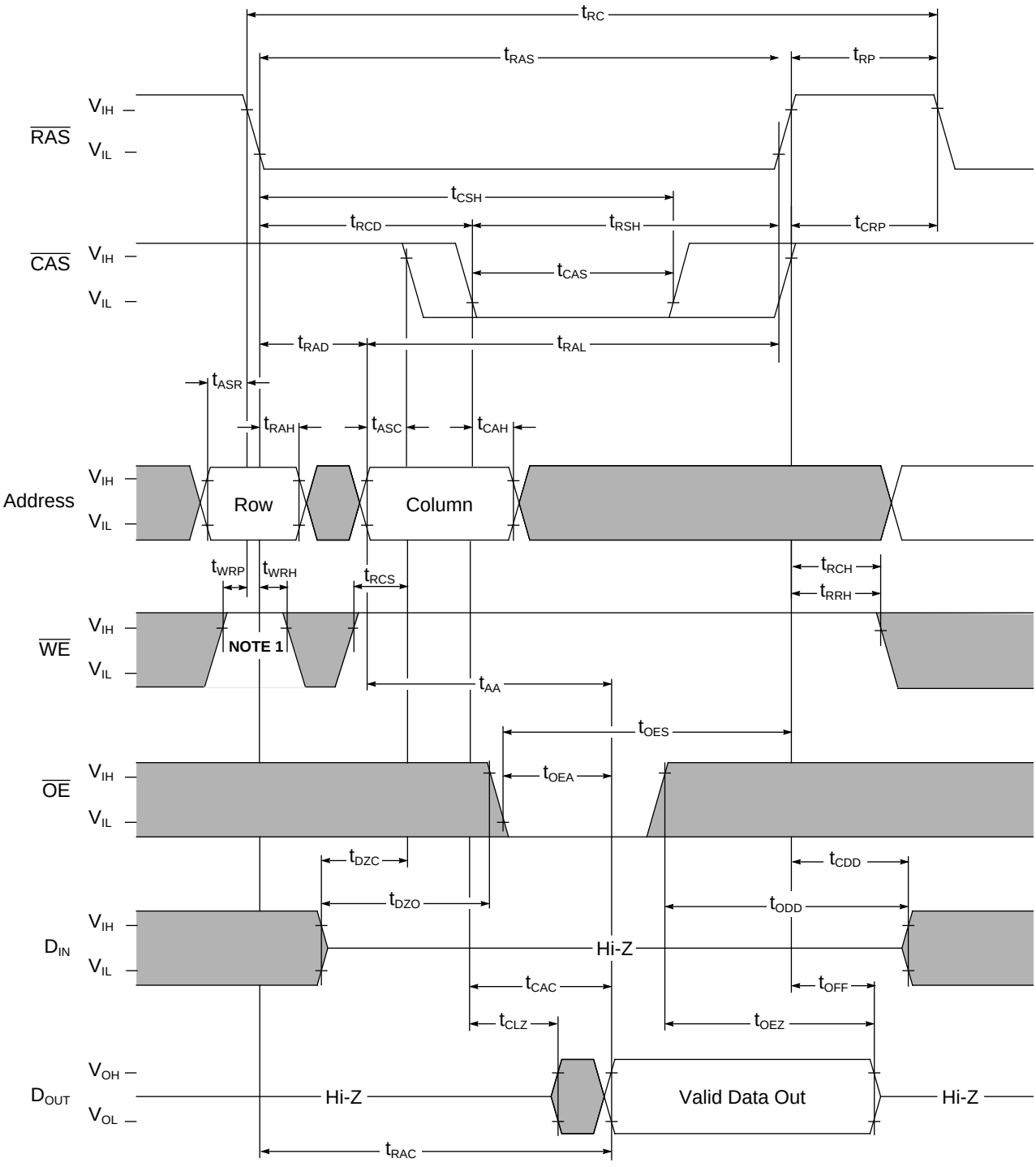
1. 4096 refreshes are required every 64ms.

Presence Detect Read Cycle

Symbol	Parameter	-50		-60		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

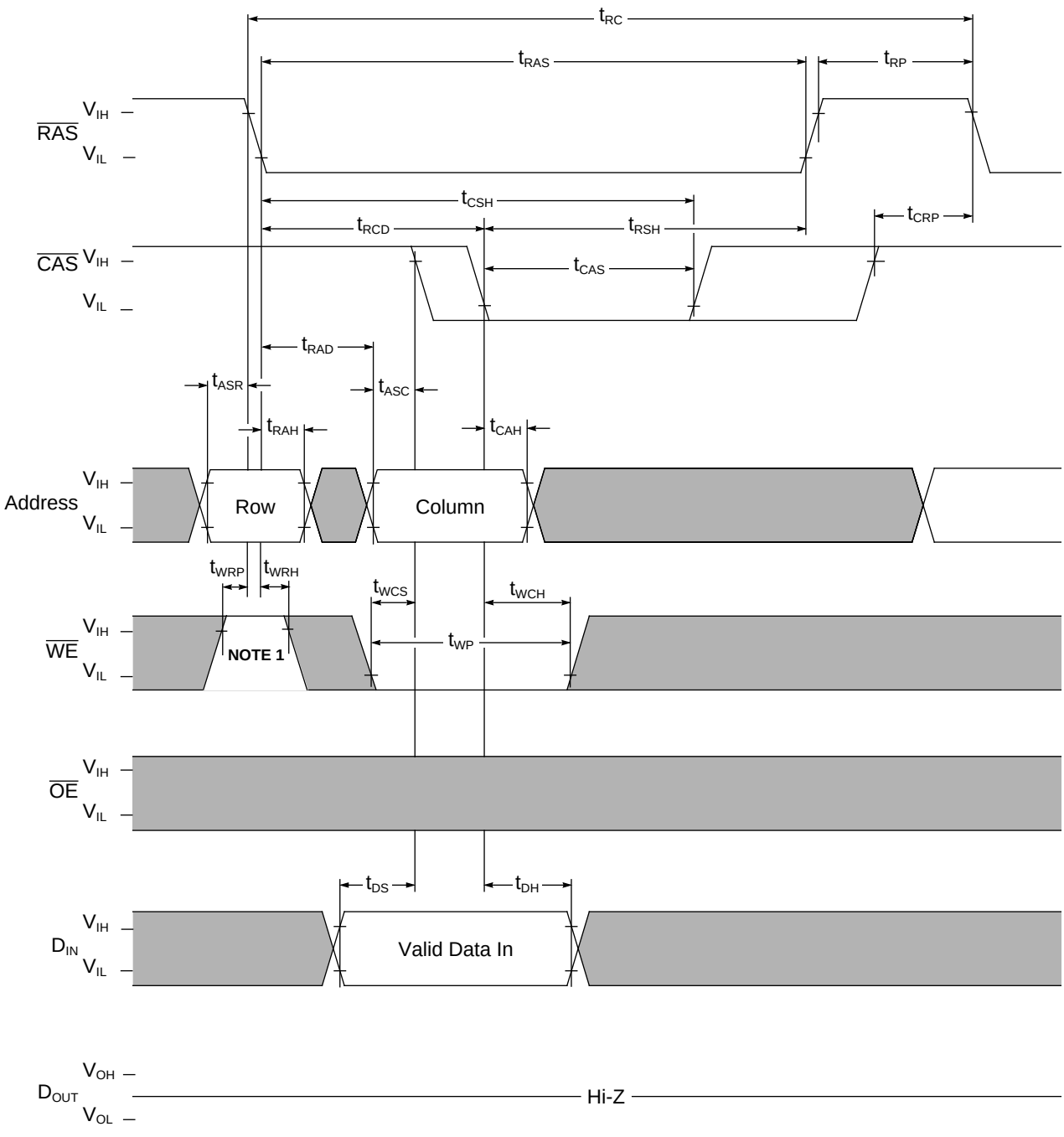
Read Cycle



: "H": or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

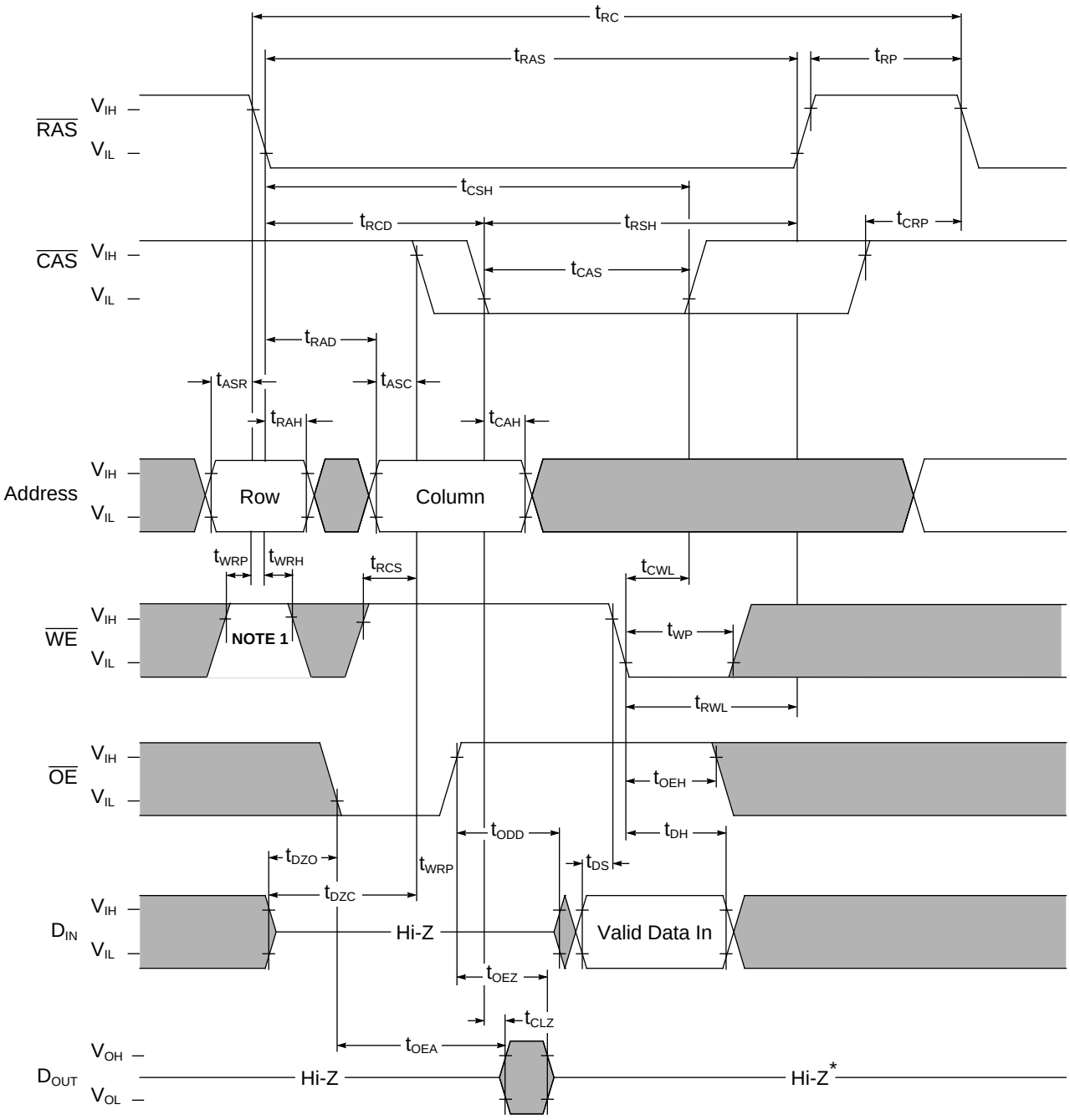
Write Cycle (Early Write)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

Write Cycle (Late Write)

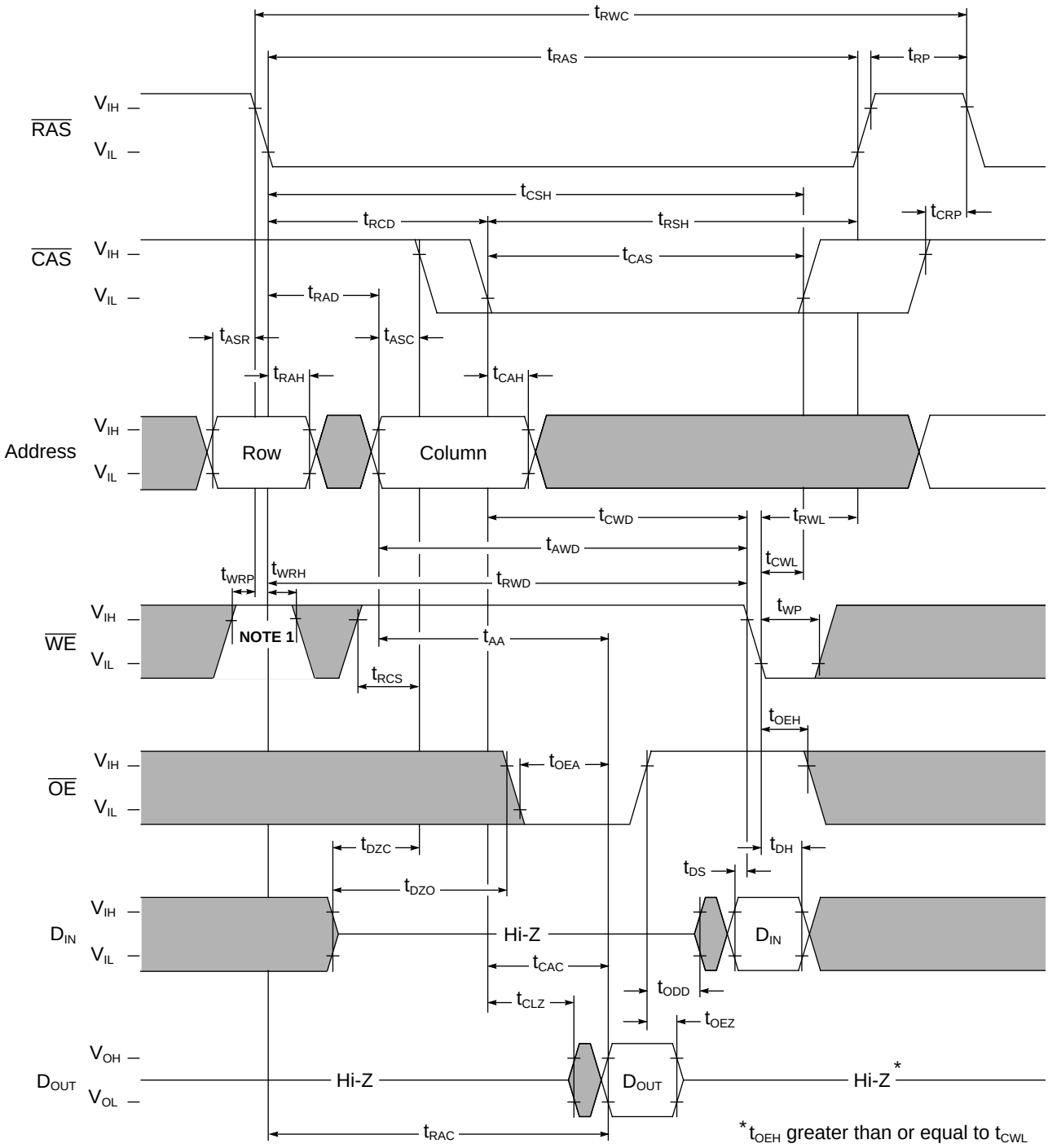


: "H" or "L"

* t_{OEH} greater than or equal to t_{CWL}

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

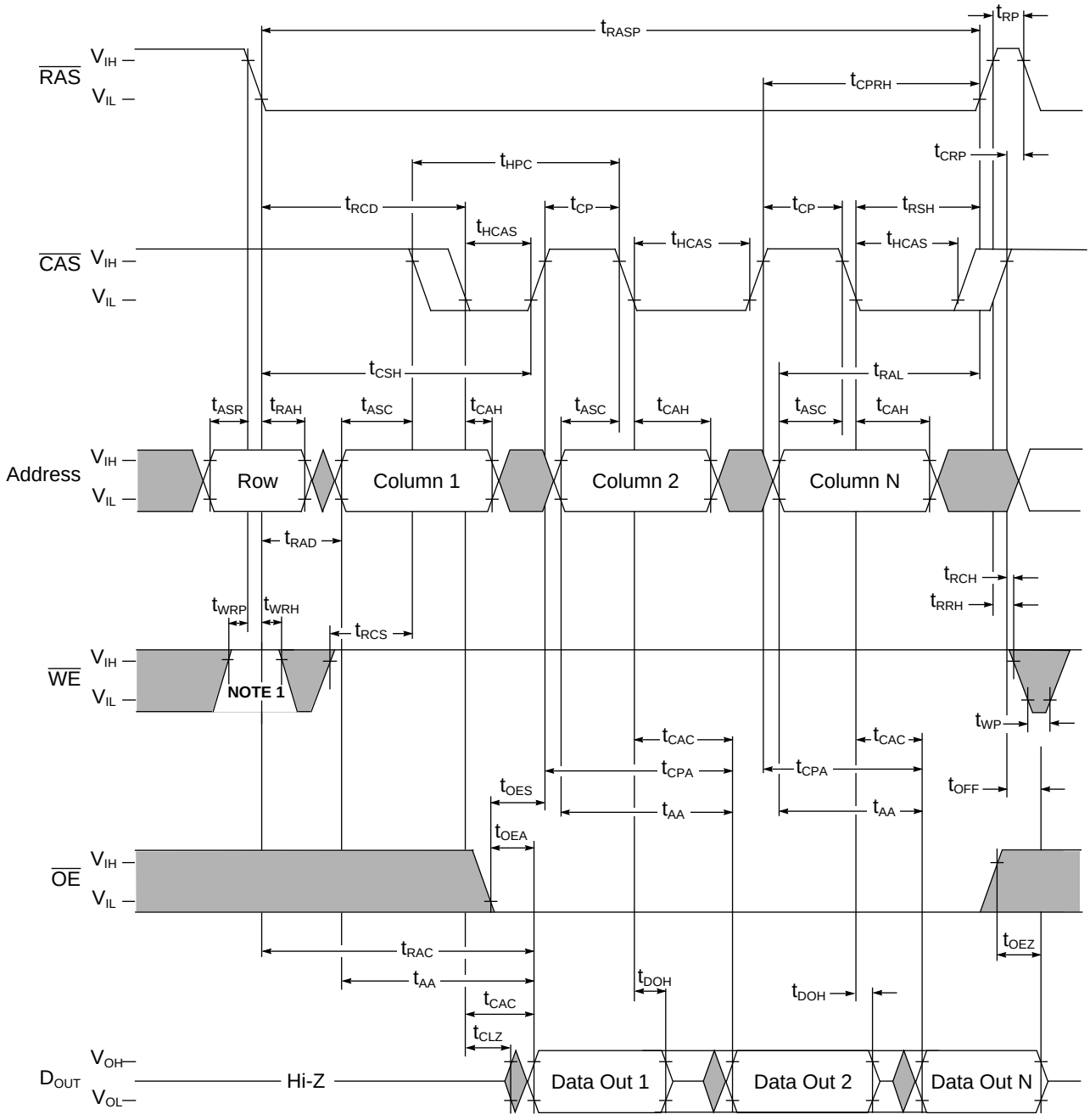
Read-Modify-Write-Cycle



: “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

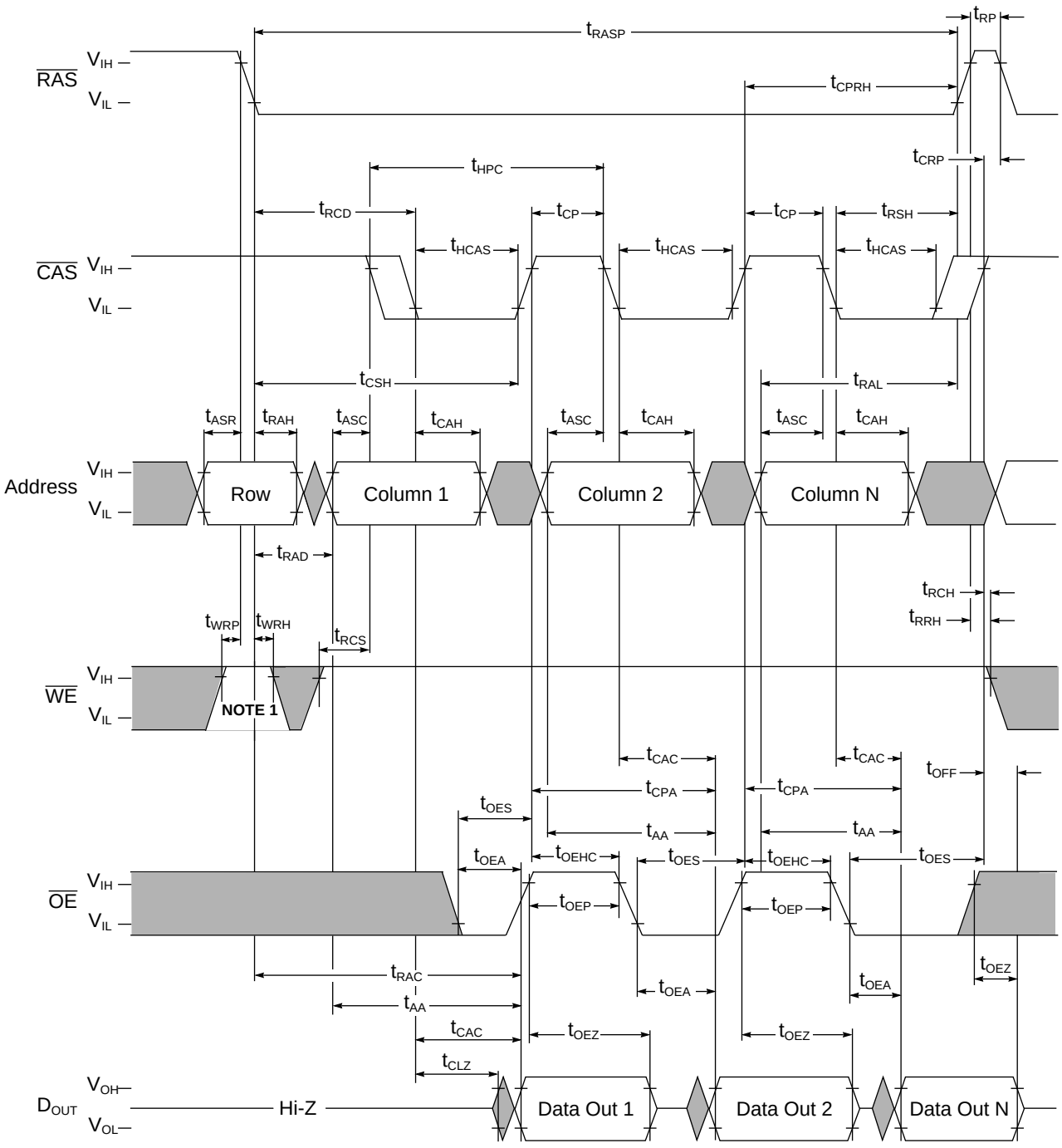
EDO Page Mode Read Cycle



: “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

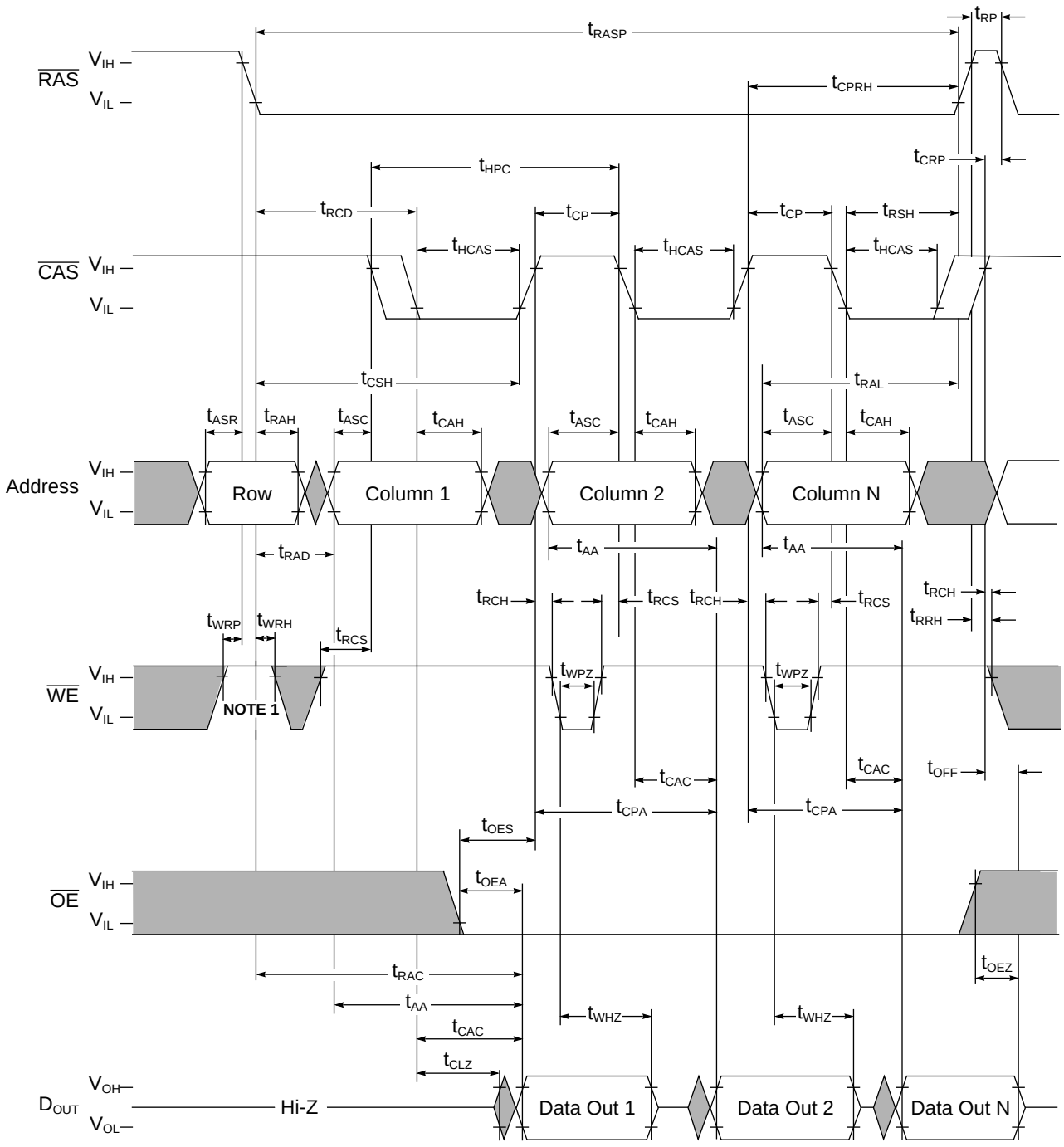
EDO Page Mode Read Cycle ($\overline{OE}$ Control)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

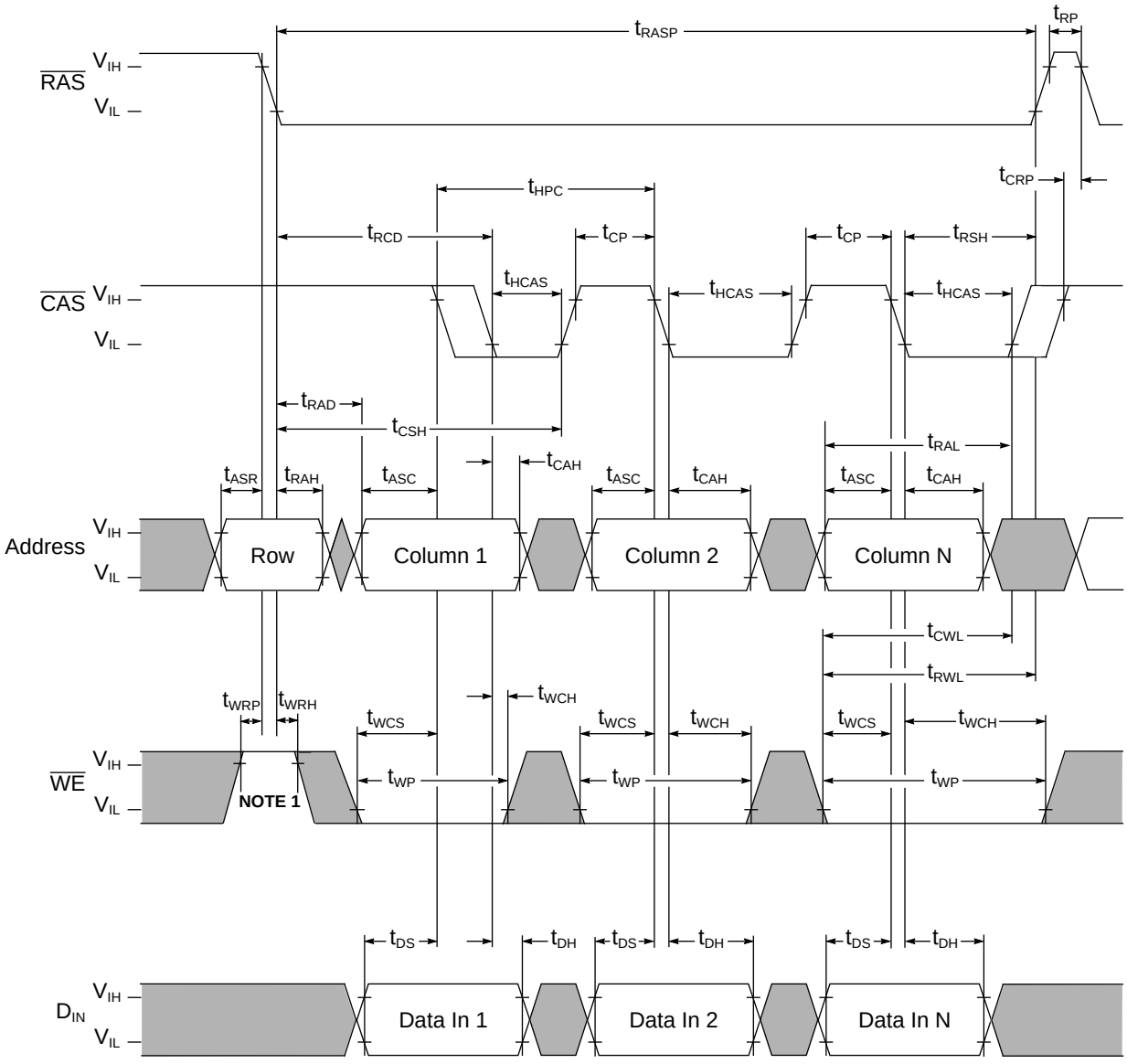
EDO Page Mode Read Cycle ($\overline{WE}$ Control)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

EDO Page Mode Early Write Cycle

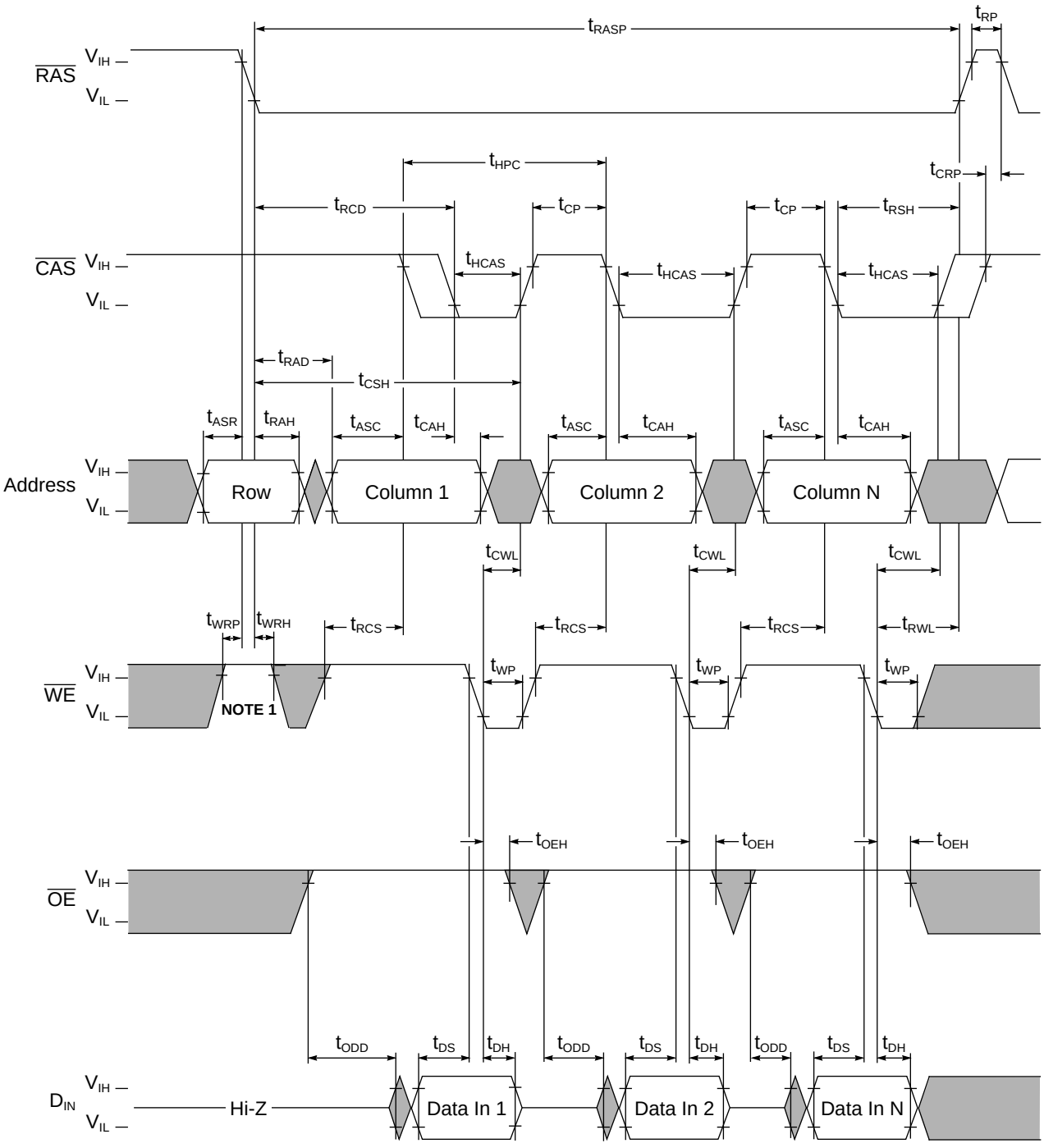


: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

$\overline{OE}$ = Don't care

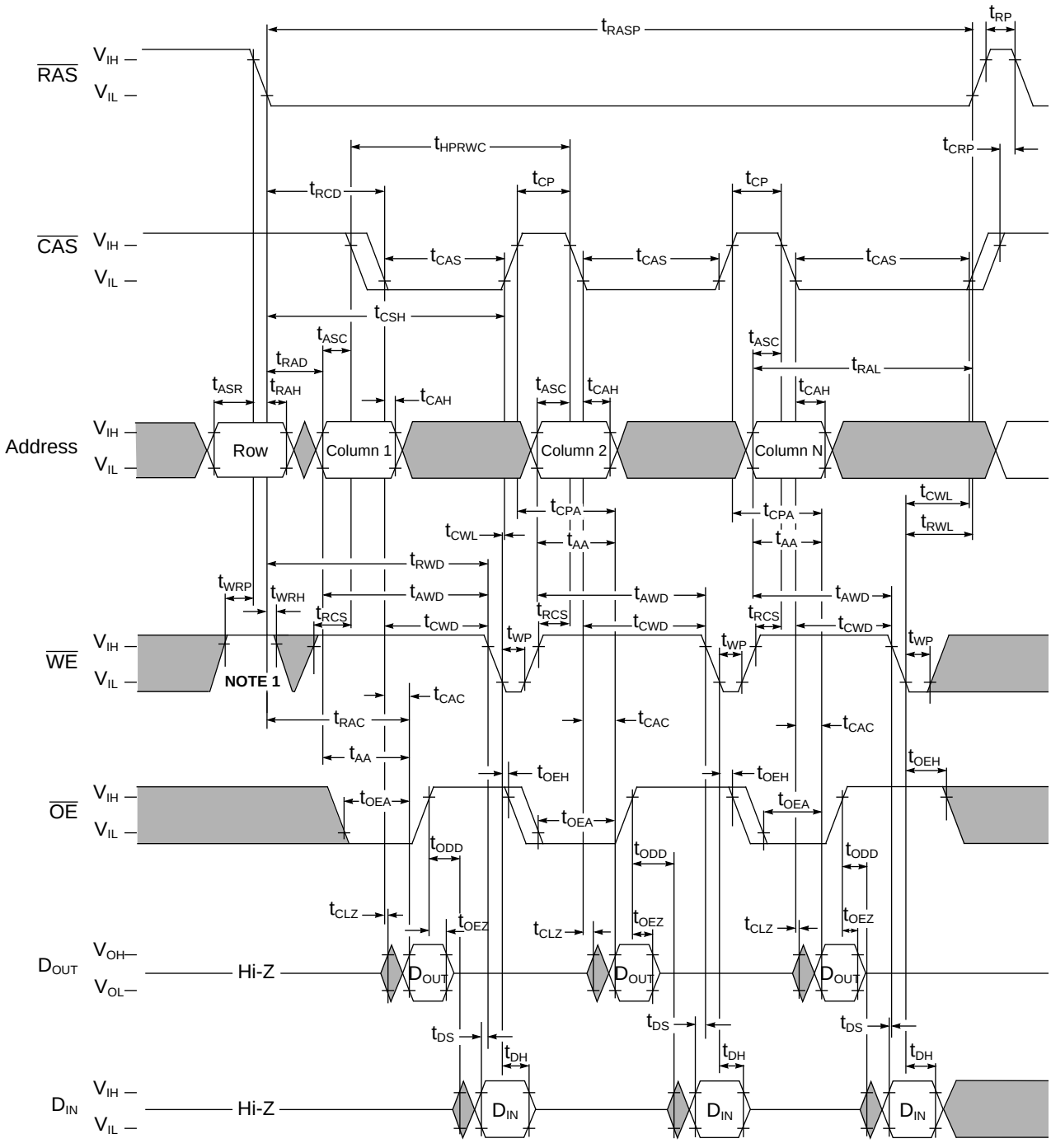
EDO Page Mode Late Write Cycle



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

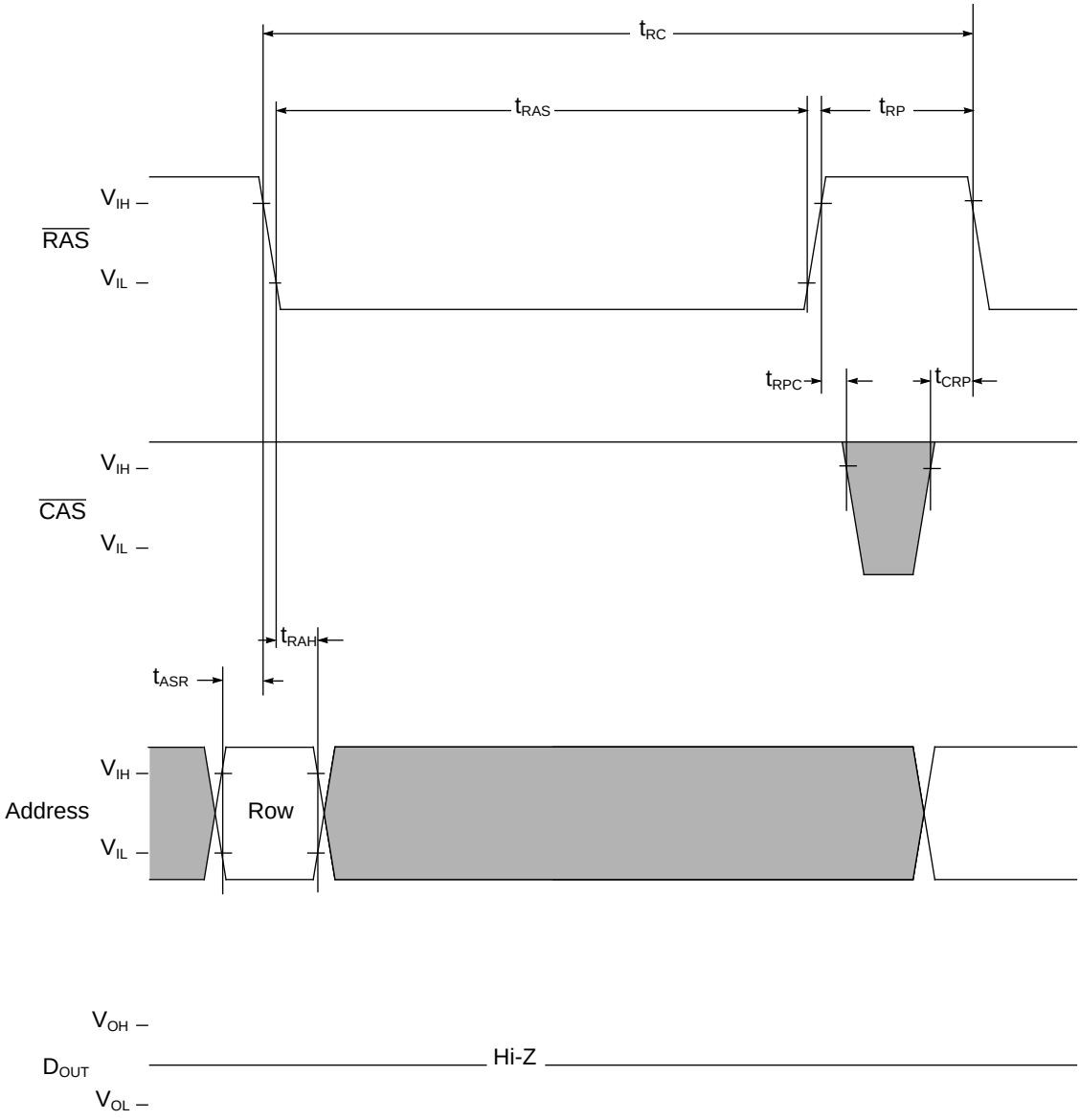
EDO Page Mode Read Modify Write Cycle



: “H” or “L”

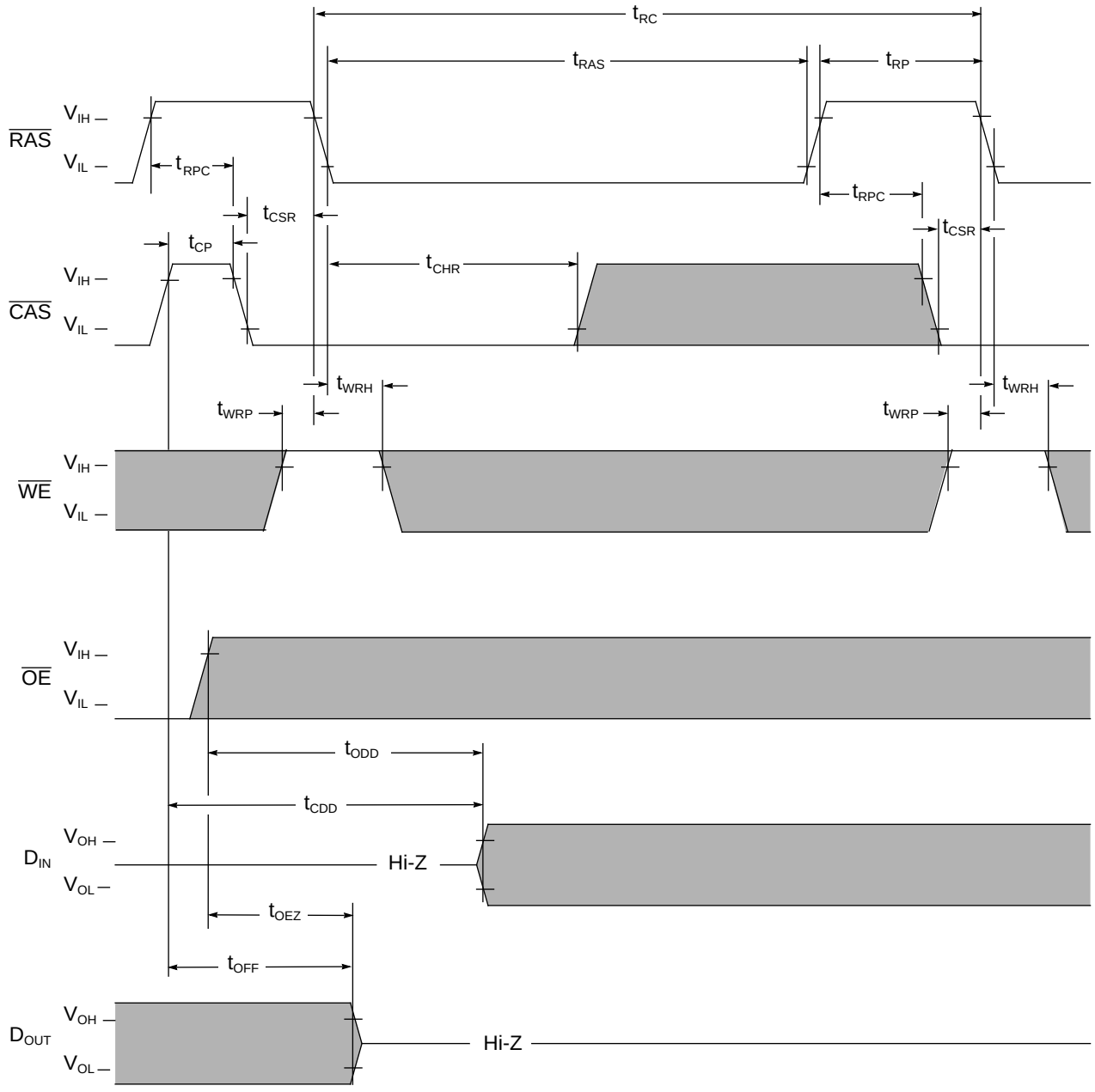
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

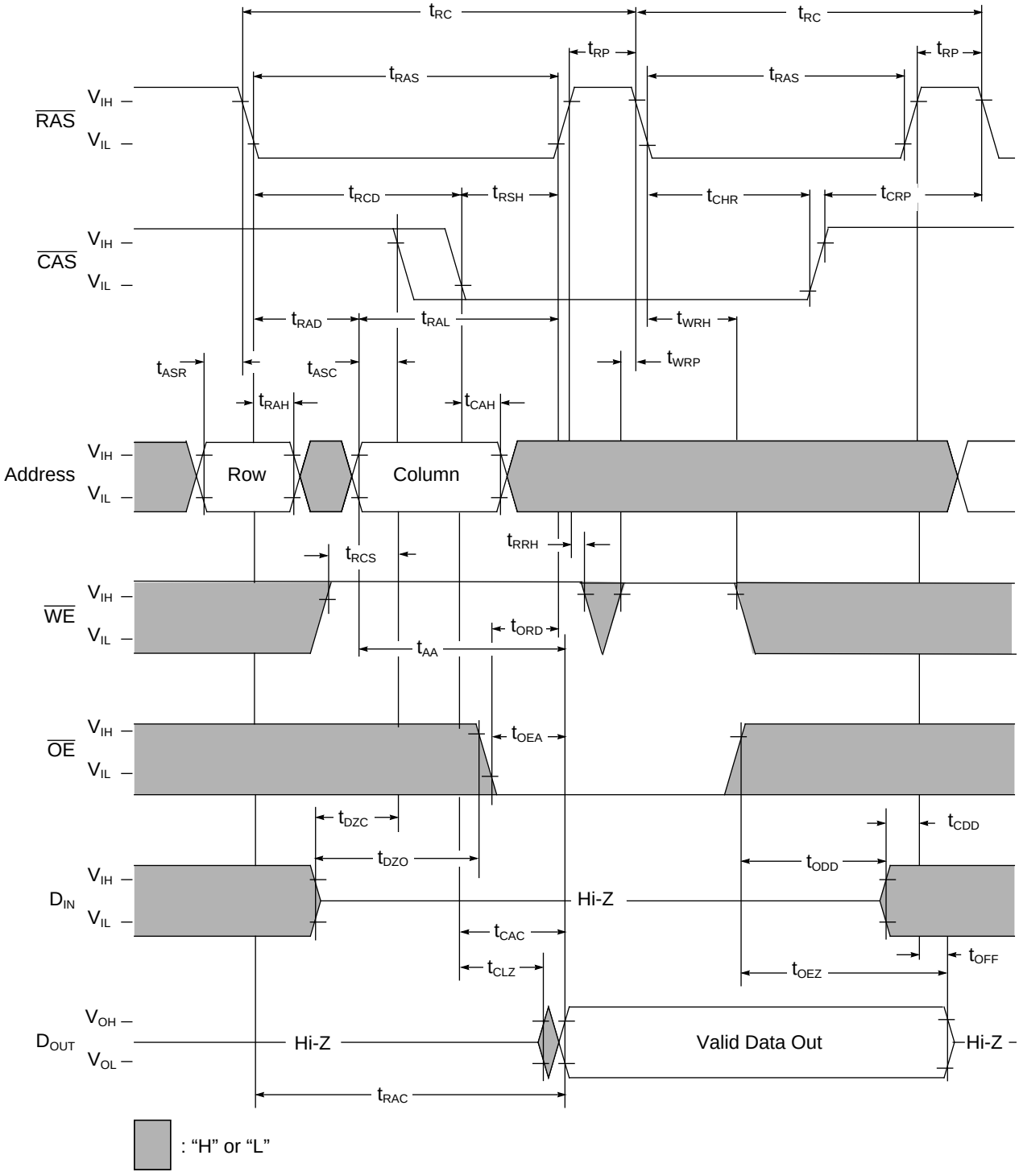
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



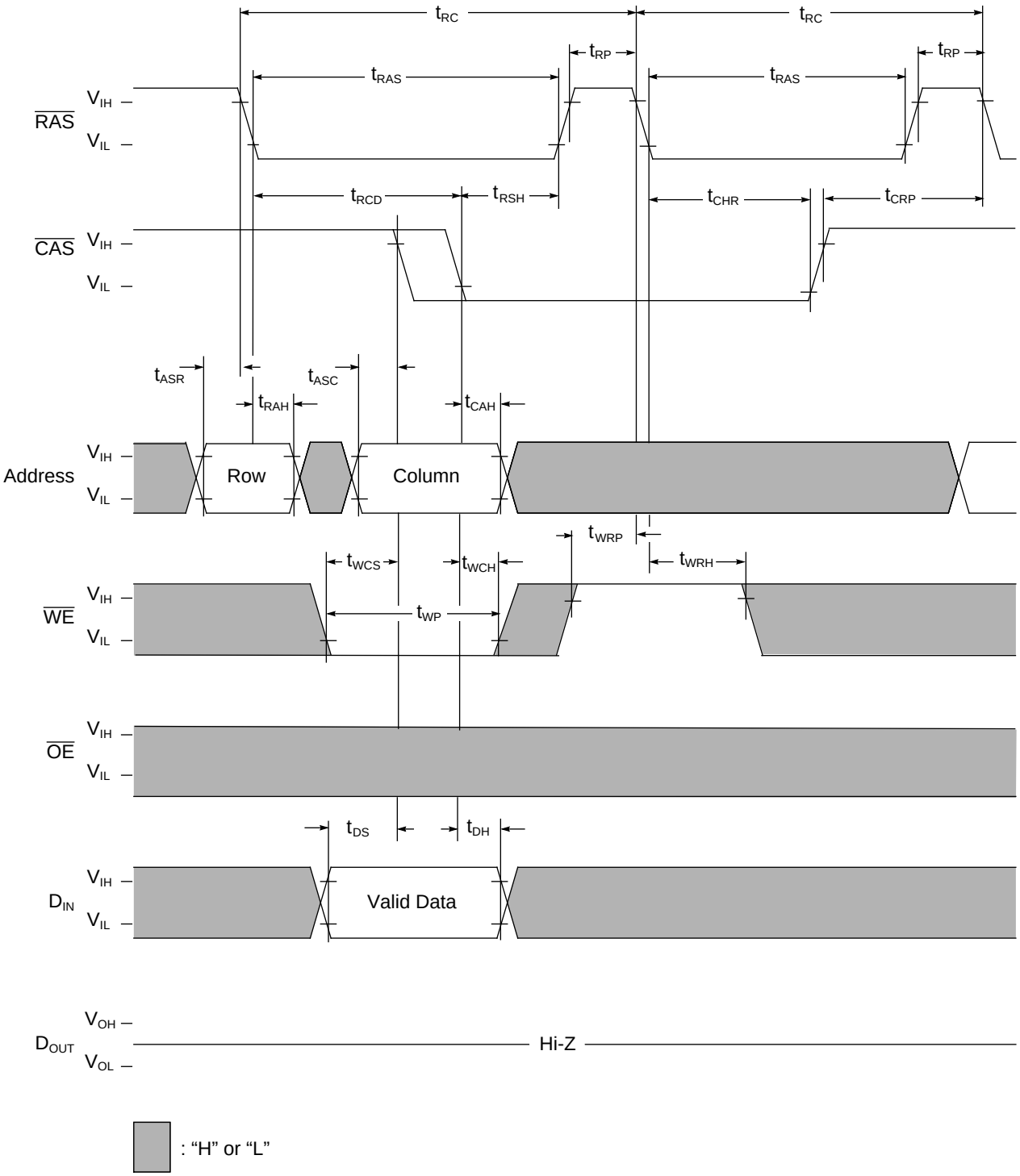
: "H" or "L"

NOTE: Address is "H" or "L"

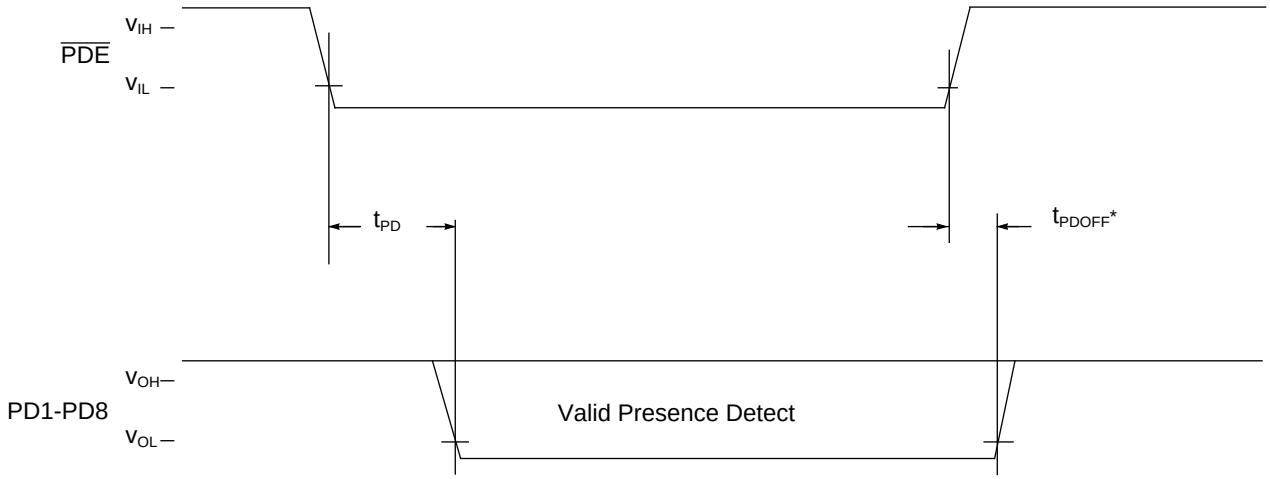
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

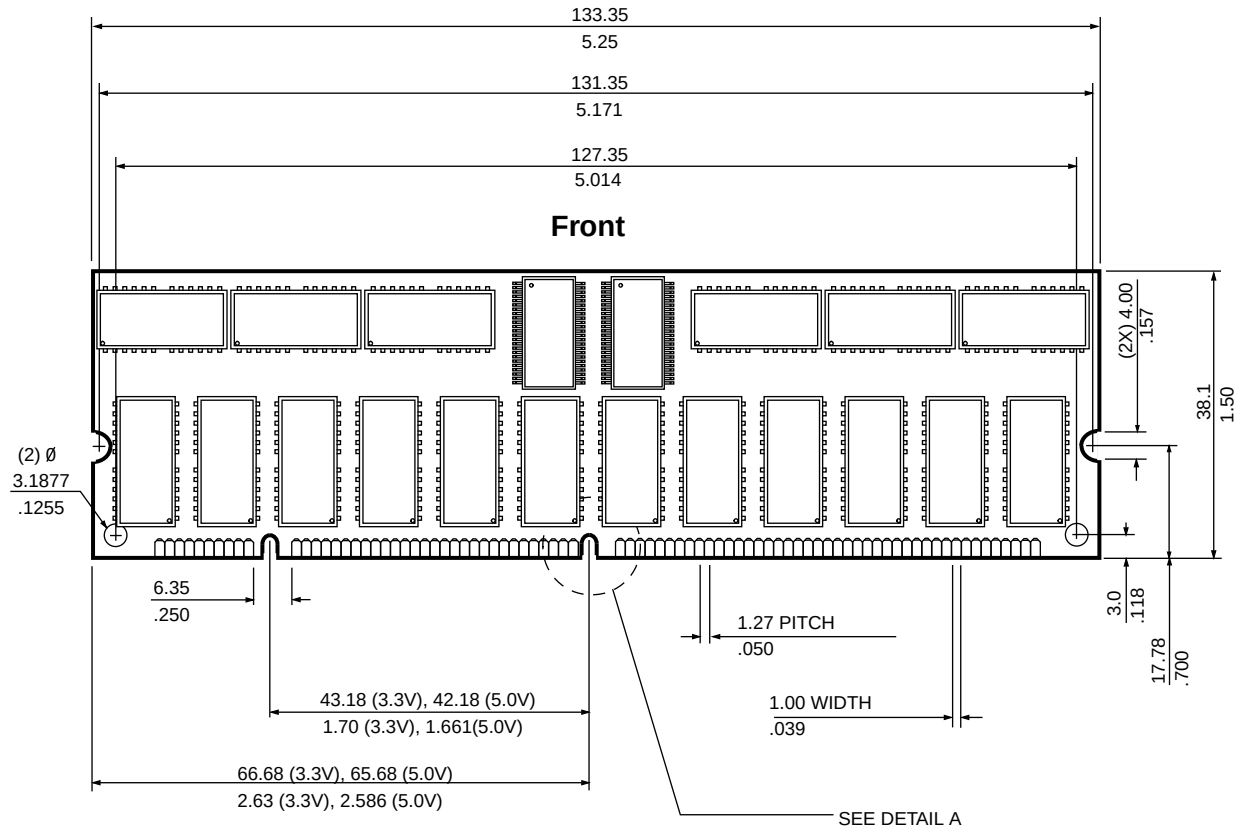


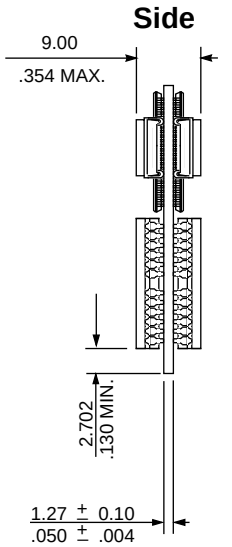
Presence Detect Read Cycle

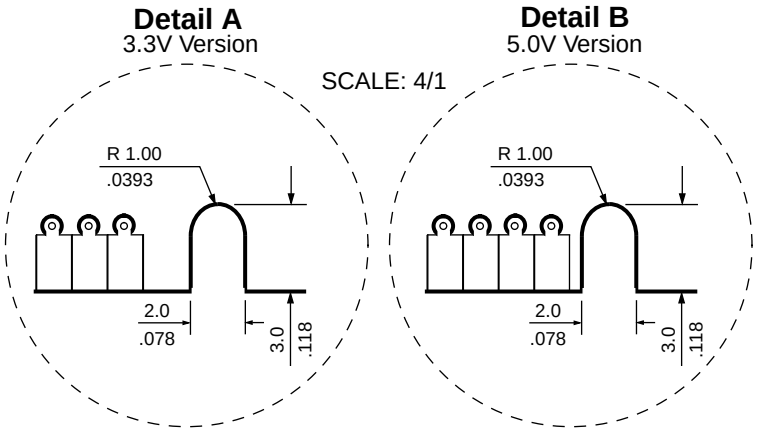


*PD pins must be pulled high at next level of assembly

Layout Drawing 3.3V/5.0V







Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Revision Log

Rev	Contents of Modification
1/96	Initial Release.
3/96	Increased timings: t_{OES}, t_{ORD} Improved timings: t_{CAH}, t_{CDD}, t_{OEZ}, t_{OFF} The CBR timing diagram was changed to allow $\overline{CAS}$ to remain low for back-to-back CBR cycles. Hidden Refresh Cycle (Read) timing diagram was changed to show data being turned off with $\overline{RAS}$ not $\overline{CAS}$
5/96	Updated ordering information
8/96	Corrected typo in performance table
12/96	Updated with 50ns speed sort

Discontinued (9/98 - last order; 3/99 - last ship)

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