Ordering number : ENN7972

SANYO Semiconductors
DATA SHEET

LC875BP4A
LC875BM2A
LC875BJ0A
LC875BH4A

CMOS IC
ROM 256K/224K/192K/176K byte, RAM 4096K byte on-chip
8-bit 1-chip Microcontroller

Overview

The LC875BP4A, LC875BM2A, LC875BJ0A, LC875BH4A is 8-bit single chip microcontroller with the following one-chip features :

- CPU : Operable at a minimum bus cycle time of 100ns
- On-chip ROM Capacity : LC875BP4A 256K bytes
  : LC875BM2A 224K bytes
  : LC875BJ0A 192K bytes
  : LC875BH4A 176K bytes
- On-chip RAM Capacity : 4K bytes
- Two high performance 16-bit timer/counters (can be divided into 8-bit timers)
- Four 8-bit timers with prescalers
- Timer for use as date/time clock
- Two synchronous serial I/O ports (with automatic block transmit/receive function)
- One asynchronous/synchronous serial I/O port
- Two UART ports (full duplex)
- 12-bit PWM × 4
- 12-channel × 8-bit AD converter
- High speed clock counter
- System clock divider
- 27-source 10-vectored interrupt system

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Features

■Read Only Memory (ROM)
- 262144 × 8-bits (LC875BP4A)
- 229376 × 8-bits (LC875BM2A)
- 196608 × 8-bits (LC875BJ0A)
- 180224 × 8-bits (LC875BH4A)

■Random Access Memory (RAM) : 4096 × 9-bit

■Bus Cycle Time
- 100ns (10MHz)

  Note : Bus cycle time indicates the speed to read ROM.

■Minimum Instruction Cycle Time (tCYC)
- 300ns (10MHz)

■Ports
- Input/output ports

Input/output programmable for each bit individually	64 (P1n, P2n, P3n, P70 to P73, P8n, PAn, PBn, PCn, S2Pn, PWM0, PWM1, XT2)
Data direction programmable in two bits	16 (PEn, PFn)
Data direction programmable in nibble units	8 (P0n)
• Input ports	1 (XT1)
• Oscillator pins	2 ($\overline{CF1}$, CF2)
• Reset pin	1 ($\overline{RES}$)
• Power supply	8 (V_{SS}1 to 4, V_{DD}1 to 4)

■Timer
- Timer 0 : 16-bit timer/counter with capture register
  - Mode 0 :8-bit timer with 8-bit programmable prescaler (with an 8-bit capture register) × 2-channels
  - Mode 1 :8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with 8-bit capture register)
  - Mode 2 :16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  - Mode 3 :16-bit counter (with a 16-bit capture register)
- Timer 1 : 16-bit timer/counter that support PWM/ toggle output
  - Mode 0 :8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter (with toggle outputs)
  - Mode 1 :8-bit PWM with an 8-bit prescaler × 2-channels
  - Mode 2 :16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (Toggle outputs also present at the lower-order 8-bits)
  - Mode 3 :16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8-bits can be used as PWM.)
- Timer 4 : 8-bit timer with a 6-bit prescaler
- Timer 5 : 8-bit timer with a 6-bit prescaler
- Timer 6 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  1. The clock is selectable from sub-clock (32.768kHz crystal oscillation), system clock or programmable prescaler output of timer 0.
  2. Interrupt are programmablein 5 different time schemes.

■High Speed Clock Counter
1. Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
2. Can generate output real time.

■Serial Interface

- SIO 0 : 8-bit synchronous serial interface
  1. LSB first/MSB first-function available
  2. An internal 8-bit baud-rate generator (maximum transmit clock period 4/3 tCYC)
  3. Consecutive automatic data communication (1 to 256-bits)

- SIO 1 : 8-bit asynchronous/synchronous serial interface
  Mode 0 : Synchronous 8-bit serial I_O (2-wire or 3-wire, transmit clock 2 to 512 tCYC)
  Mode 1 : Asynchronous serial I_O (half duplex, 8 data bits, 1 stop bit, baud-rate 8 to 2048 tCYC)
  Mode 2 : Bus mode 1 (start bit, 8 data bits, transmit clock 2 to 512 tCYC)
  Mode 3 : Bus mode 2 (start detection, 8 data bits, stop detection)

- SIO2 : 8-bit synchronous serial interface
  1. LSB-first
  2. Internal 8-bit baud-rate generator (maximum transmit clock period 4/3 tCYC)
  3. Consecutive automatic data communication (1 to 32 bytes)

■UART :2-channels

1. Full duplex
2. 7/8/9 bit data bits selectable
3. 1stop bit
4. built-in baudrate generator

■AD Converter

- 12-channel × 8-bit AD converter

■PWM

- 4-channel × synchronous variable 12-bit PWM

■ Remote Receiver Circuit (share with P73/INT3/T0IN terminal)

- Noise rejection function (The filtering time of the noise rejection filter (1tCYC/32 tCYC/128 tCYC) can be switched by program.)

■Watchdog Ttimer

- External RC circuit is required.
- Interrupt or system reset is activated when the timer overflows.

■Interrupts

- 27-source and 10-vectored interrupt function :
  1. Three interrupt priorities, low (L), high (H) and highest (X) are supported with multi-level nesting possible. During interrupt handling, an equal or lower level interrupt request is refused.
  2. If interrupt requests for two or more vector addresses occur at once, the higher level interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable Level	Interrupt Signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1, 2 receive
8	0003BH	H or L	SIO1/SIO2/UART1, 2 transmit
9	00043H	H or L	ADC/T6/T7/PWM4, PWM5
10	0004BH	H or L	Port 0/T4/T5/PWM0, PWM1

- Priority Level : X > H > L
- For equal priority levels, vector with lowest address takes precedence.

■Subroutine Stack Levels
- A maximum of 3072 levels (set stack inside RAM)

■Multiplication and division
- 16-bits × 8-bits (5 instruction-cycle times)
- 24-bits × 16-bits (12 instruction-cycle times)
- 16-bits ÷ 8-bits (8 instruction-cycle times)
- 24-bits ÷ 16-bits (12 instruction-cycle times)

■Oscillation Circuits
- Built-in RC oscillation circuit used for the system clock
- CF oscillation circuit used for the system clock
- Crystal oscillation circuit used for the system clock

■System Clock Divider
- Operable on the lowest power consumption
- Minimum instruction cycle time (300ns, 600ns, 1.2µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, 76.8µs can be switched by program (when using 10MHz main clock)

■Standby Function
- HALT mode

  The HALT mode stops program execution while the peripheral circuits keep operating and minimizes power consumption. This operation mode can be released by a system reset or an interrupt request.
- HOLD mode

  The HOLD mode stops program execution and all oscillation circuits : CF, RC and Crystal oscillations.
  This mode can be released by the following conditions.
  1. Supply "L" level to the reset terminal ($\overline{\text{RES}}$)
  2. Supply the selected level to at lease one of INT0, INT1, INT2, INT4, INT5.
  3. Supply an interrupt condition to Port 0.
- X'tal HOLD mode

  The X'tal HOLD mode stops program execution and all peripheral circuits except for the base timer. The crystal oscillator maintains its state at HOLD mode inception. This mode can be released by the following conditions.
  1. Supply "L" level to the reset terminal ($\overline{\text{RES}}$).
  2. Supply the selected level to at least one of INT0, INT1, INT2, INT4, INT5.
  3. Supply an interrupt condition to Port 0.
  4. Supply an interrupt condition to the base timer circuit.

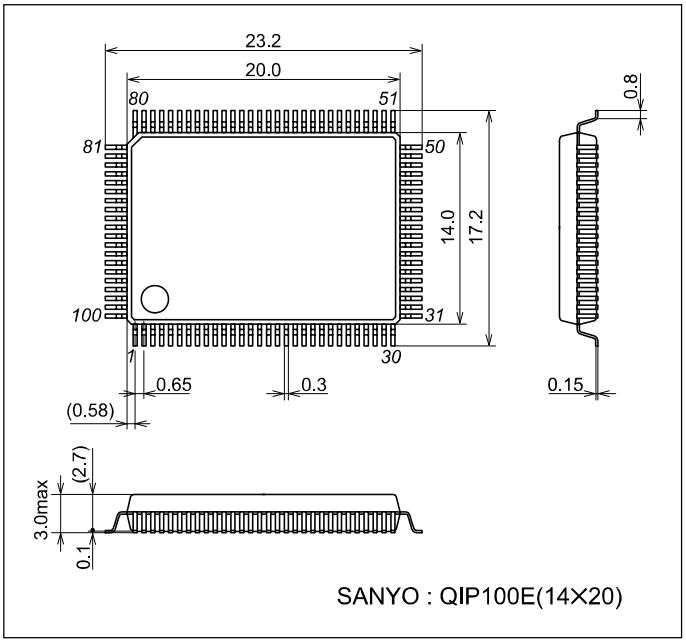
■Shipping Form
- QFP100E (Lead Free Product)
- TQFP100 (Lead Free Product)

■Development Tools
- Evaluation (EVA) chip : LC87EV690
- Emulator : EVA62S + ECB876600D + SUB875200 + POD100QFP or POD100SQFP Type B
  : ICE-B877300 + SUB875200 + POD100QFP or POD100SQFP Type B

Package Dimensions

unit : mm

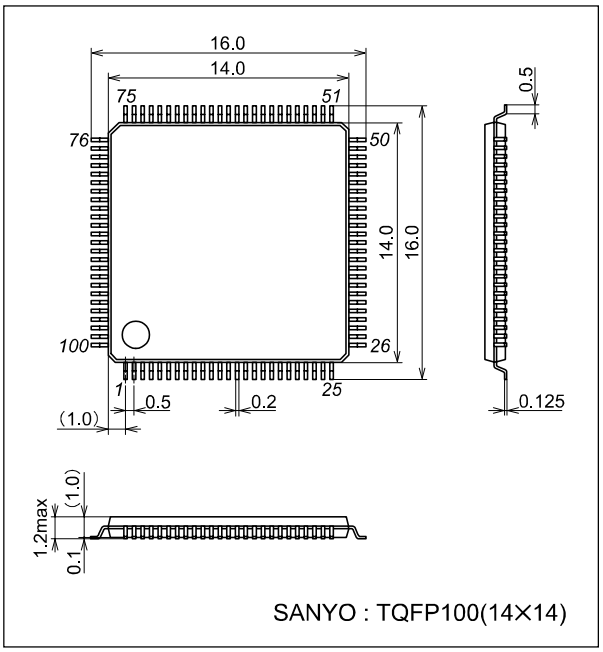
3151A



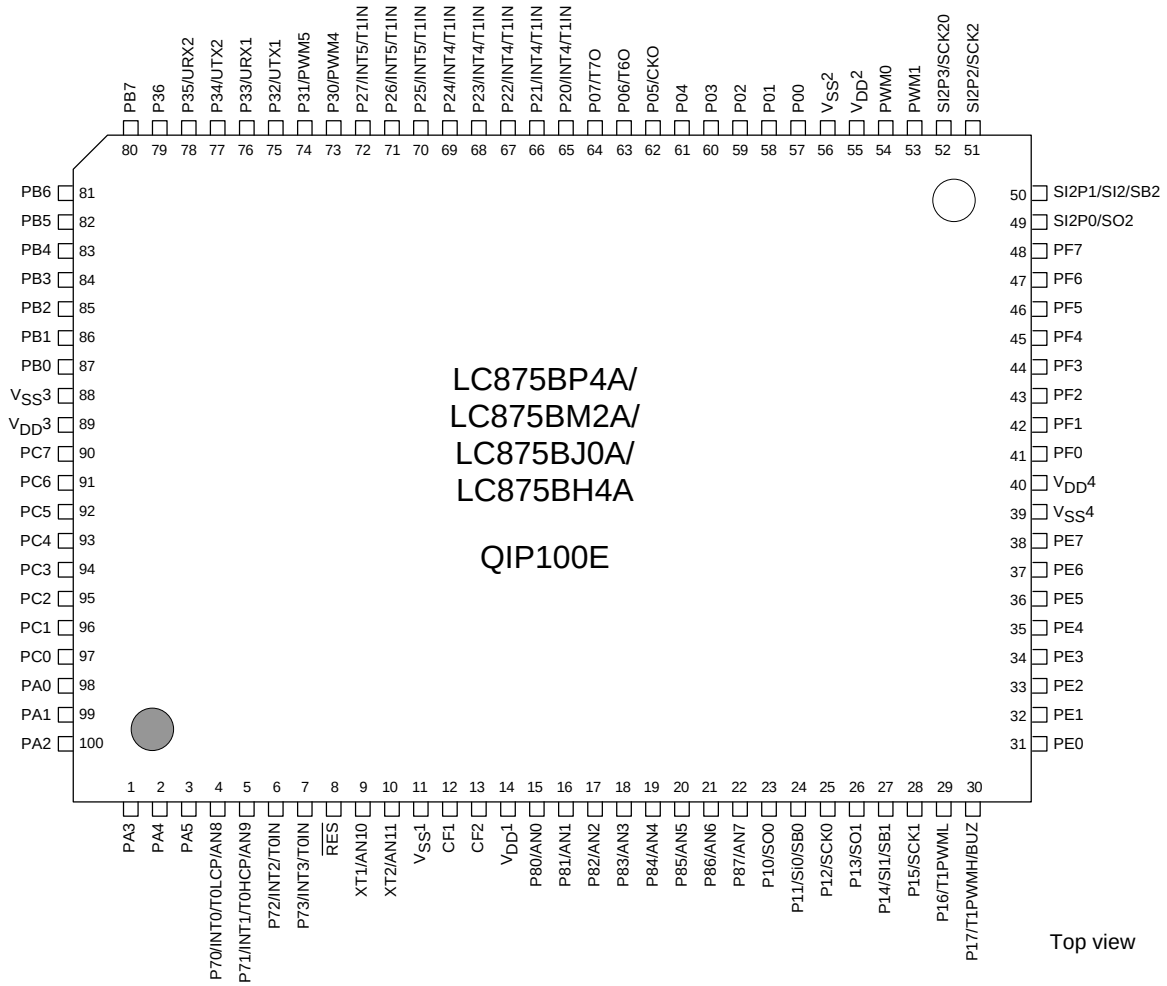
Package Dimensions

unit : mm

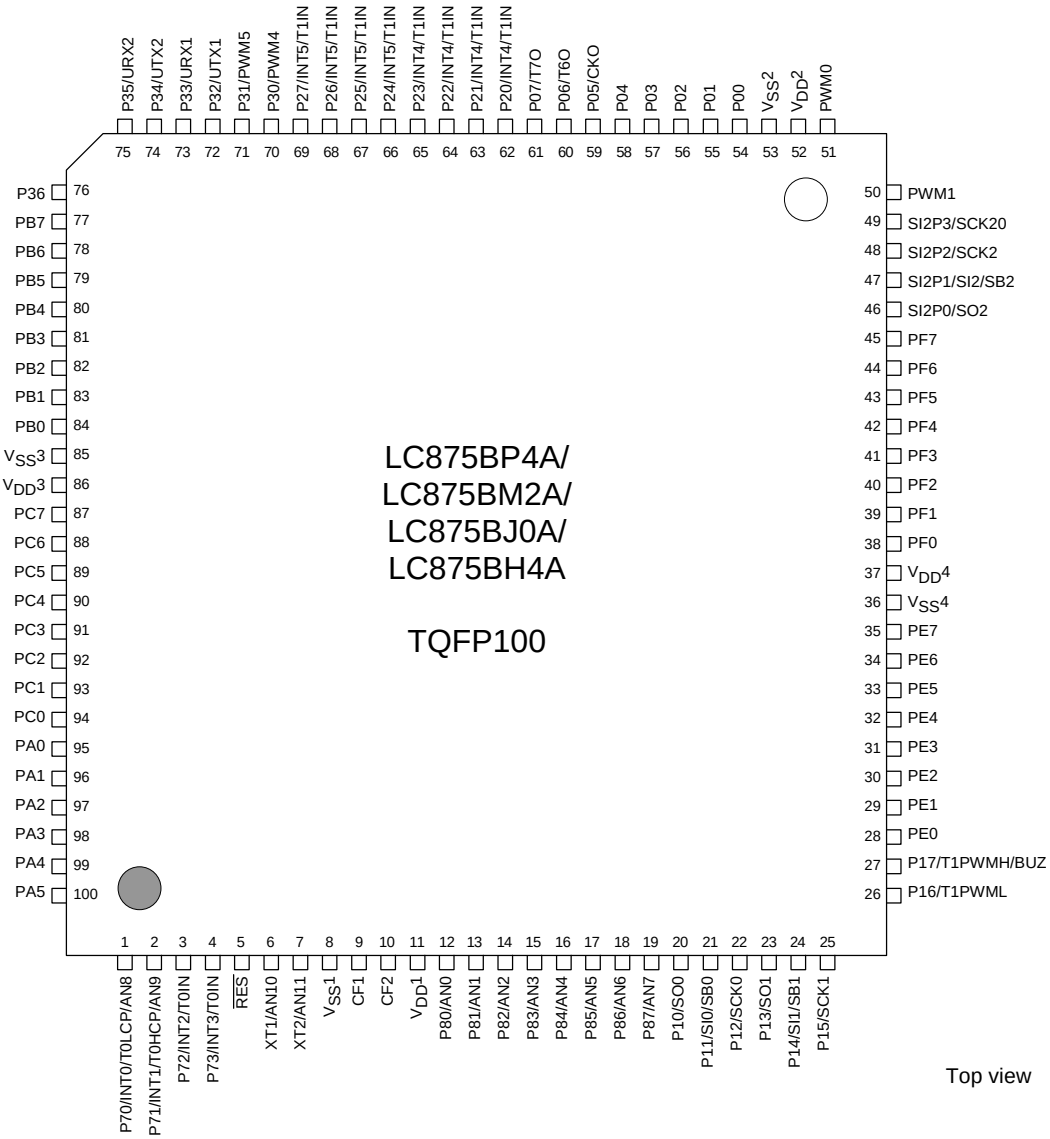
3274



Pin Assignment



Top view


LC875BP4A/
LC875BM2A/
LC875BJ0A/
LC875BH4A
TQFP100
1 P70/INT0/T0LCP/AN8
2 P71/INT1/T0HCP/AN9
3 P72/INT2/T0IN
4 P73/INT3/T0IN
5 RES
6 XT1/AN10
7 XT2/AN11
8 VSS1
9 CF1
10 CF2
11 VDD1
12 P80/AN0
13 P81/AN1
14 P82/AN2
15 P83/AN3
16 P84/AN4
17 P85/AN5
18 P86/AN6
19 P87/AN7
20 P10/SO0
21 P11/SI0/SB0
22 P12/SCK0
23 P13/SO1
24 P14/SI1/SB1
25 P15/SCK1
26 P16/T1PWML
27 P17/T1PWMH/BUZ
28 PE0
29 PE1
30 PE2
31 PE3
32 PE4
33 PE5
34 PE6
35 PE7
36 VSS4
37 VDD4
38 PF0
39 PF1
40 PF2
41 PF3
42 PF4
43 PF5
44 PF6
45 PF7
46 SI2P0/SO2
47 SI2P1/SI2/SB2
48 SI2P2/SCK2
49 SI2P3/SCK20
50 PWM1
51 PWM0
52 VDD2
53 VSS2
54 P00
55 P01
56 P02
57 P03
58 P04
59 P05/CKO
60 P06/T6O
61 P07/T7O
62 P20/INT4/T1IN
63 P21/INT4/T1IN
64 P22/INT4/T1IN
65 P23/INT4/T1IN
66 P24/INT5/T1IN
67 P25/INT5/T1IN
68 P26/INT5/T1IN
69 P27/INT5/T1IN
70 P30/PWM4
71 P31/PWM5
72 P32/UTX1
73 P33/URX1
74 P34/UTX2
75 P35/URX2
76 P36
77 PB7
78 PB6
79 PB5
80 PB4
81 PB3
82 PB2
83 PB1
84 PB0
85 VSS3
86 VDD3
87 PC7
88 PC6
89 PC5
90 PC4
91 PC3
92 PC2
93 PC1
94 PC0
95 PA0
96 PA1
97 PA2
98 PA3
99 PA4
100 PA5

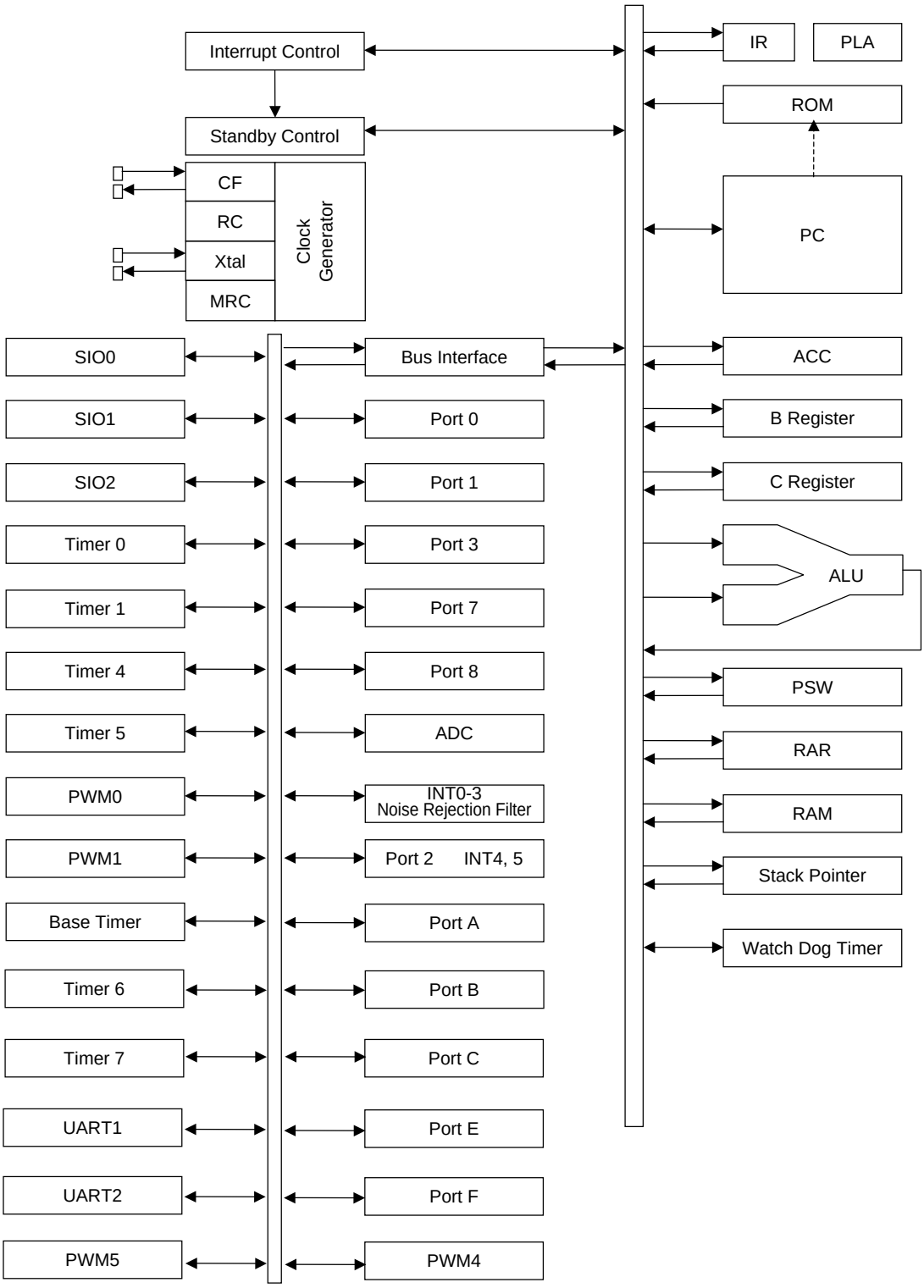
Top view

PAD Coordinate Values

QIP	NAME	TQFP
1	PA3	98
2	PA4	99
3	PA5	100
4	P70/INT0/T0LCP/AN8	1
5	P71/INT1/T0HCP/AN9	2
6	P72/INT2/T0IN	3
7	P73/INT3/T0IN	4
8	$\overline{RES}$	5
9	XT1/AN10	6
10	XT2/AN11	7
11	$V_{SS}1$	8
12	CF1	9
13	CF2	10
14	$V_{DD}1$	11
15	P80/AN0	12
16	P81/AN1	13
17	P82/AN2	14
18	P83/AN3	15
19	P84/AN4	16
20	P85/AN5	17
21	P86/AN6	18
22	P87/AN7	19
23	P10/SO0	20
24	P11/SI0/SB0	21
25	P12/SCK0	22
26	P13/SO1	23
27	P14/SI1/SB1	24
28	P15/SCK1	25
29	P16/T1PWML	26
30	P17/T1PWMH/BUZ	27
31	PE0	28
32	PE1	29
33	PE2	30
34	PE3	31
35	PE4	32
36	PE5	33
37	PE6	34
38	PE7	35
39	$V_{SS}4$	36
40	$V_{DD}4$	37
41	PF0	38
42	PF1	39
43	PF2	40
44	PF3	41
45	PF4	42
46	PF5	43
47	PF6	44
48	PF7	45
49	SI2P0/SO2	46
50	SI2P1/SI2/SB2	47

QIP	NAME	TQFP
51	SI2P2/SCK2	48
52	SI2P3/SCK20	49
53	PWM1	50
54	PWM0	51
55	$V_{DD}2$	52
56	$V_{SS}2$	53
57	P00	54
58	P01	55
59	P02	56
60	P03	57
61	P04	58
62	P05/CKO	59
63	P06/T6O	60
64	P07/T7O	61
65	P20/INT4/T1IN	62
66	P21/INT4/T1IN	63
67	P22/INT4/T1IN	64
68	P23/INT4/T1IN	65
69	P24/INT5/T1IN	66
70	P25/INT5/T1IN	67
71	P26/INT5/T1IN	68
72	P27/INT5/T1IN	69
73	P30/PWM4	70
74	P31/PWM5	71
75	P32/UTX1	72
76	P33/URX1	73
77	P34/UTX2	74
78	P35/URX2	75
79	P36	76
80	PB7	77
81	PB6	78
82	PB5	79
83	PB4	80
84	PB3	81
85	PB2	82
86	PB1	83
87	PB0	84
88	$V_{SS}3$	85
89	$V_{DD}3$	86
90	PC7	87
91	PC6	88
92	PC5	89
93	PC4	90
94	PC3	91
95	PC2	92
96	PC1	93
97	PC0	94
98	PA0	95
99	PA1	96
100	PA2	97

System Block Diagram



Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$, $V_{SS}2$
$V_{SS}3$, $V_{SS}4$</td><td>-</td><td>Power supply pin (-)</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$
$V_{DD}3$, $V_{DD}4$</td><td>-</td><td>Power supply pin (+)</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4-bit units
• Pull-up resistor can be turned on and off in 4-bit units
• HOLD release input
• Port 0 interrupt input
• Pin functions
P05 : System clock output
P06 : Timer 6 toggle output
P07 : Timer 7 toggle output</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
P10: SIO0 data output
P11 : SIO0 data input, bus I/O
P12 : SIO0 clock I/O
P13 : SIO1 data output
P14 : SIO1 data input, bus I/O
P15 : SIO1 clock I/O
P16 : Timer 1 PWML output
P17 : Timer 1 PWMH output/buzzer output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P27</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Other functions
P20 to P23 : INT4 input/HOLD release input/timer 1 event input/timer 0L capture input/timer 0H capture input
P24 to P27 : NT5 input/HOLD release input/timer 1 event input/timer 0L capture input/timer 0H capture input
• Interrupt detection style
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30 to P36</td><td>I/O</td><td>• 7-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
P30 : PWM4 output
P31 : PWM5 output
P32 : UART1 transmit
P33 : UART1 receive
P34 : UART2 transmit
P35 : UART2 receive</td><td>Yes</td></tr>
</table>

Continued on next page.

Continued from preceding page.

<table>
<tr><th>Name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Other functions
P70 : INT0 input/HOLD release input/timer 0L capture input/output for watchdog timer
P71 : INT1 input/HOLD release input/timer 0H capture input
P72 : INT2 input/HOLD release input/timer 0 event input/timer 0L capture input
P73 : INT3 input with noise filter/timer 0 event input/timer 0H capture input
• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table>
• AD converter input port : AN8 (P70), AN9 (P71)</td><td>No</td></tr>
<tr><td>Port 8
P80 to P87</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Other functions
P80 to P87 : AD converter input port</td><td>No</td></tr>
<tr><td>Port A
PA0 to PA5</td><td>I/O</td><td>• 6-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units</td><td>Yes</td></tr>
<tr><td>Port B
PB0 to PB7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units</td><td>Yes</td></tr>
<tr><td>Port C
PC0 to PC7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units</td><td>Yes</td></tr>
<tr><td>Port E
PE0 to PE7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 2-bit units
• Pull-up resistor can be turned on and off in 1-bit units</td><td>No</td></tr>
<tr><td>Port F
PF0 to PF7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 2-bit units
• Pull-up resistor can be turned on and off in 1-bit units</td><td>No</td></tr>
<tr><td>SIO2 Port
SI2P0 to SI2P3</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Other functions
SI2P0 : SIO2 data output
SI2P1 : SIO2 data input, bus input/output
SI2P2 : SIO2 clock input/output
SI2P3 : SIO2 clock output</td><td>No</td></tr>
<tr><td>PWM0</td><td>O</td><td>• PWM0 output port
• General-purpose I/O available</td><td>No</td></tr>
<tr><td>PWM1</td><td>O</td><td>• PWM1 output port
• General-purpose I/O available</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I</td><td>Reset pin</td><td>No</td></tr>
<tr><td>XT1</td><td>I</td><td>• Input terminal for 32.768kHz X'tal oscillation
• Other function
AN10 : AD converter input port
General input port
When not in use, connect terminal to $V_{DD}1$.</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• Output terminal for 32.768kHz X'tal oscillation
• Other function
AN11 : AD converter input port
General input port
When not in use, set as oscillation and leave terminal open</td><td>No</td></tr>
<tr><td>CF1</td><td>I</td><td>Input terminal for ceramic resonator</td><td>No</td></tr>
<tr><td>CF2</td><td>O</td><td>Output terminal for ceramic resonator</td><td>No</td></tr>
</table>

Port Output Configuration

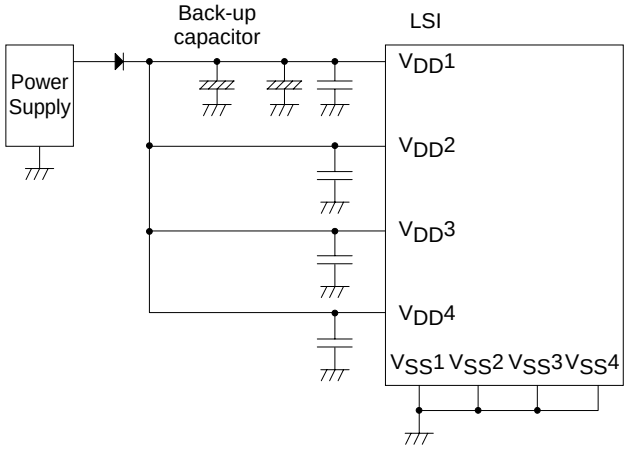
Output configuration and pull-up resistor options are shown in the following table.
Input is possible even when a port is in output mode.

Terminal	Option applies to :	Option	Output format	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	None
P10 to P17 P20 to P27 P30 to P36	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PA0 to PA5 PB0 to PB7 PC0 to PC7	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PE0 to PE7 PF0 to PF7	-	None	CMOS	Programmable
P70	-	None	Nch-open drain	Programmable
P71 to P73	-	None	CMOS	Programmable
P80 to P87	-	None	Nch-open drain	None
SI2P0, SI2P2 SI2P3 PWM0, PWM1	-	None	CMOS	None
SI2P1	-	None	CMOS (when used as general port) Nch-open drain (when used for SIO2 data)	None
XT1	-	None	Input only	None
XT2	-	None	Output for 32.768kHz crystal oscillation Nch-open drain (when in general-purpose output mode)	None

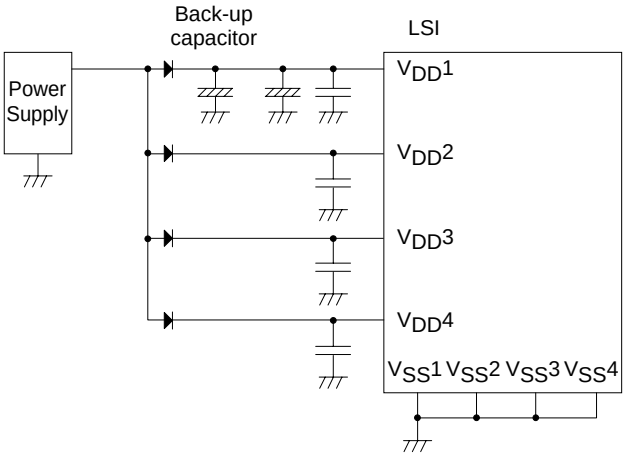
Note 1 Programmable pull-up resistor of Port 0 is specified in nibble units (P00 to P03, P04 to P07).

Note : To reduce V_{DD} signal noise and to increase the duration of the backup battery supply, $V_{SS}1$, $V_{SS}2$, $V_{SS}3$ and $V_{SS}4$ should connect to each other and they should also be grounded.

Example 1 : During backup in hold mode, port output 'H' level is supplied from the back-up capacitor.



Example 2 : During backup in hold mode, output is not held high and its value in unsettled.



Absolute Maximum Ratings / Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter		Symbol	Pins	Conditions		Limits			
					V_{DD}[V]	min	typ	max	unit
Supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$, $V_{DD}4$	$V_{DD}1=V_{DD}2=V_{DD}3=V_{DD}4$		-0.3		+6.5	V
Input voltage		V_I (1)	XT1, XT2, CF1			-0.3		V_{DD}+0.3	
Output voltage		V_O (1)	PWM0, PWM1			-0.3		V_{DD}+0.3	
Input/output voltage		VIO (1)	• Ports 0, 1, 2 • Ports 3, 7, 8 • Ports A, B, C, E, F • SI2P00 to SI2P03 • PWM0, PWM1			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH (1)	• Ports 0, 1, 2, 3 • Ports A, B, C, E, F • SI2P00 to SI2P03 • PWM0, PWM1	• CMOS output • For each pin.		-10			mA
		IOPH (2)	P71 to P73	For each pin.		-5			
	Total output current	ΣIOAH (1)	P71 to P73	Total of all pins		-5			
		ΣIOAH (2)	• Port 1 • PWM0, PWM1 • Port 3 • SI2P00 to SI2P03	Total of all pins		-30			
		ΣIOAH (3)	Ports 0, 2	Total of all pins		-20			
		ΣIOAH (4)	Port B	Total of all pins		-20			
		ΣIOAH (5)	Ports A, C	Total of all pins		-20			
Low level output current	Peak output current	IOPL (1)	• P02 to P07 • Ports 1, 2, 3 • Ports A, B, C, E, F • SI2P00 to SI2P03 • PWM0, PWM1	For each pin.				20	
		IOPL (2)	P00, P01	For each pin.				30	
		IOPL (3)	Ports 7, 8	For each pin.				5	
	Total output current	ΣIOAL (1)	Port 7	Total of all pins				15	
		ΣIOAL (2)	Port 8	Total of all pins				15	
		ΣIOAL (3)	• PWM0, PWM1 • Port 3 • SI2P00 to SI2P03	Total of all pins				40	
		ΣIOAL (4)	Ports 0, 2, 3	Total of all pins				80	
		ΣIOAL (5)	Port B	Total of all pins				40	
		ΣIOAL (6)	Ports A, C	Total of all pins				40	
		ΣIOAL (7)	Port F	Total of all pins				40	
		ΣIOAL (8)	Port 1, E	Total of all pins				70	
Maximum power consumption		Pd max	QIP100E	Ta= -30 to +70°C				519	mW
			TQFP100					363	
Operating temperature range		Topr				-30		70	°C
Storage temperature range		Tstg				-55		125	

Recommended Operating Range / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Pins	Conditions		Limits			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage range	V_{DD} (1)	$V_{DD}1=V_{DD}2=V_{DD}3=V_{DD}4$	0.294µs ≤ tCYC ≤ 200µs		4.5		5.5	V
			0.588µs ≤ tCYC ≤ 200µs		2.5		5.5	
HOLD voltage	VHD	$V_{DD}1=V_{DD}2=V_{DD}3=V_{DD}4$	RAM and register data are kept in HOLD mode.		2.0		5.5	
Input high voltage	V_{IH} (1)	• Ports 1, 2, 3 • SI2P00 to 03 • P71 to P73 • P70 port input /interrupt		2.5 to 5.5	$0.3V_{DD}+0.7$		V_{DD}	
	V_{IH} (2)	• Ports 0, 8 • Ports A, B, C, E, F		2.5 to 5.5	$0.3V_{DD}+0.7$		V_{DD}	
	V_{IH} (3)	Port 70 watchdog timer		2.5 to 5.5	$0.9V_{DD}$		V_{DD}	
	V_{IH} (4)	XT1, XT2, CF1, $\overline{RES}$		2.5 to 5.5	$0.75V_{DD}$		V_{DD}	
Input low voltage	V_{IL} (1)	• Ports 1, 2, 3 • SI2P00 to 03 • P71 to P73 • P70 port input /interrupt		2.5 to 5.5	V_{SS}		$0.1V_{DD}+0.4$	
	V_{IL} (2)	• Ports 0, 8 • Ports A, B, C, E, F		2.5 to 5.5	V_{SS}		$0.15V_{DD}+0.4$	
	V_{IL} (5)	Port 70 Watchdog timer		2.5 to 5.5	V_{SS}		$0.8V_{DD}-1.0$	
	V_{IL} (6)	XT1, XT2, CF1, $\overline{RES}$		2.5 to 5.5	V_{SS}		$0.25V_{DD}$	
Operation cycle time	tCYC			4.5 to 5.5	0.294		200	µs
				2.5 to 5.5	0.588		200	
External system clock frequency	FEXCF (1)	CF1	• Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY=50±5%	4.5 to 5.5	0.1		10	MHz
			• Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY=50±5%	2.5 to 5.5	0.1		5	
			• Leave CF2 pin open • System clock divider set to 1/2	4.5 to 5.5	0.2		20.4	
			• Leave CF2 pin open • System clock divider set to 1/2	2.5 to 5.5	0.1		10	
Oscillation frequency Range (Note1)	FmCF (1)	CF1, CF2	10MHz ceramic resonator oscillation Refer to figure 1	4.5 to 5.5		10		
	FmCF (2)	CF1, CF2	5MHz ceramic resonator oscillation Refer to figure 1	2.5 to 5.5		5		
	FmRC		RC oscillation	2.5 to 5.5	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation source oscillation	2.5 to 5.5		50		
	FsX'tal	XT1, XT2	32.768kHz crystal resonator oscillation Refer to figure 2	2.5 to 5.5		32.768		kHz

Note 1 : The oscillation parameters are shown on Tables 1 and 2.

Electrical Characteristics / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Pins	Conditions		Limits			
				V_{DD}[V]	min	typ	max	unit
Input high current	I_{IH} (1)	• Ports 0, 1, 2 • Ports 3, 7, 8 • Ports A, B, C • SI2P00 to SI2P03 • $\overline{RES}$ • PWM0, PWM1	• Output disable • Pull-up resistor OFF • $V_{IN}=V_{DD}$ (including the off-leak current of the output Tr.)	2.5 to 5.5			1	µA
	I_{IH} (2)	XT1, XT2	• Using as an input port • $V_{IN}=V_{DD}$	2.5 to 5.5			1	
	I_{IH} (3)	CF1	$V_{IN}=V_{DD}$	2.5 to 5.5			15	
Input low current	I_{IL} (1)	• Ports 0, 1, 2 • Ports 3, 7, 8 • Ports A, B, C, E, F • SI2P00 to SI2P03 • $\overline{RES}$ • PWM0, PWM1	• Output disable • Pull-up resistor OFF • $V_{IN}=V_{SS}$ (including the off-leak current of the output Tr.)	2.5 to 5.5	-1			
	I_{IL} (2)	XT1, XT2	• Using as an input port • $V_{IN}=V_{SS}$	2.5 to 5.5	-1			
	I_{IL} (3)	CF1	$V_{IN}=V_{SS}$	2.5 to 5.5	-15			
Output high voltage	V_{OH} (1)	• Ports 0, 1, 2, 3 • Ports A, B, C, E, F • SI2P00 to SI2P03	I_{OH}= -1.0mA	4.5 to 5.5	V_{DD}-1			V
	V_{OH} (2)		I_{OH}= -0.1mA	2.5 to 5.5	V_{DD}-0.5			
	V_{OH} (3)	Port 71, 72, 73	I_{OH}= -1.5mA	4.5 to 5.5	V_{DD}-1			
	V_{OH} (4)	PWM0, PWM1 P30, P31 (PWM4, 5 output mode)	I_{OH}= -6.0mA	4.5 to 5.5	V_{DD}-1			
	V_{OH} (5)		I_{OH}= -1.6mA	4.5 to 5.5	V_{DD}-0.4			
	V_{OH} (6)		I_{OH}= -1.0mA	2.5 to 5.5	V_{DD}-0.4			
Output low voltage	V_{OL} (1)	• Ports 0, 1, 2, 3 • Ports A, B, C, E, F • SI2P00 to SI2P03 • PWM0, PWM1	I_{OL}=10mA	4.5 to 5.5			1.5	
	V_{OL} (2)		I_{OL}=1.6mA	4.5 to 5.5			0.4	
	V_{OL} (3)		I_{OL}=1.0mA	2.5 to 5.5			0.4	
	V_{OL} (4)	P00, P01	I_{OL}=30mA	4.5 to 5.5			1.5	
	V_{OL} (5)	Ports 7, 8	I_{OL}=1.0mA	2.5 to 5.5			0.4	
Pull-up resistor	Rpu	• Ports 0, 1, 2, 3 • Port 7 • Ports A, B, C, E, F	$V_{OH}=0.9V_{DD}$	2.5 to 5.5	15	40	70	kΩ
Hysteresis voltage	VHIS	• $\overline{RES}$ • Port 1 • Port 2 • Port 3 • Port 7 • SIP00 to SIP03		2.5 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	• All pins except the measured terminal : $V_{IN}=V_{SS}$ • f=1MHz • Ta=25°C	2.5 to 5.5		10		pF

Serial Input/Output Characteristics / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter			Symbol	Pins	Conditions	V_{DD} [V]	Limits min	typ	max	unit
Serial clock	Input clock	Cycle	tSCK (1)	SCK0 (P12), SI2P2	Refer to figure 6	2.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL (1)				1			
			tSCKLA (1)				1			
		High level pulse width	tSCKH (1)				1			
			tSCKHA (1)				4(SIO0) 5(SIO2)			
		Cycle	tSCK (2)	SCK1 (P15)	Refer to figure 6	2.5 to 5.5	2			
		Low level pulse width	tSCKL (2)				1			
		High level pulse width	tSCKH (2)				1			
	Output clock	Cycle	tSCK (3)	SCK0 (P12), SI2P2 SI2P3	• CMOS output • Refer to figure 6	2.5 to 5.5	4/3			
		Low level pulse width	tSCKL (3)					1/2		tSCK
			tSCKLA (2)		SCK0 (P12) SIO0			3/4		
					SI2P2, SI2P3 SIO2			1		
		High level pulse width	tSCKH (3)					1/2		
			tSCKHA (2)		SCK0 (P12) SIO0			2		
					SI2P2, SI2P3 SIO2			7/4		
		Cycle	tSCK (4)	SCK1 (P15)	• CMOS output • Refer to figure 6	2.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL (4)					1/2		tSCK
		High level pulse width	tSCKH (4)					1/2		
Serial input	Data set-up time		tsDI	SB0 (P11), SB1 (P14), SI2P1 SI0 SI1	• Data set-up to SI0CLK • Data hold from SI0CLK • Refer to figure 6	2.5 to 5.5	0.03			µs
	Data hold time		thDI				0.03			
Serial output	Output delay time		tdD0	SO0 (P10), SO1 (P13), SB0 (O11), SB1 (P14), SI2P0, SI2P1	• Data hold from SI0CLK • Time delay from SI0CLK trailing edge to the SO data change in the open drain • Refer to figure 6	2.5 to 5.5			1/3tCYC +0.05	

Pulse Input Conditions / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Limits min	typ	max	unit
High/low level pulse width	tPIH (1) tPIL (1)	INT0 (P70), INT1 (P71), INT2 (P72) INT4 (P20 to P23) INT5 (P24 to P27)	• Interrupt acceptable • Timer 0 and 1 event input acceptable	2.5 to 5.5	1			tCYC
	tPIH (2) tPIL (2)	INT3 (P73) (The noise rejection clock is selected to 1/1.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 to 5.5	2			
	tPIH (3) tPIL (3)	INT3 (P73) (The noise rejection clock is selected to 1/32.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 to 5.5	64			
	tPIH (4) tPIL (4)	INT3 (P73) (The noise rejection clock is selected to 1/128.)	• Interrupt acceptable • Timer 0 event input acceptable	2.5 to 5.5	256			
	tPIL (5)	$\overline{RES}$	Reset acceptable	2.5 to 5.5	200			µs

AD Converter Characteristics / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Limits min	typ	max	unit
Resolution	N	AN0 (P80) to AN7 (P87) AN8 (P70) AN9 (P71) AN10 (XT1) AN11 (XT2)		3.0 to 5.5		8		bit
Absolute precision	ET		(Note 2)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time=32 × tCYC (ADCR2=0) (Note 3)	4.5 to 5.5	15.10 (tCYC= 0.588µs)		97.92 (tCYC= 3.06µs)	µs
				3.0 to 5.5	31.36 (tCYC= 0.980µs)		97.92 (tCYC= 3.06µs)	
			AD conversion time=64 × tCYC (ADCR2=1) (Note 3)	4.5 to 5.5	18.82 (tCYC= 0.294µs)		97.92 (tCYC= 1.53µs)	
				3.0 to 5.5	62.72 (tCYC= 0.980µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Note 2 : Absolute precision excludes the quantizing error (±1/2 LSB).

Note 3 : The conversion time is the time from executing the AD conversion instruction to setting the complete digital conversion value in the register.

Current Dissipation Characteristics / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Limits min	typ	max	unit
Current drain during basic operation (Note 4)	IDDOP (1)	$V_{DD}1$ $=V_{DD}2$ $=V_{DD}3$ $=V_{DD}4$	• FmCF=10MHz by ceramic resonator • FmX'tal=32.768kHz by crystal oscillation • System clock : CF oscillation (10MHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/1 divided	4.5 to 5.5		10	15	mA
	IDDOP (2)		• CF1=20MHz by external clock • FmX'tal=32.768kHz by crystal oscillation • System clock : CF1 oscillation (20MHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/2 divided	2.5 to 5.5		10.5	16	
	IDDOP (3)		• FmCF=5MHz by ceramic resonator • FmX'tal=32.768kHz by crystal oscillation • System clock : CF oscillation (5MHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/1 divided	4.5 to 5.5		5.5	8	
	IDDOP (4)			2.5 to 4.5		3	6	
	IDDOP (5)		• FmCF=0Hz (when oscillation stops) • FmX'tal=32.768kHz by crystal oscillation • System clock : RC oscillation • Frequency variable RC oscillation stops • 1/2 divided	4.5 to 5.5		0.7	4	
	IDDOP (6)			2.5 to 4.5		0.3	1.5	
	IDDOP (7)		• FmCF=0Hz (when oscillation stops) • FmX'al=32.768kHz by crystal oscillation • System clock : 1MHz with frequency variable RC oscilatin • Internal RC oscillation stops • 1/2 divided	4.5 to 5.5		2	6	
	IDDOP (8)			2.5 to 5.5		0.7	3.5	
	IDDOP (9)		• FmCF=0Hz (when oscillation stops) • FmX'al=32.768kHz by crystal oscillation • System clock : X'tal oscillation (32.768kHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/2 divided	4.5 to 5.5		27	60	µA
	IDDOP (10)			2.5 to 4.5		12	40	

Note 4 : The current of the output transistors and pull-up MOS transistors are excluded.

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Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Limits min	typ	max	unit
Current drain in HALT mode (Note 4)	IDDHALT (1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ =$V_{DD}4$	• HALT mode • FmCF=10MHz by ceramic resonator • FmX'tal=32.768kHz by crystal oscillation • System clock : CF oscillation (10MHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/1 divided	4.5 to 5.5		2.5	5	mA
	IDDHALT (2)		• HALT mode • CF1=20MHz by external clock • FmX'tal=32.768kHz by crystal oscillation • System clock : CF1 oscillation (20MHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/2 divided	4.5 to 5.5		3.2	6	
	IDDHALT (3)		• HALT mode • FmCF=5MHz by ceramic resonator • FmX'tal=32.768kHz by crystal oscillation • System clock : CF oscillation (5MHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/1 divided	4.5 to 6.0		1.5	3	
	IDDHALT (4)			2.5 to 4.5		0.7	1.5	
	IDDHALT (5)		• HALT mode • FmCF=0Hz (when oscillation stops) • FmX'tal=32.768kHz by crystal oscillation • System clock : RC oscillation • Frequency variable RC oscillation stops • 1/2 divided	4.5 to 5.5		0.3	1	
	IDDHALT (6)			2.5 to 4.5		0.15	0.5	
	IDDHALT (7)		• HALT mode • FmCF=0Hz (when oscillation stops) • FmX'tal=32.768kHz by crystal oscillation • System clock : 1MHz with frequency variable RC oscilatin • Internal RC oscillation stops • 1/2 divided	4.5 to 5.5		1.6	2.5	
	IDDHALT (8)			2.5 to 4.5		0.6	1.8	
	IDDHALT (9)		• HALT mode • FmCF=0Hz (when oscillation stops) • FmX'tal=32.768kHz by crystal oscillation • System clock : X'tal oscillation (32.768kHz) • Internal RC oscillation stops • Frequency variable RC oscillation stops • 1/2 divided	4.5 to 5.5		16	40	µA
	IDDHALT (10)			2.5 to 4.5		5	25	
Current drain during HOLD mode	IDDHOLD (1)	$V_{DD}1$	• HOLD mode • CF1=V_{DD} or leave it open (when using external clock)	4.5 to 5.5		0.015	10	
	IDDHOLD (2)			2.5 to 4.5		0.001	5	
Current drain during time-base clock HOLD mode	IDDHOLD (3)	$V_{DD}1$	• Time-base clock HOLD mode • CF1=V_{DD} or leave it open (when using external clock) • FmX'tal=32.768kHz by crystal oscillation	4.5 to 5.5		14	35	
	IDDHOLD (4)			2.5 to 4.5		3.8	20	

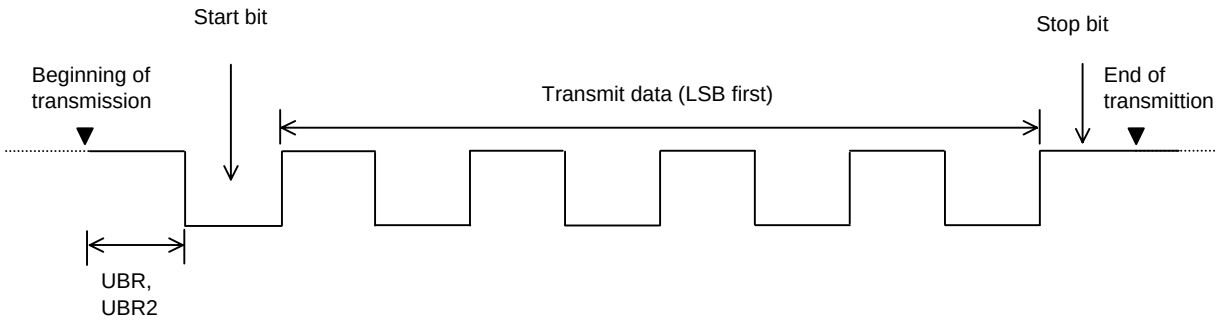
Note 4 : The current of the output transistors and pull-up MOS transistors are excluded.

UART (full duplex) Operating Conditions / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

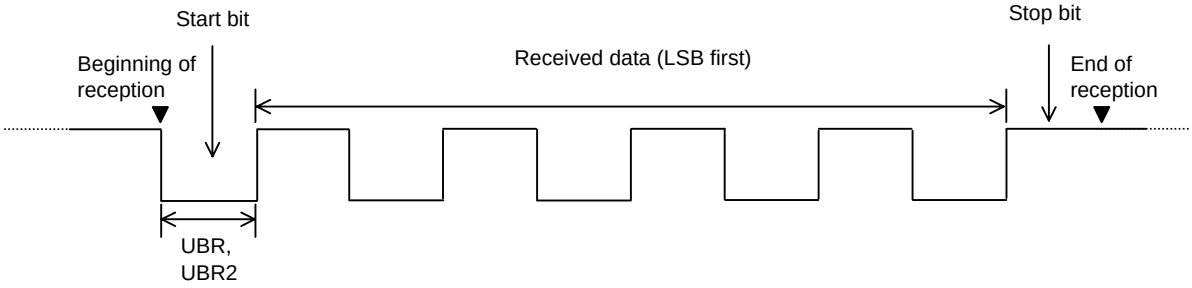
Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD} [V]	min	typ	max	unit
Clock rate	UBR, UBR2	UTX1 (P32), RTX1 (P33), UTX2 (P33), RTX2 (P34)		2.5 to 5.5	16/3		8192/3	tCYC

Data length : 7, 8 and 9 bits (LSB first)
Stop bits : 1-bit
Parity bits : Non

Continuous 8-bit data transmit mode (first transmit data = 55H)



Continuous 8-bit data receive mode (first transmit data = 55H)



Main System Clock Oscillation Circuit Characteristics

The characteristics in the table bellow is based on the following conditions :
1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacturer.

Table 1. Recommended circuit parameters for the main system clock using the ceramic resonator

Frequency	Manufacturer	Oscillator	Recommended circuit parameters			Operating supply voltage range	Oscillation stabilizing time		Note
			C1	C2	Rd1		typ	max	
10MHz	MURATA	CSLS10M0G53-R0	(10pF)	(10pF)	150Ω	4.5 to 5.5V			Internal C1,C2
		CSTLS10M0G52-B0	(10pF)	(10pF)	100Ω	4.5 to 5.5V			Internal C1,C2
5MHz	MURATA	CSTLS5M00G53-R0	(15pF)	(15pF)	470Ω	2.5 to 5.5V			Internal C1,C2
		CSTLS5M00G53-B0	(15pF)	(15pF)	470Ω	2.5 to 5.5V			Internal C1,C2

*The oscillation stabilizing time is a period until the oscillation becomes stable after V_{DD} becomes higher than minimum operating voltage. (Refer to Figure 4)

Subsystem Clock Oscillation Circuit Characteristics

The characteristics in the table bellow is based on the following conditions :
1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacturer.

Table 2. Recommended circuit parameters for the subsystem clock using the crystal oscillation

Frequency	Manufacturer	Oscillator	Recommended circuit Parameters				Operating supply voltage range	Oscillation stabilizing time		Note
			C3	C4	Rf	Rd2		typ	max	
32.768kHz	SEIKO EPSON	MC-306	15pF	15pF	OPEN	390kΩ	2.5 to 5.5V			

*The oscillation stabilizing time is the period until the oscillation becomes stable, after executing the instruction which starts the sub-clock oscillator or after releasing a HOLD mode. (Refer to Figure 4)

Notes : Since the oscillation frequency precision is affected by the circuit pattern, place the oscillation related parts as close to the oscillation pins as possible, using the shortest possible pattern length.

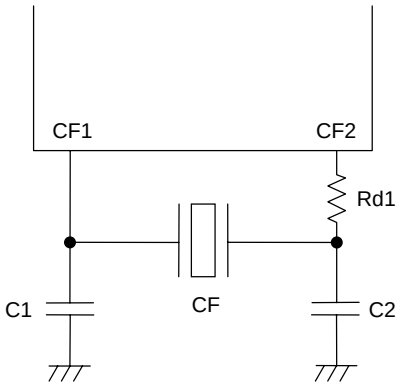


Figure 1 Ceramic oscillation circuit

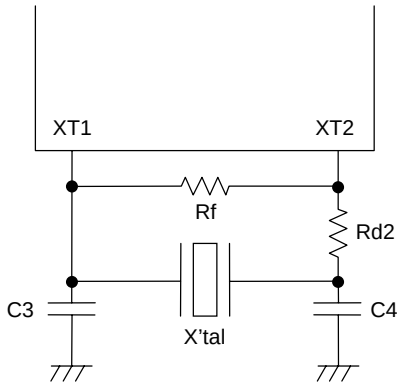


Figure 2 Crystal oscillation circuit

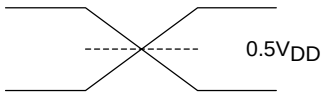
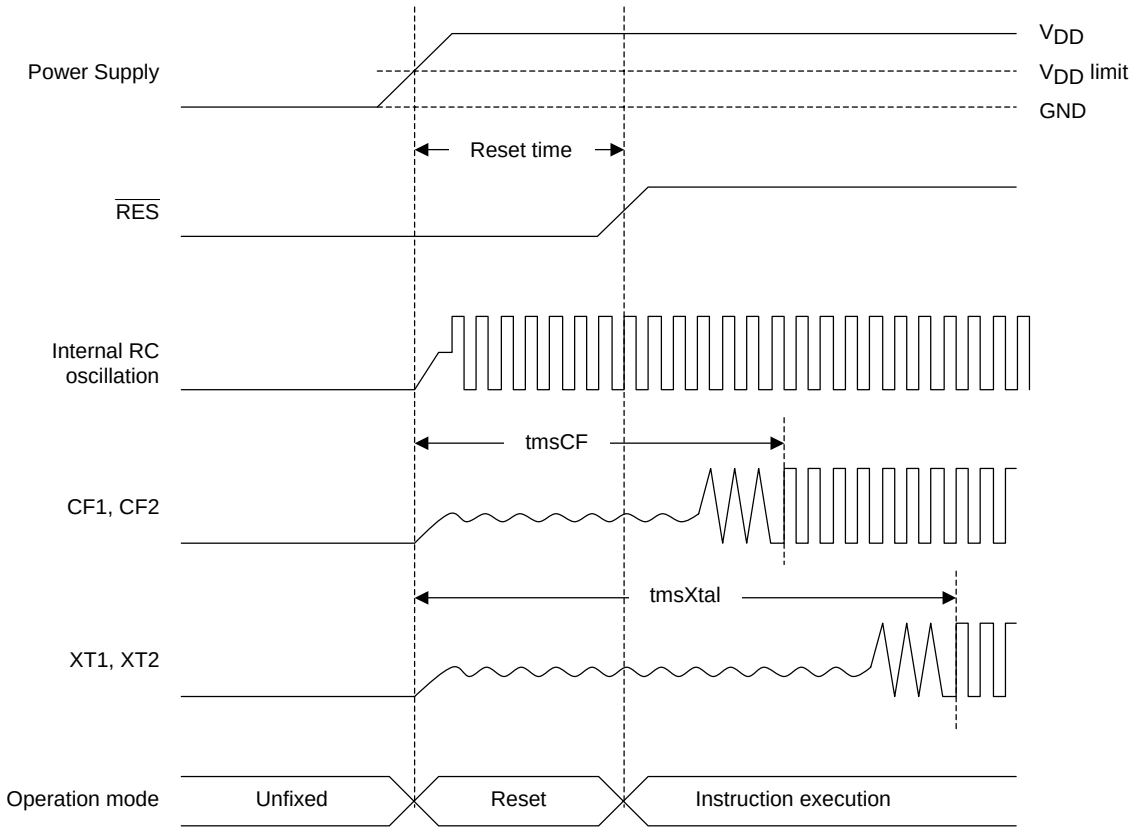
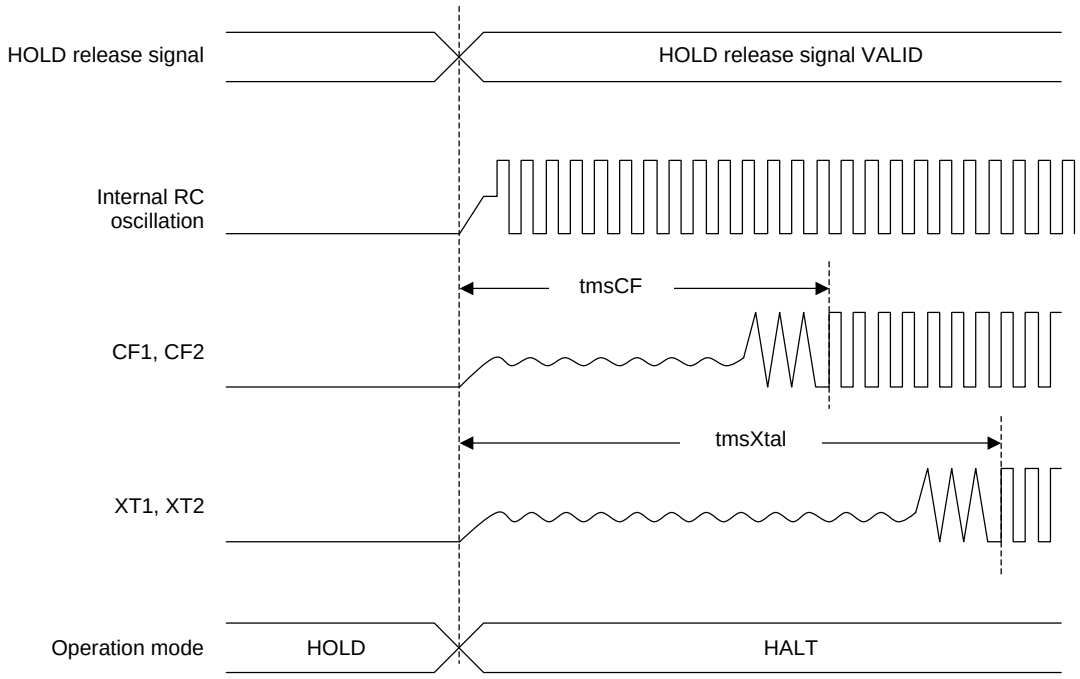


Figure 3 AC timing point

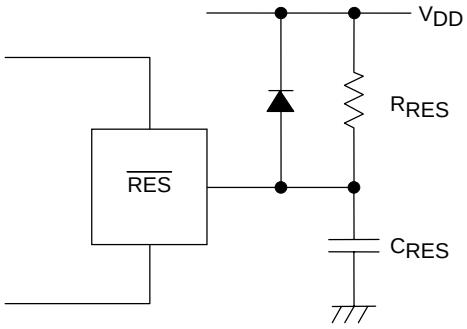


Reset time and oscillation stabilizing time



HOLD release signal and oscillation stabilizing time

Figure 4 Oscillation stabilizing time



(Note)
Select C_{RES} and R_{RES} value to assure that at least 200μs reset time is generated after the V_{DD} becomes higher than the minimum operating voltage.

Figure 5 Reset circuit

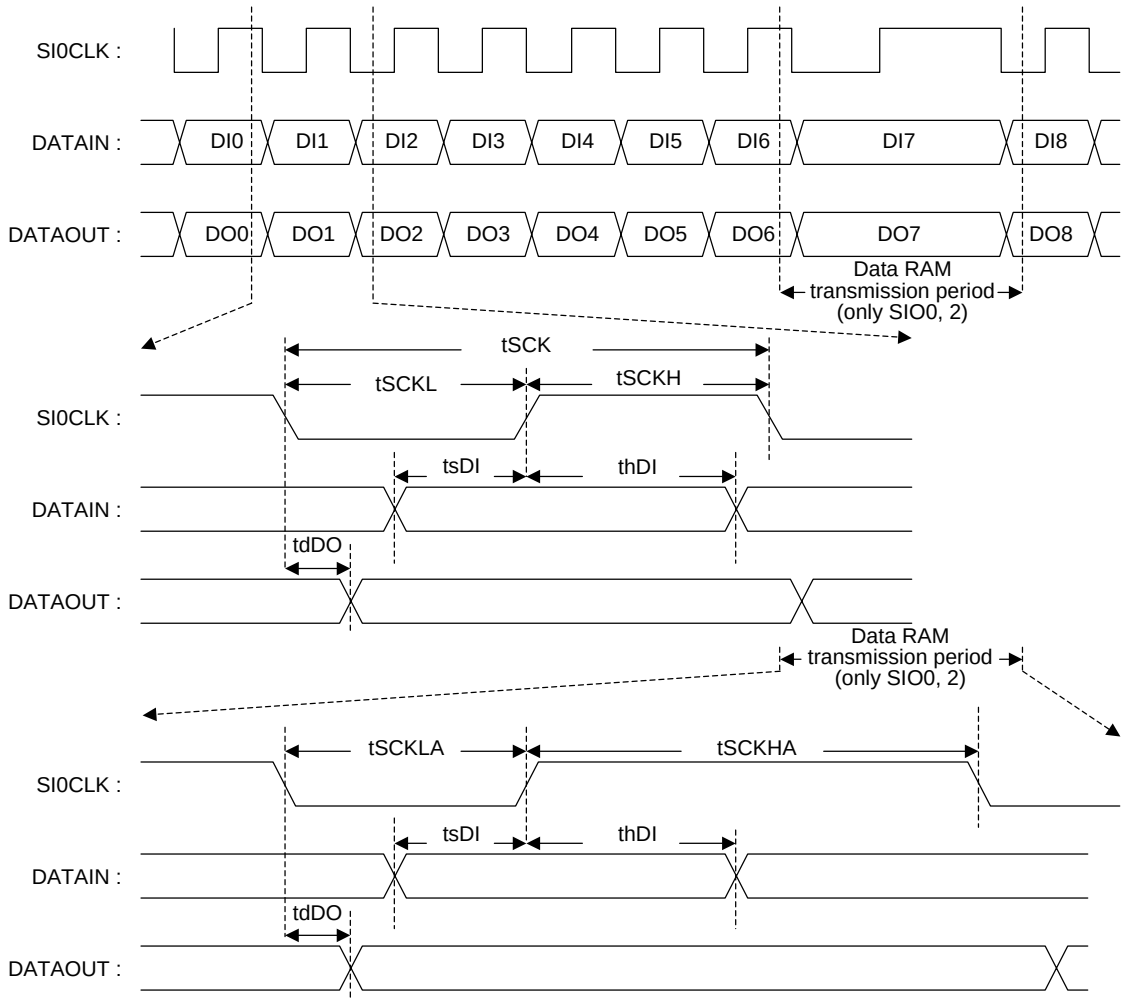


Figure 6 Serial input/output test condition

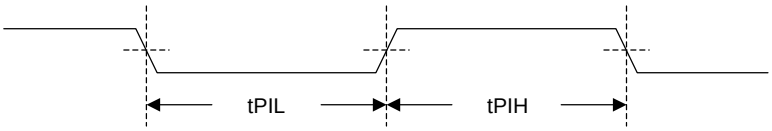


Figure 7 Pulse input timing condition