Ordering number : ENA1977

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

Bi-CMOS IC

LV5858M — Step-down Switching Regulator

Overview

LV5858M is a 3A and 1ch step-down switching regulator. 0.1Ω FET is incorporated on the upper side to achieve high-efficiency operation for large output current. Current mode control type, with superior load current response and easy phase compensation ON/OFF pin, allowing the standby mode with the current drain of 60μA or less Pulse-by-pulse over-current protection and overheat protection available for protection of load devices Soft start pin to be provided with a capacitance for soft start.

Functions

- Wide input dynamic range (8 to 42V)
- High efficiency (V_{IN} = 24V, V_O = 5V, I_{OUT} = 3A, 88%)
- Current mode control type
- Standby mode: 60μA
- Built-in pulse-by-pulse OCP circuit. It is detected by using ON resistance of an external MOS.
- Thermal shutdown
- Reference voltage: 0.708V
- Fixed frequency: 385kHz
- Load-independent soft start circuit

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter		Symbol	Conditions	Ratings	Unit
Supply voltage		V_{IN} max		45	V
Allowable pin voltage	V_{IN}, SW			45	V
	CBOOT			52	V
	Between CBOOT and SW			6.0	V
	EN			V_{IN} max	V
	V_{DD}			6.0	V
	SS, FB, COMP, RT			V_{DD}	V
Allowable power dissipation		Pd max	Ta≤85°C Mounted on a specified board *	0.95	W
Operating temperature		Topr		-40 to 85	°C
Storage temperature		Tstg		-55 to 150	°C
Junction temperature		Tj max		150	°C

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* Specified board: 36.0mm × 44.0mm ×1.6mm, glass epoxy, 2 layer substrate.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{IN}		8 to 42	V
Error amplifier input voltage	V_{FB}		0 to 1.6	V

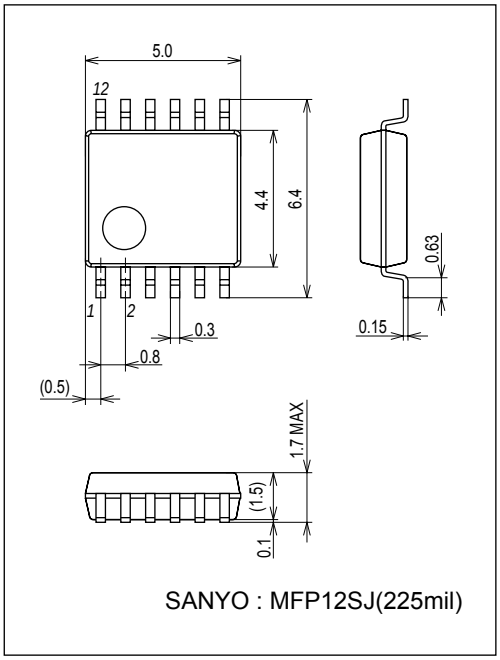
Electrical Characteristics at Ta = 25°C, V_{IN} = 24V

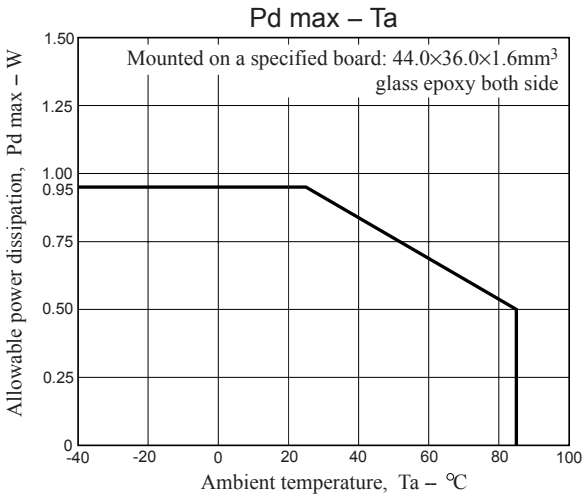
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reference voltage block						
Internal reference voltage	VREF	Including offset of E/A	0.698	0.708	0.718	V
5V power supply	V_{DD}	I_{OUT}=0 to 5mA	4.7	5.2	5.7	V
Triangular waveform oscillator block						
Oscillation frequency	f_{OSC}		335	385	435	kHz
Frequency variation	f_{OSC} DV	V_{IN}=8.0 to 42V		1		%
Oscillation frequency fold back detection voltage	V_{OSC} FB	FB voltage detection after SS ends		0.5		V
Oscillatory frequency after fold back	f_{OSC} FB		25	45	60	kHz
ON/OFF circuit block						
IC start-up voltage	V_{EN}_on	V_{IN}=8.0 to 42V		3.4	4.3	V
IC off voltage	V_{EN}_off		1.1	1.3		V
Soft start circuit block						
Soft start source current	I_{SS}_SC	EN › 3.5V	4	5	6	μA
Soft start sink current	I_{SS}_SK	EN ‹ 1V, V_{DD}=5V		2		mA
Voltage to end the soft start function	V_{SS}_END		0.9	1.1	1.3	V
UVLO circuit block						
UVLO lock release voltage	V_{UVLO}		7.0	7.4	7.8	V
UVLO hysteresis	V_{UVLO}_H			0.6		V
Error amplifier						
Input bias current	I_{EA}_IN				100	nA
Error amplifier transconductance	G_{EA}		1000	1400	1800	μA/V
Common mode input voltage range	V_{EA}_R		0.0		1.6	V
Sink output current	I_{EA}_OSK	FB=1.0V		-100		μA
Source output current	I_{EA}_OSC	FB=0V		100		μA
Current detection amplifier gain	GISNS			1.3		
Over current limiter circuit block						
Current limit pead value	I_{LIM}_OFS	VOUT=5V, L=-10μH	4.0	4.5		A
PWM comparator						
Input threshold voltage f_{OSC}=125kHz)	Vt max	Duty cycle=D max	1.0	1.1	1.2	V
	Vt0	Duty cycle=0%	0.4	0.5	0.6	V
Maximum ON duty	D max		85	90	95	%
Output block						
Output stage ON resistance (the upper side)	R_{ON}			0.1		Ω
The whole device						
Standby current	I_{CC}S	EN ‹ 1V			60	μA
Mean consumption current	I_{CC}A	EN ‹ 4.3V		3.3		mA
Protection function						
Temperature at which the high-temperature protection function operates	TSD_on	*Design guarantee		170		°C
High-temperature protection function hysteresis	TSD_hys	*Design guarantee		30		°C

Package Dimensions

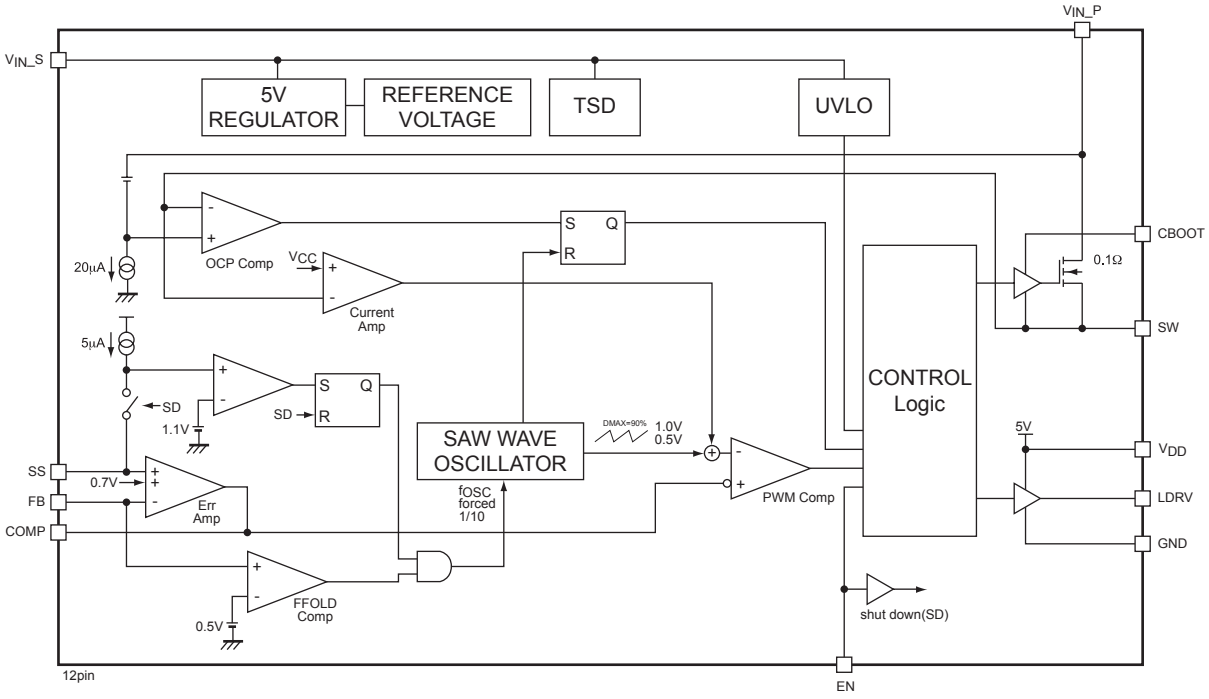
unit : mm (typ)

3403

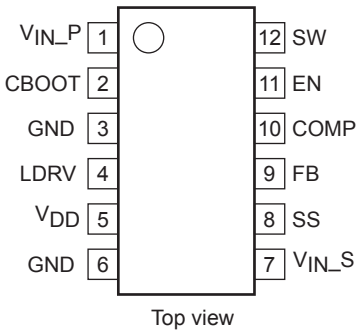




Block Diagram

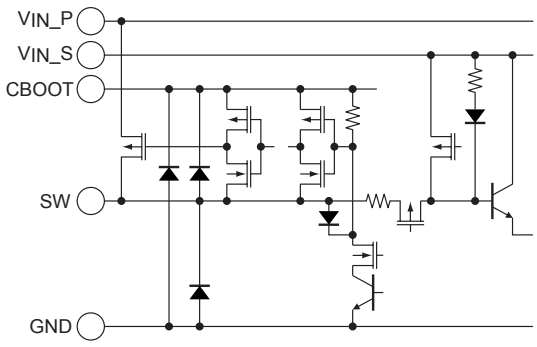
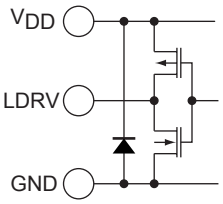
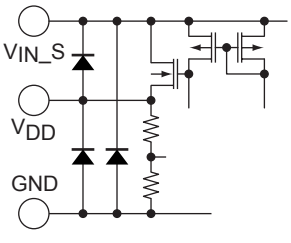


Pin Assignment



Top view

Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	V_{IN}_P	Power supply pin.	
2	CBOOT	Bootstrap capacity connection pin. This pin becomes a GATE drive power supply of an external Nch MOSFET. Connect a bypath capacitor CBOOT and SW.	
12	SW	Pin to connect with switching node. Connect the source of external upper Nch MOSFET and the drain of external lower Nch MOSFET.	
3, 6	GND	Ground pin. Each reference voltage is based on the voltage of the ground pin.	
4	LDRV	An external the lower MOSFET gate drive pin.	
5	V_{DD}	Power supply pin for an external the lower MOS-FET gate drive.	
7	V_{IN}_S	Control circuit supply pin. This pin is monitored by UVLO function. When the voltage of this pin become 8V or more by UVLO function. The IC state and the soft start function operates.	

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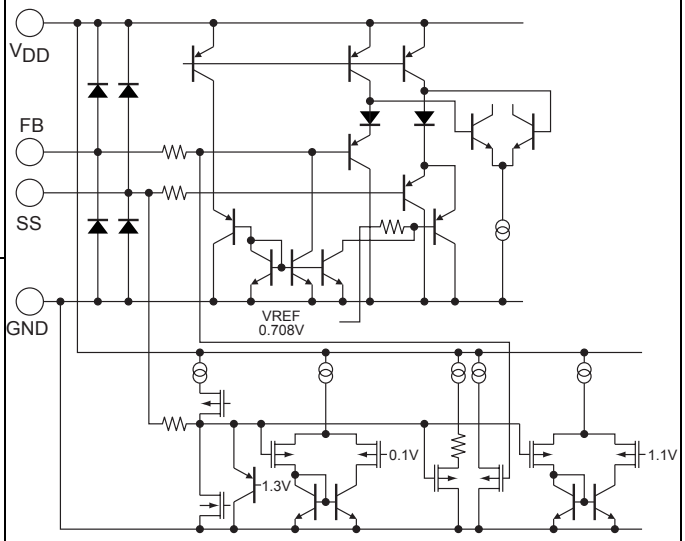
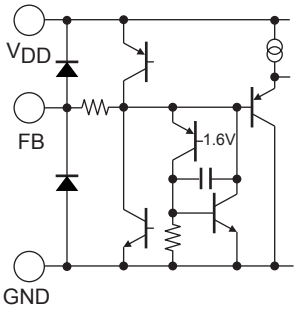
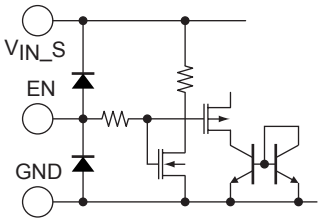
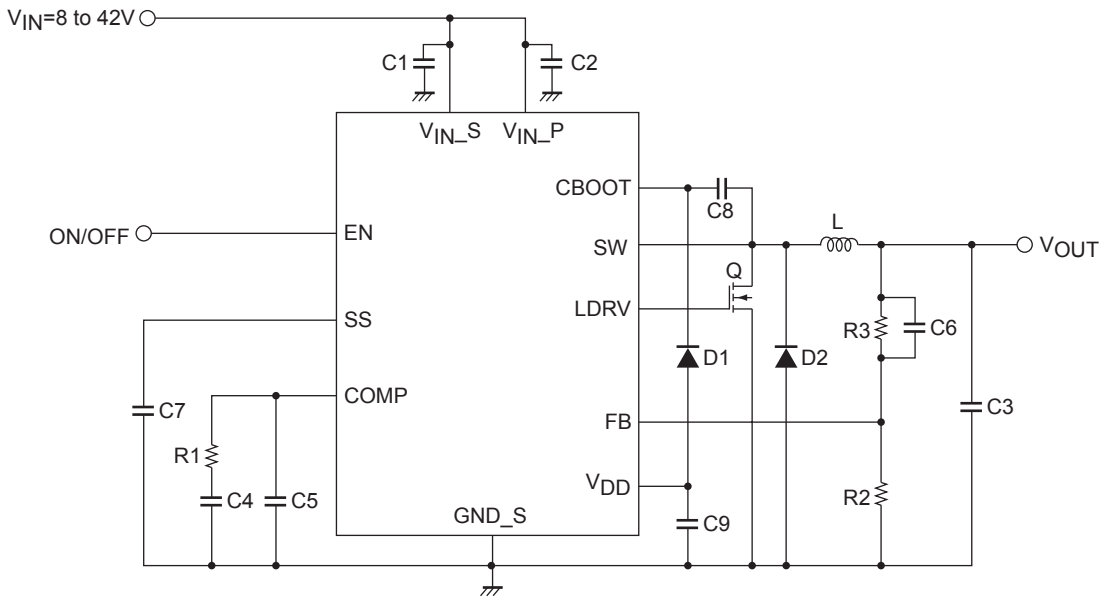
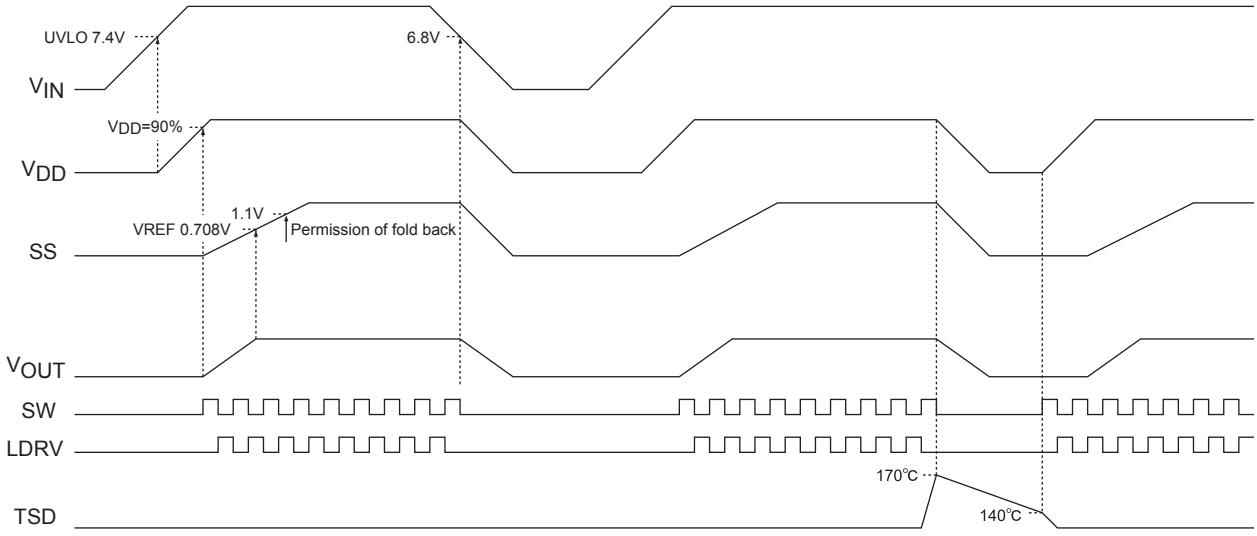
Pin No.	Pin name	Function	Equivalent circuit
8	SS	Pin to connect a capacitor for soft start. A capacitor for soft start is charged by using the voltage of about 5μA. This pin ends the soft start period by using the voltage of about 1.1V and the frequency fold back function becomes active.	
9	FB	Error amplifier reverse input pin. By operating the converter, the voltage of this pin becomes 0.7V. The voltage in which the output voltage is divided by an external resistance is applied to this pin. Moreover, when this pin voltage becomes 0.1V or less after a soft start ends, the oscillatory frequency becomes 1/3.	
10	COMP	Error amplifier output pin. Connect a phase compensation circuit between this pin and GND.	
11	EN	ON/OFF pin.	

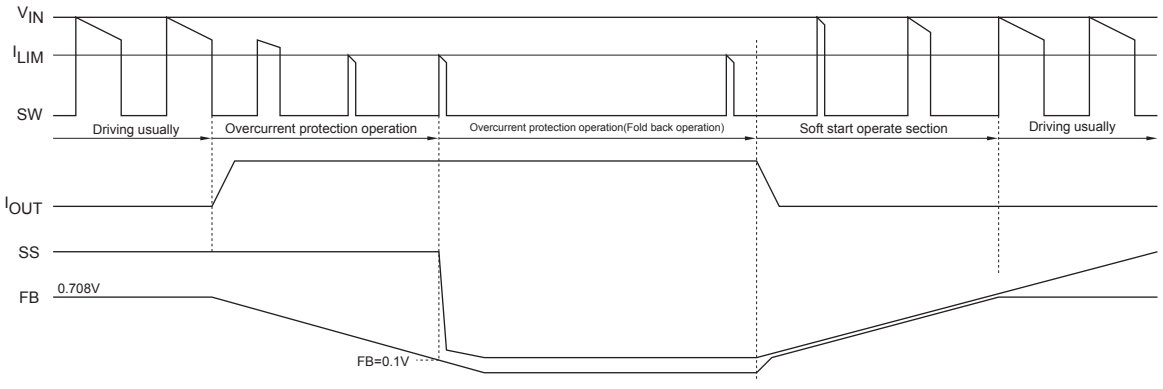
Sample Application Circuit



Boot sequence, UVLO, and TSD operation



Sequence of overcurrent protection



Various settings

Output voltage setting

The setting of output voltage (V_{OUT}) follows the following expressions (1).

$$V_{OUT} = (1 + \frac{R3}{R2}) \times Vref = (1 + \frac{9.1k}{1.5k}) \times 0.708 \text{ (typ)} \quad [V] \qquad (1)$$

EX) To adjust the output voltage to 5V, it becomes R2=1.5kΩand R3=9.1kΩ.

Soft start setting

The setting of soft start capacitor (C7) follows the following expressions (2).

$$C7 = \frac{I_{SS} \times T_{SS}}{VREF} = \frac{5\mu \times T_{SS}}{0.708V} \quad [\mu F] \qquad (2)$$

I_{SS}: Charge current value, T_{SS}: Soft start time

EX) To adjust the soft start time to about 1.5ms, it becomes C5=0.1μF.

Boot strap capacitor

Boot strap capacitor (C8) is with a capacitor about 1000 times Ciss of power MOSFET of building into. Ciss of built-in power MOSFET is 505pF.

Ex) C8=505pF×1000=0.505μF. C8 recommends 0.1 to 1μF.

Selection of input smoothness capacitor

The ripple current flows to the input side capacitor of the DC-DC converter by the thing that IC does the switching. Duty extends by the flow by there are a lot of output currents of the ripple current that flows to the input side capacitor just like the input current, and the input voltage low and a lot of ripple currents flow, too. Please select the big one of a permissible ripple current from the value requested from the calculating formula. It must arrange near Power IC, and inductance by the pattern must become small when you mount the input side capacitor. Calculating formula (3) from which the execution value is requested becomes the following.

$$I_{RIP\_in} = \sqrt{D(1-D)} \times I_{OUT} \quad [Arms] \qquad (3)$$

D is Duty Cycle defined by V_{OUT}/V_{IN}.

Selection of output smoothness capacitor

Please select the one with small impedance by the high frequency when the ripple voltage of the output is decided by the impedance of the output smoothness capacitor, and you want to suppress the voltage of the output ripple small. Moreover, please select it so as not to exceed the permissible ripple current value. Moreover, because the high frequency noise is removed, using the ceramic capacitor together is effective. Using of the aluminum electrolytic capacitor or the polymer aluminum electrolytic capacitor and the ceramic capacitor together is recommended. Calculating formula (4) from which the execution value is requested becomes it as follows.

$$I_{RIP\_out} = \frac{1}{2\sqrt{3}} \times \frac{V_{OUT}(V_{IN}-V_{OUT})}{L \times f_{OSC} \times V_{IN}} = \quad [Arms] \qquad (4)$$

How to request smooth chalk coil

L1: Please note generation of heat of the choke coil because of the overload and DC magnetic saturation when the load is short-circuited.

The inductance value is decided because of voltage (V_{RIP}) of the output ripple and the impedance of the output capacitor of the switching frequency. Calculating formula (5) from which the most small inductance is requested becomes it as follows.

$$L \text{ min} = \frac{V_{IN} - V_{OUT}}{f_{OSC} \times V_{IN}} \times \frac{V_{OUT} \times R_C}{V_{RIP}} \quad [\mu H] \qquad (5)$$

ESR is used by the above expression instead of the impedance of the output capacitor. In many cases, the impedance of the output capacitor of the switching frequency depends on a reason extremely near R_C as for this. However, the actual impedance is used in the ceramic capacitor instead of R_C.

Ex) V_{IN} (max)=40V, V_{OUT}=12V, V_{RIP}=100mV, R_C=10mΩ, f_{OSC}=385kHz

$$L \text{ min} = \frac{40V - 12V}{385k \times 40V} \times \frac{12V \times 10m}{100mV} \approx 2.2 \quad [\mu H] \qquad (6)$$

In actual part selection, inductance is selected from the decision of the ripple voltage with the selection of the start capacitor. Please consider the maximum value, minimum value, the output voltage, and the load change of the input voltage. The ripple current of inductance is recommended to be confirmed because it often becomes the selection criterion of the output inductance. Calculating formula (7) from which the ripple current value is requested becomes it as follows.

$$I_{RIP} = \frac{V_{IN} - V_{OUT}}{f_{OSC} \times L} \times D \quad [A] \qquad (7)$$

D is Duty Cycle defined by V_{OUT}/V_{IN}.

Moreover, an important item is a ripple current shown with I_{RIP}/I_{OUT}. In general, there is no problem if the ripple element is less than 50%. The inductance loss greatness and minute increases when there are a lot of ripple elements.

Ex) V_{IN}=24V, V_{OUT}=5V, f_{OSC}=385kHz, L=10μH

$$I_{RIP} = \frac{24V - 5V}{385k \times 10\mu} \times 0.2 = 0.99 \quad [A] \qquad (8)$$

Pattern layout note

Input capacitor

The ripple current flows to the input capacitor of the DC-DC converter by the thing that IC does the switching. Mounting and the pattern must be arranged in the input capacitor near the V_{IN}_P pin, and inductance by the pattern must become small.

C2: Please connect it near between the V_{IN}_P pin and the GND pin of IC.

C1: Please connect the bypass capacitor connected with the V_{IN}_S pin of IC near between the V_{IN}_S pin and the GND pin.

(Unusually, please note that intense ringing might be caused in the V_{IN} pin if the bypass capacitor is connected. The recommendation becomes 1000pF.)

MOSFET

Q (external FET) drives by using Nch-MOSFET. The SW node generates Q along with ON/OFF, and it changes, and the high frequency noise is generated between V_{IN} + and GND. It influences a peripheral pattern and the element at this time. Please the pattern of the gate and the SW node on a low side must draw around neither LDRV nor the SW pin of IC, and wire for the pattern fat as much as possible. The wiring for LDRV and the SW pin is recommended to wire for the pattern between GND patterns to prevent the noise from influencing it.

When low side FET is turned on, it becomes the current pathway of inductor (L) →V_{OUT} (load) →PGND→. It becomes possible to suppress the generation of the noise by doing the thing and the pattern wiring that reduces the area of this current pathway fat, and it becomes malfunction prevention. Therefore, please arrange Q, C2, and C3 in neighborhood.

Small signal system: FB, COMP, EN, CBOOT, V_{DD}, SS

Please connect parts connected with the small signal system with short wiring as much as possible in IC neighborhood, and make GND of parts common with the GND pattern of IC. Please do not wire the under of the wiring for the inductor and the SW node and neighborhood for the FB pattern. Please there must be a possibility of causing the malfunction, and avoid and wire for the pattern.