freescale
飞思卡尔(深圳)功率半导体有限公司

AOD609

Complementary Enhancement Mode Field Effect Transistor

General Description

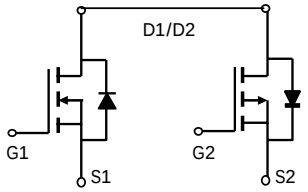
The AOD609 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

Features

n-channel
V_{DS} (V) = 40V, I_D = 12A (V_{GS}=10V)
$R_{DS(ON)}$< 30mΩ (V_{GS}=10V)
$R_{DS(ON)}$< 40mΩ (V_{GS}=4.5V)
p-channel
V_{DS} (V) = -40V, I_D = -12A (V_{GS}=-10V)
$R_{DS(ON)}$< 45mΩ (VGS= -10V)
$R_{DS(ON)}$< 66mΩ (VGS= -4.5V)

Green Product RoHS Compliant

Top View
Drain Connected to Tab



n-channel **p-channel**

Absolute Maximum Ratings T_A=25°C unless otherwise noted					
Parameter		**Symbol**	**Max n-channel**	**Max p-channel**	**Units**
Drain-Source Voltage		V_{DS}	40	-40	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current [B,H]	T_C=25°C	I_D	12	-12	A
	T_C=100°C		12	-12	
Pulsed Drain Current [B]		I_{DM}	30	-30	
Avalanche Current [C]		I_{AR}	14	-20	
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	9.8	20	mJ
Power Dissipation	T_C=25°C	P_D	27	30	W
	T_C=100°C		14	15	
Power Dissipation	T_A=25°C	P_{DSM}	2	2	W
	T_A=70°C		1.3	1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	-55 to 175	°C

Thermal Characteristics: n-channel and p-channel						
Parameter		**Symbol**	**Device**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A,D]	t ≤ 10s	$R_{\theta JA}$	n-ch	17.4	25	°C/W
Maximum Junction-to-Ambient [A,D]	Steady-State		n-ch	50	60	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JC}$	n-ch	4	5.5	°C/W
Maximum Junction-to-Ambient [A,D]	t ≤ 10s	$R_{\theta JA}$	p-ch	16.7	25	°C/W
Maximum Junction-to-Ambient [A,D]	Steady-State		p-ch	50	60	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JC}$	p-ch	3.5	5	°C/W

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N Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.7	2.5	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=12A		24	30	mΩ
		T_J=125°C		37	46	
		V_{GS}=4.5V, I_D=8A		31	40	
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=12A		25		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, f=1MHz		516	650	pF
C_{oss}	Output Capacitance			82		pF
C_{rss}	Reverse Transfer Capacitance			43		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		4.6	6.9	Ω
SWITCHING PARAMETERS						
Q_g (10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=20V, I_D=12A		8.3	10.8	nC
Q_{gs}	Gate Source Charge			2.3		nC
Q_{gd}	Gate Drain Charge			1.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=20V, R_L=1.4Ω, R_{GEN}=3Ω		6.4		ns
t_r	Turn-On Rise Time			3.6		ns
$t_{D(off)}$	Turn-Off DelayTime			16.2		ns
t_f	Turn-Off Fall Time			6.6		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=12A, dI/dt=100A/µs		18	24	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=12A, dI/dt=100A/µs		10		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A =25°C. The power dissipation P_{DSM} and current rating I_{DSM} are based on $T_{J(MAX)}$=150°C, using the steady state junction-to-ambient thermal resistance.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation lim for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

H. The maximum current rating is limited by bond-wires.

*This device is guaranteed green after data code 8X11 (Sep th 2008).

Rev4: Aug 2009

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL

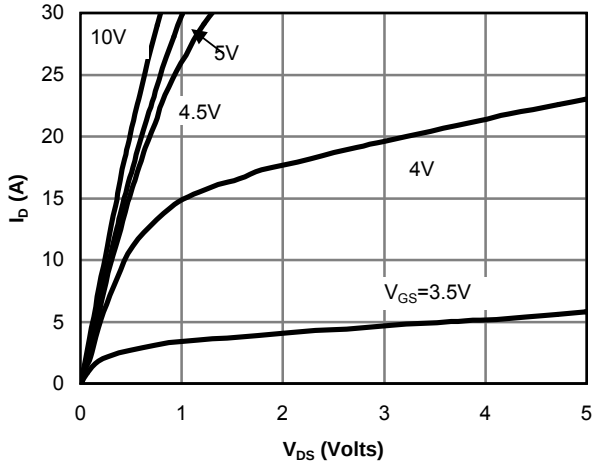


Fig 1: On-Region Characteristics

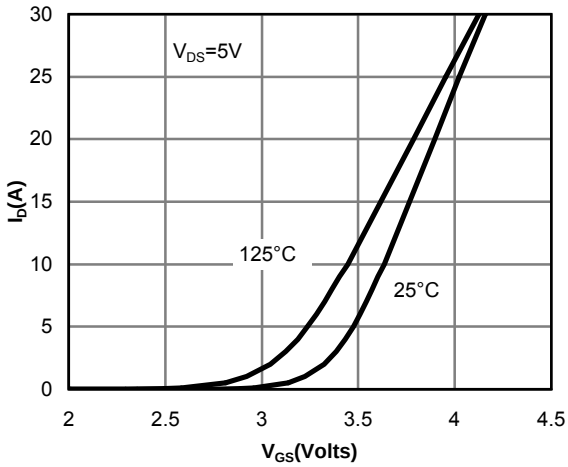


Figure 2: Transfer Characteristics

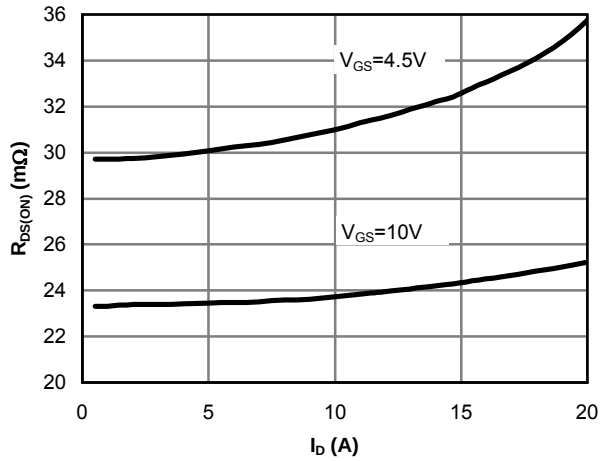


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

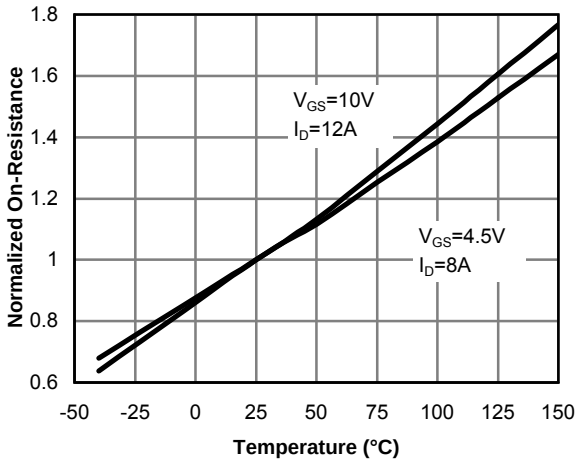


Figure 4: On-Resistance vs. Junction Temperature

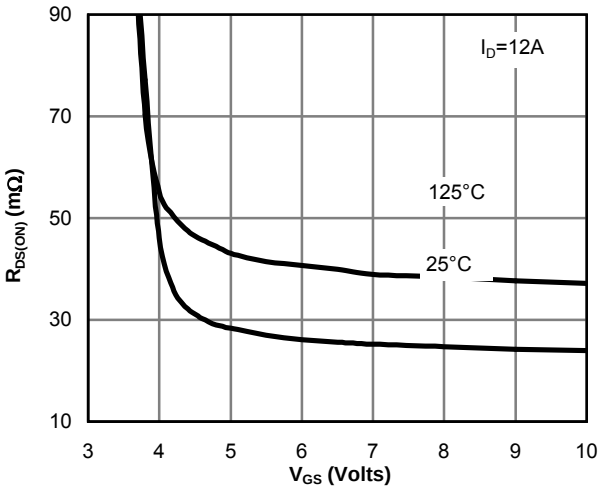


Figure 5: On-Resistance vs. Gate-Source Voltage

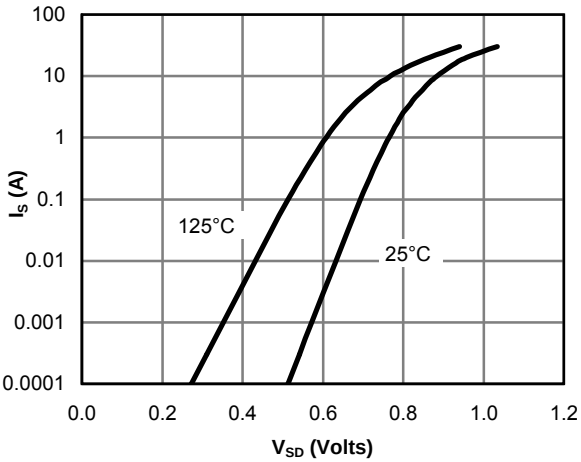


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL

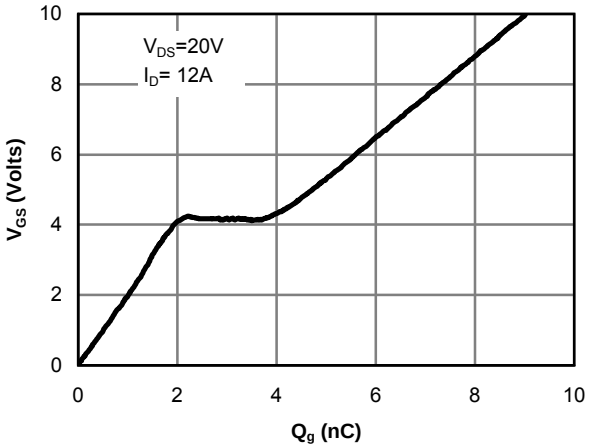


Figure 7: Gate-Charge Characteristics

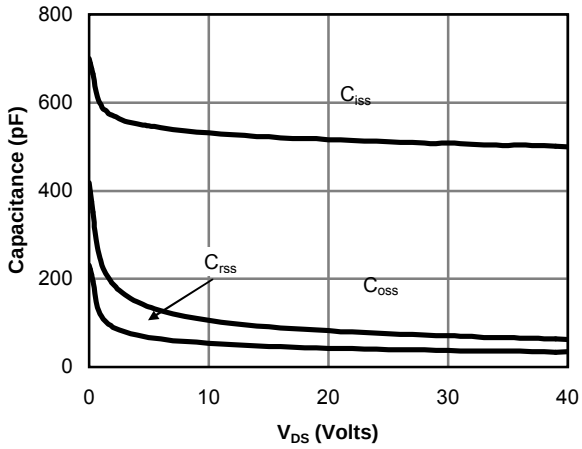


Figure 8: Capacitance Characteristics

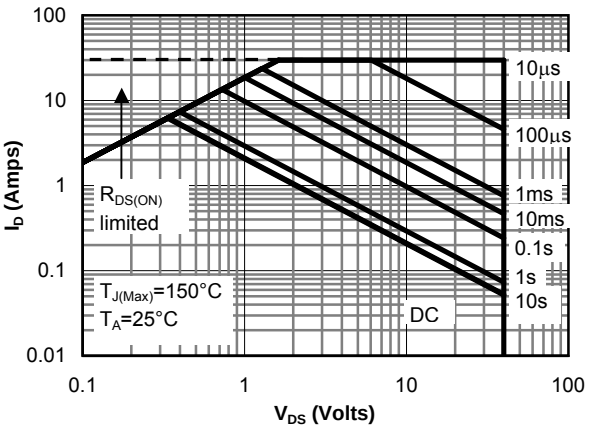


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

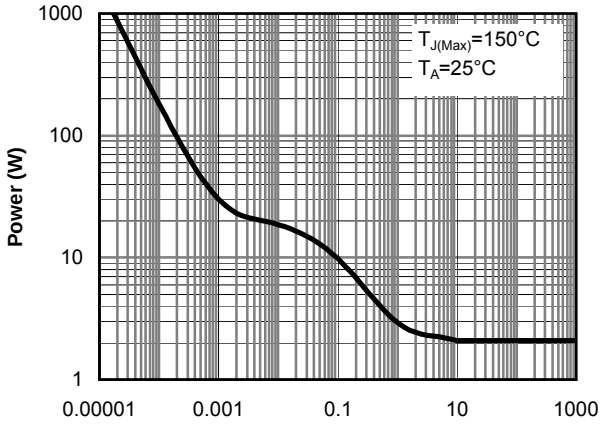


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

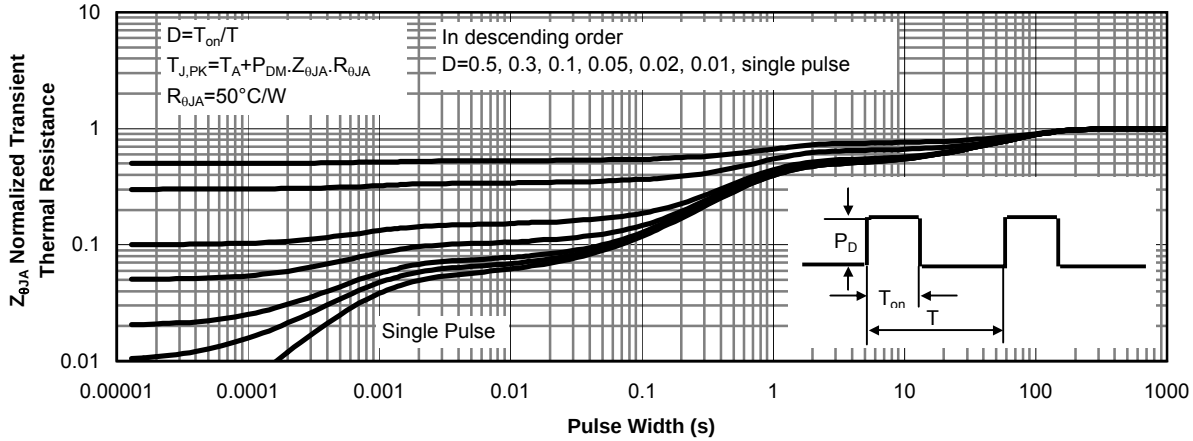
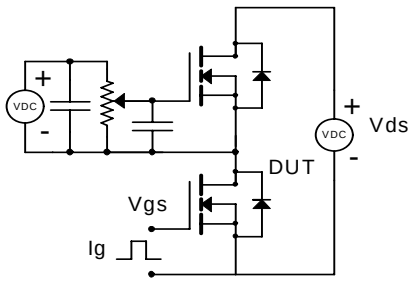
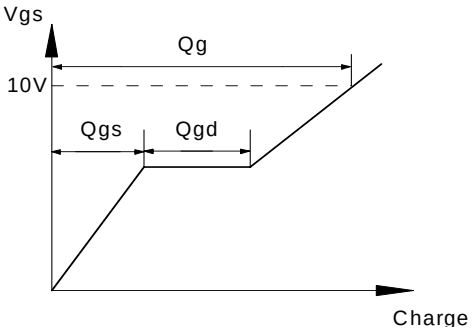


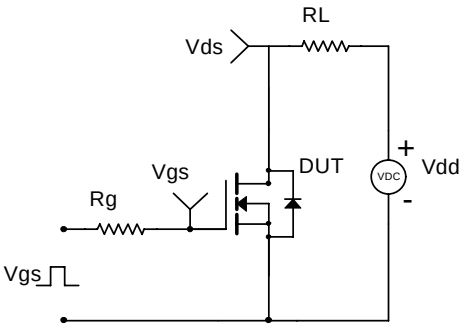
Figure 11: Normalized Maximum Transient Thermal Impedance

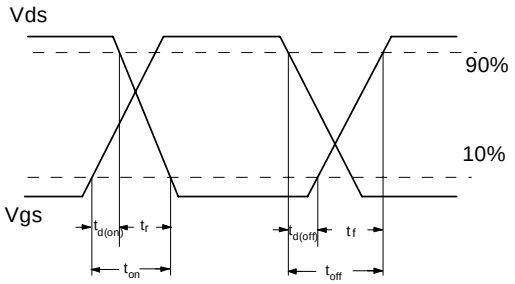
Gate Charge Test Circuit & Waveform



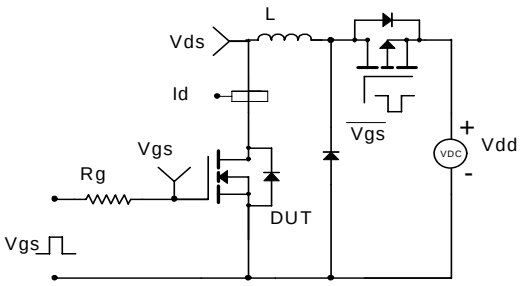


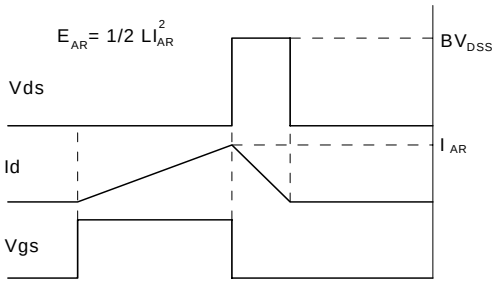
Resistive Switching Test Circuit & Waveforms



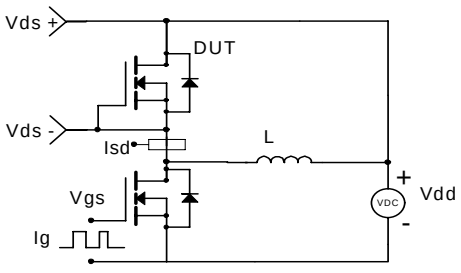


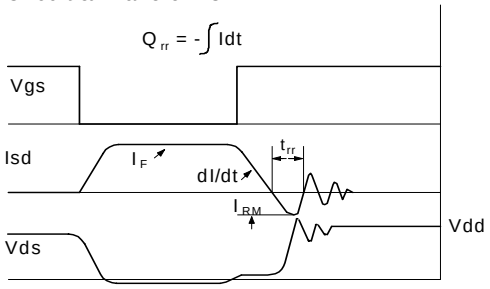
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms





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Complementary Enhancement Mode Field Effect Transistor

P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D= -250µA, V_{GS}=0V	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}= -40V, V_{GS}=0V			-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D= -250µA	-1.7	-2	-3	V
$I_{D(ON)}$	On state drain current	V_{GS}= -10V, V_{DS}= -5V	-30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}= -10V, I_D= -12A		36	45	mΩ
		T_J=125°C		52	65	
		V_{GS}= -4.5V, I_D= -8A		51	66	
g_{FS}	Forward Transconductance	V_{DS}= -5V, I_D= -12A		22		S
V_{SD}	Diode Forward Voltage	I_S= -1A,V_{GS}=0V		-0.76	-1	V
I_S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}= -20V, f=1MHz		900	1125	pF
C_{oss}	Output Capacitance			97		pF
C_{rss}	Reverse Transfer Capacitance			68		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		14		Ω
SWITCHING PARAMETERS						
Q_g (-10V)	Total Gate Charge	V_{GS}= -10V, V_{DS}= -20V, I_D= -12A		16.2	21	nC
Q_g (-4.5V)	Total Gate Charge			7.2	9.4	nC
Q_{gs}	Gate Source Charge			3.8		nC
Q_{gd}	Gate Drain Charge			3.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}= -10V, V_{DS}= -20V, R_L=1.4Ω, R_{GEN}=3Ω		6.2		ns
t_r	Turn-On Rise Time			8.4		ns
$t_{D(off)}$	Turn-Off DelayTime			44.8		ns
t_f	Turn-Off Fall Time			41.2		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F= -12A, dI/dt=100A/µs		21	27	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F= -12A, dI/dt=100A/µs		14		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A =25°C. The power dissipation P_{DSM} and current rating I_{DSM} are based on $T_{J(MAX)}$=150°C, using t ≤ 10s junction-to-ambient thermal resistance.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

H. The maximum current rating is limited by bond-wires.

*This device is guaranteed green after data code 8X11 (Sep 9th 2008).

Rev4: Aug 2009

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

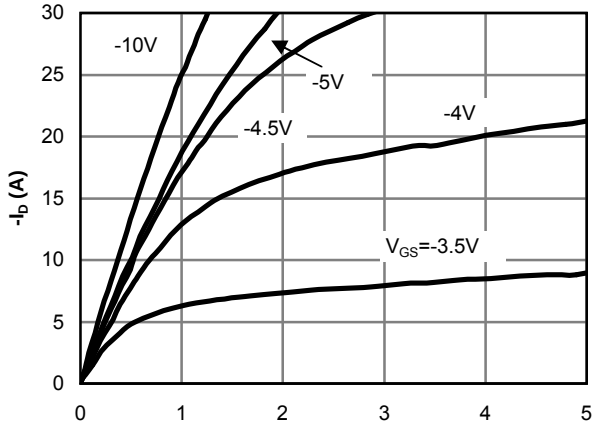


Fig 12: On-Region Characteristics

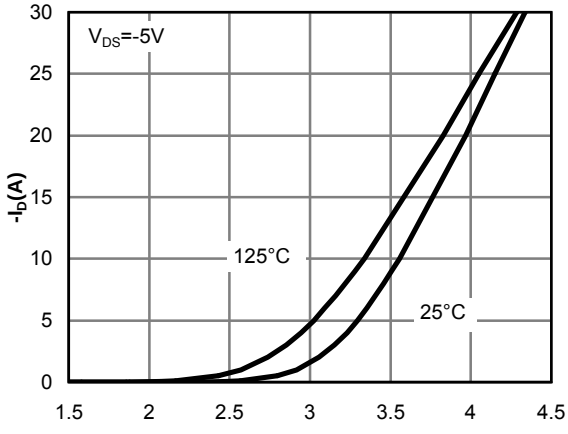


Figure 13: Transfer Characteristics

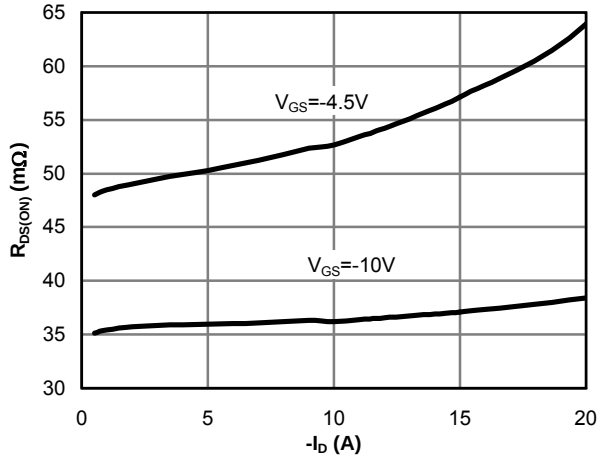


Figure 14: On-Resistance vs. Drain Current and Gate Voltage

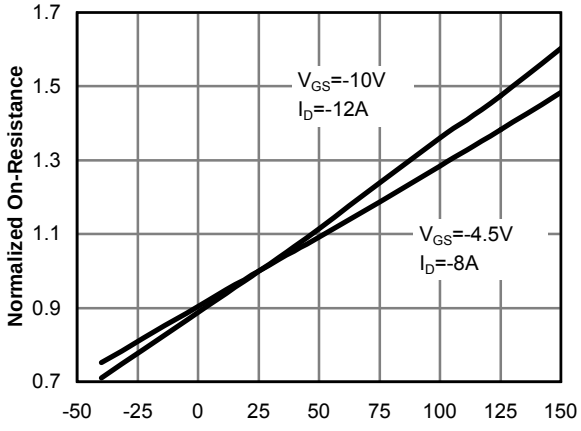


Figure 15: On-Resistance vs. Junction Temperature

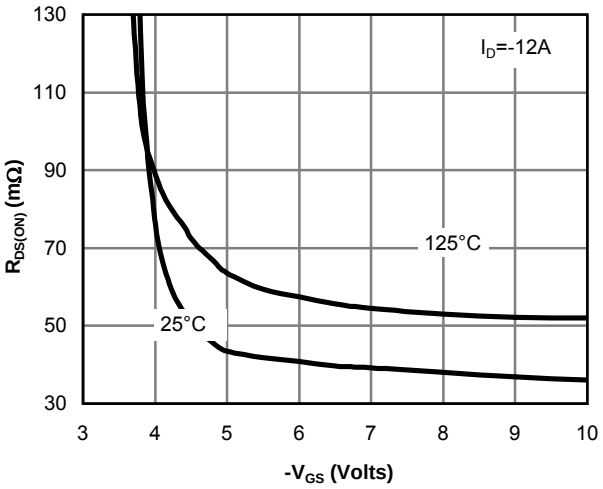


Figure 16: On-Resistance vs. Gate-Source Voltage

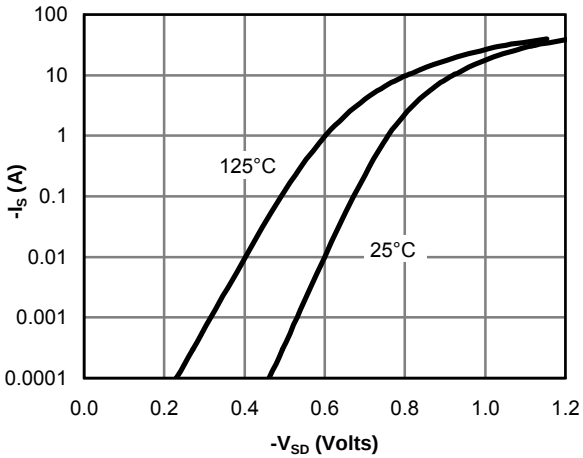


Figure 17: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

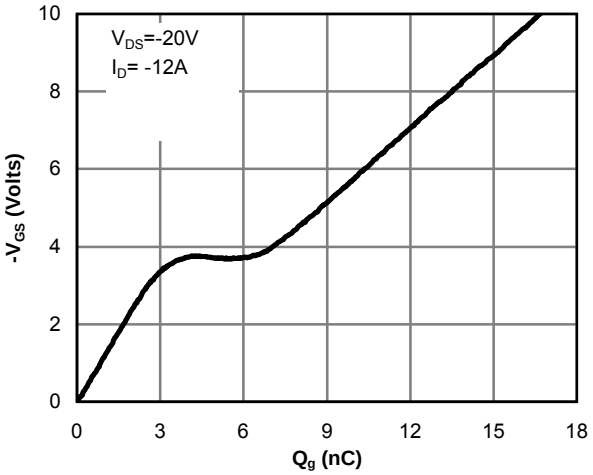


Figure 18: Gate-Charge Characteristics

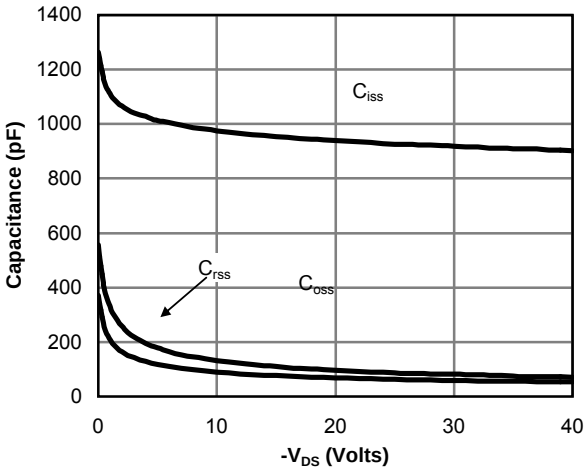


Figure 19: Capacitance Characteristics

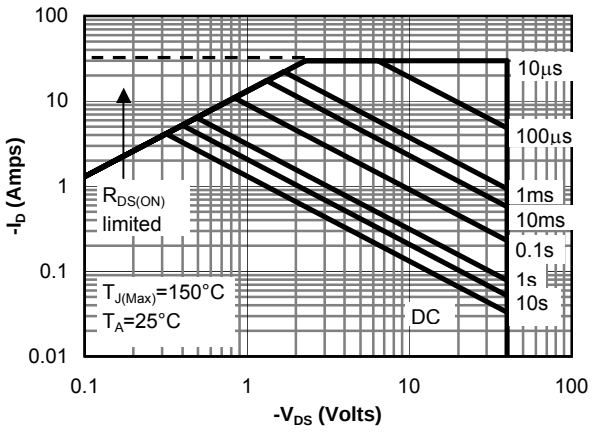


Figure 20: Maximum Forward Biased Safe Operating Area (Note E)

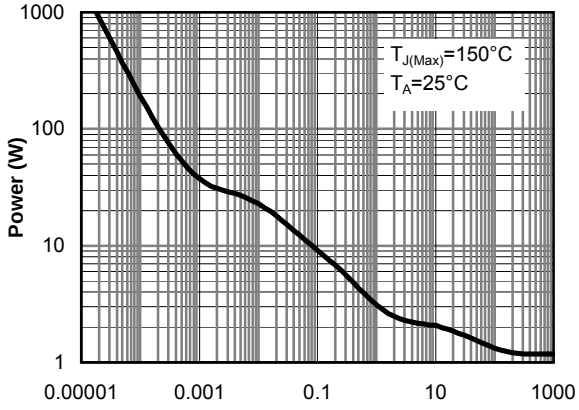


Figure 21: Single Pulse Power Rating Junction-to-Ambient (Note E)

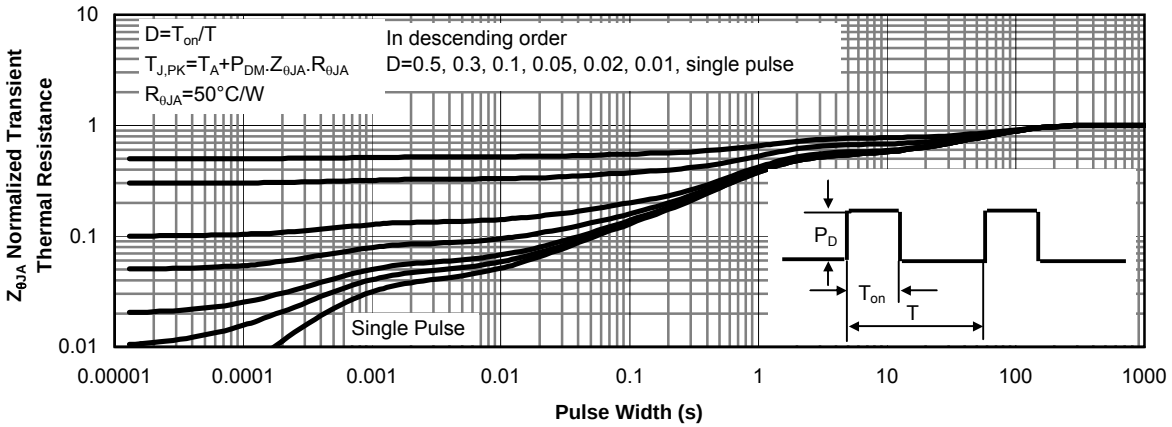
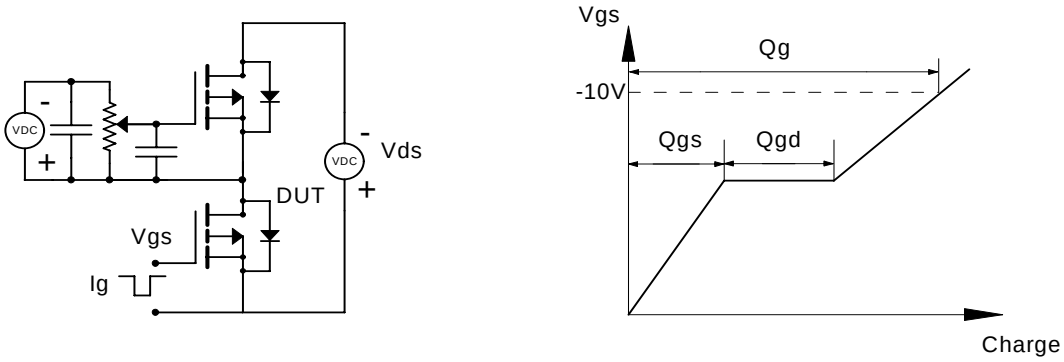
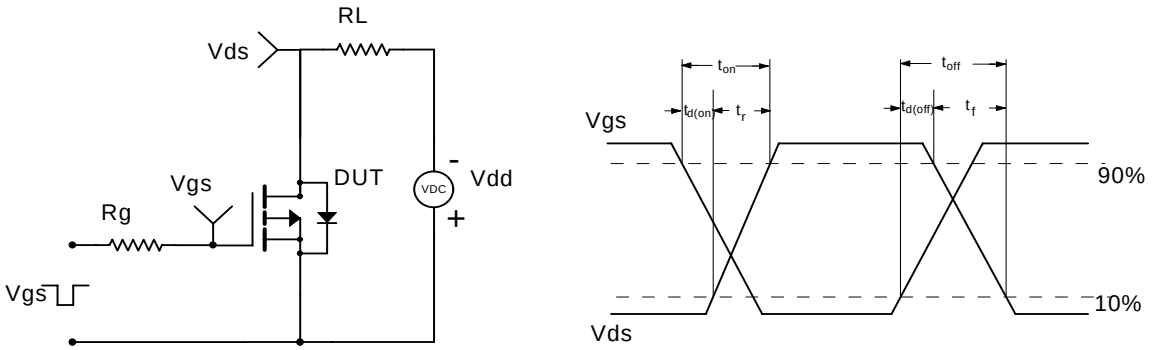


Figure 22: Normalized Maximum Transient Thermal Impedance

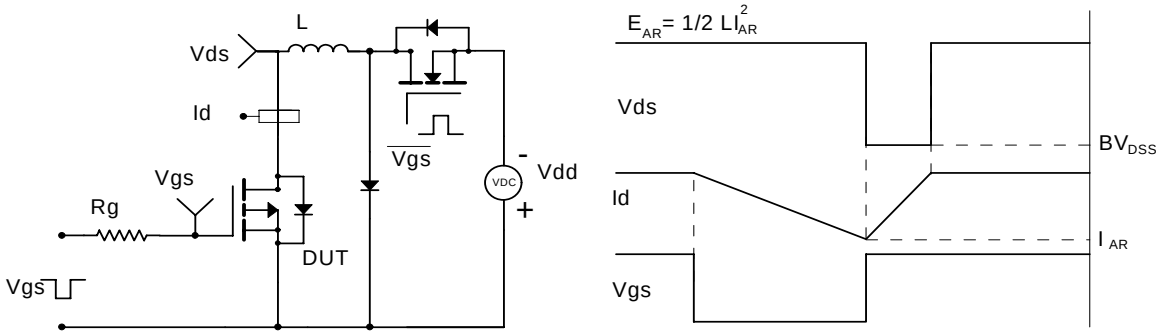
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms