

R8821
Brief Sheet
16-BIT RISC MICROCONTROLLER

1. Features

I CPU Core

- RDC's proprietary RISC architecture
- Five-stage pipeline
- CPU clock speed: 40MHz
- Supports CPU ID
- Supports 32 PIO pins
- Static & synthesizable design

I Bus Interface

- Multiplexed address and data bus
- Supports a non-multiplexed address bus A[19:0]
- 8-bit or 16-bit external bus dynamic access

I ROM/RAM/DRAM Controller and Addressing Space

- 1M-byte memory address space
- 64K-byte I/O space
- With 8-bit or 16-bit boot ROM bus size
- Supports 64Kx16, 128Kx16, 256Kx16 EDO or FP DRAM with auto-refresh control

I Two independent DMA channels

I Asynchronous Serial Channels

- Supports two asynchronous serial channels with hardware handshaking signals

I Interrupt Controller

- The Interrupt controller with seven maskable external interrupts and one non-maskable external interrupt

I Programmable Chip-select Logic

- Programmable chip-select logic for memory or I/O bus cycle decoder

I Programmable Wait-state Generators

I Counters/Timers

- Three independent 16-bit timers and one independent programmable watchdog timer

I Software Compatible with the 80C186 Microprocessor

I Operating Voltage Range

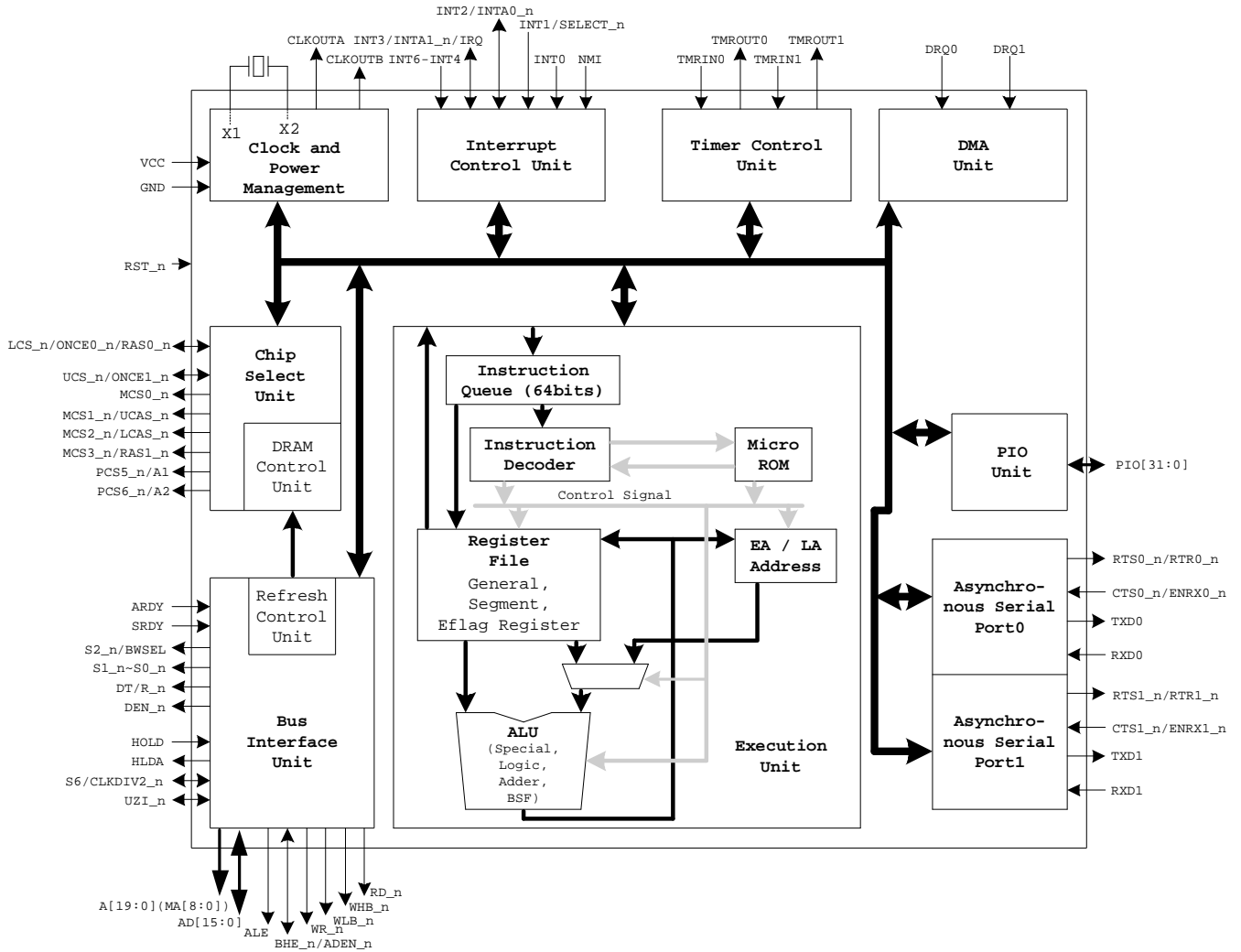
- Core voltage: 5V ± 10%
- I/O voltage: 5V ± 10%

I Ambient Temperature: 0 ~ +70°C

I Package Type

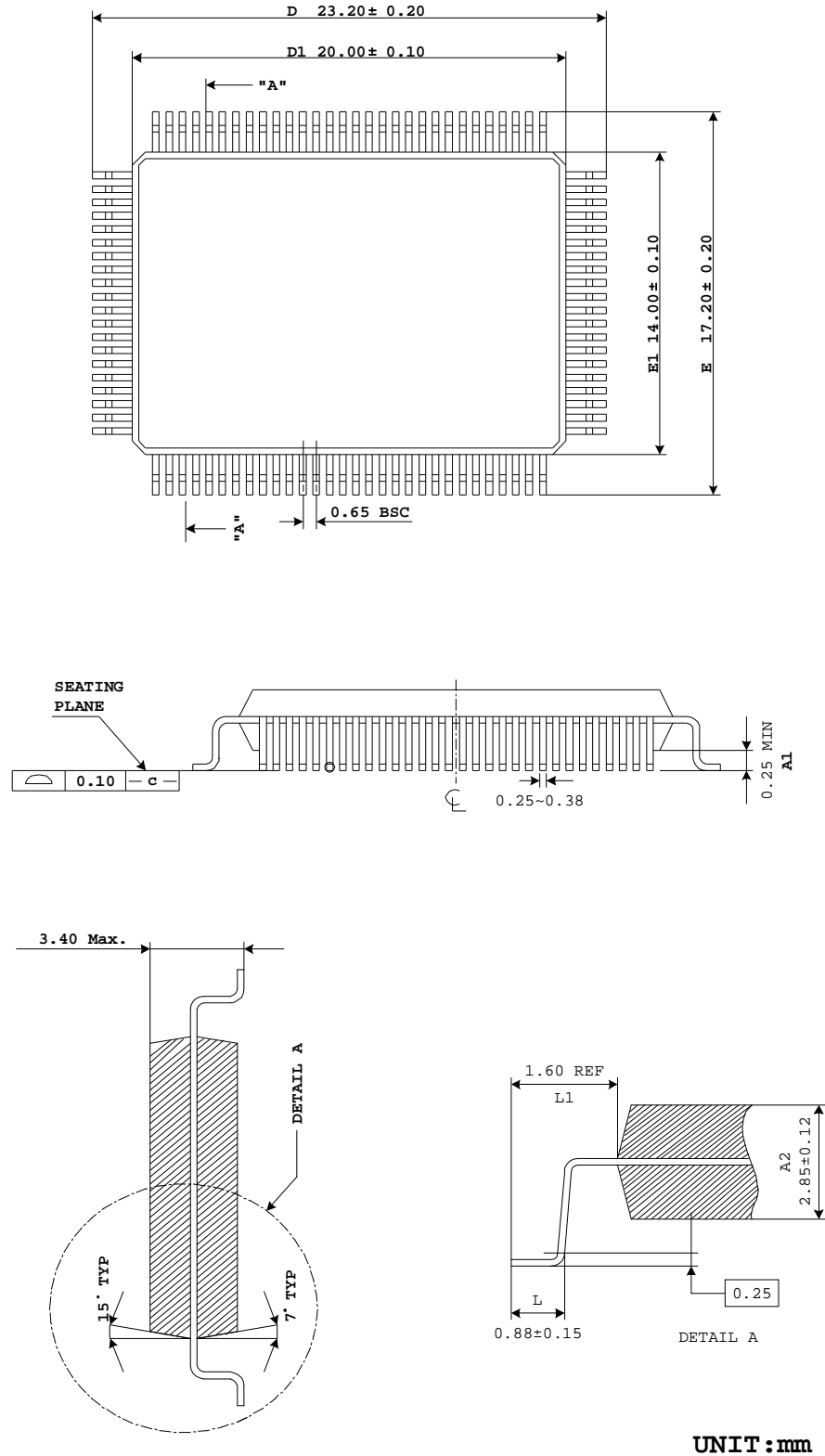
- 100-pin PQFP & 100-pin LQFP

2. Block Diagram

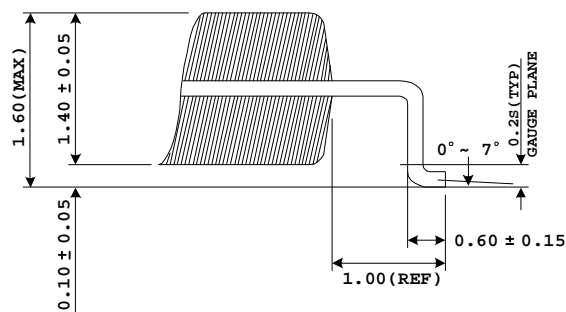
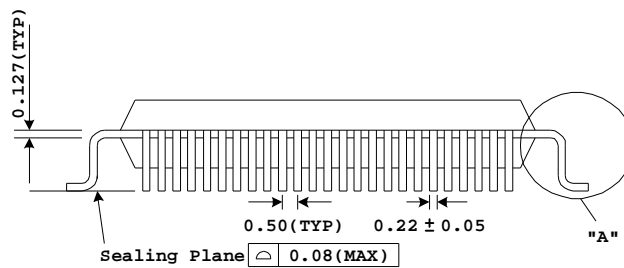
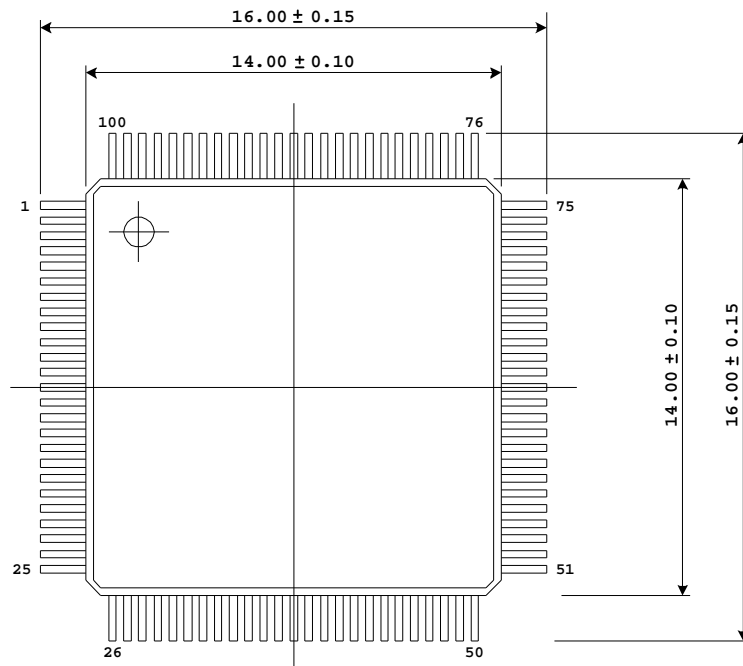


3. Package Information

PQFP 100 pins



LQFP 100 pins



UNIT : mm