



AKD4426-SA

AK4426 Evaluation Board Rev.2

General Description

AKD4426-SA is an evaluation board for AK4426 (192kHz sampling 24Bit Stereo DAC with 2Vrms Output). AKD4426-SA has a digital audio interface (AK4118) of Optical input and can easily achieve the interface with digital audio system. Therefore, it is easy to evaluate the sound quality of AK4426.

■ **Ordering Guide**

AKD4426-SA ---- AK4426 Evaluation Board

Function

On-board digital audio interface. (AK4118)

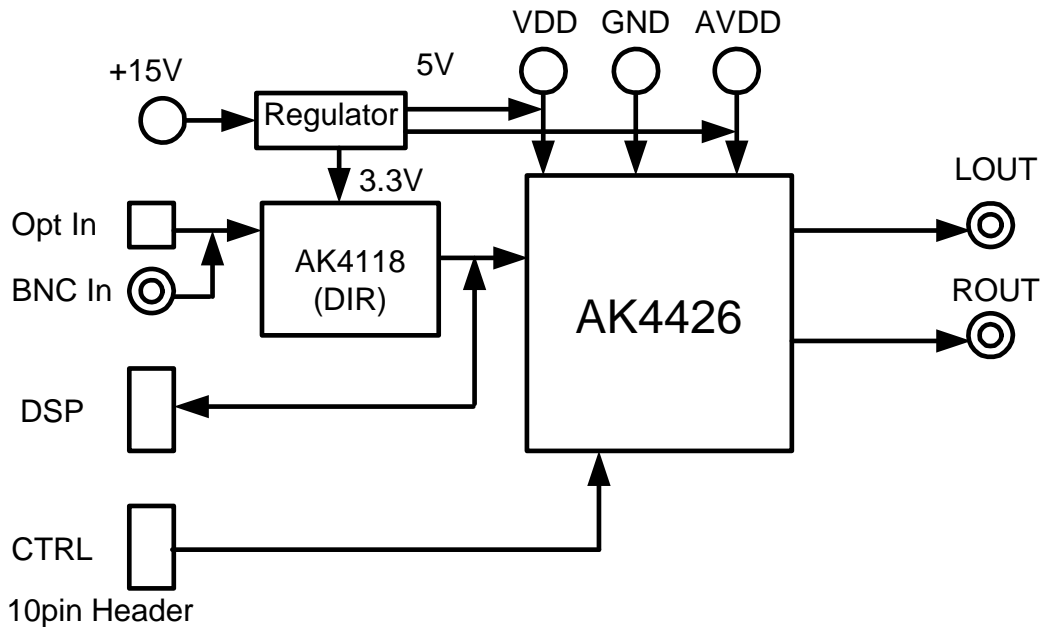


Figure 1. AKD4426-SA Block diagram
 (* Circuit diagram are attached at the end of this manual.)

Board Outline Chart

■ Outline Chart

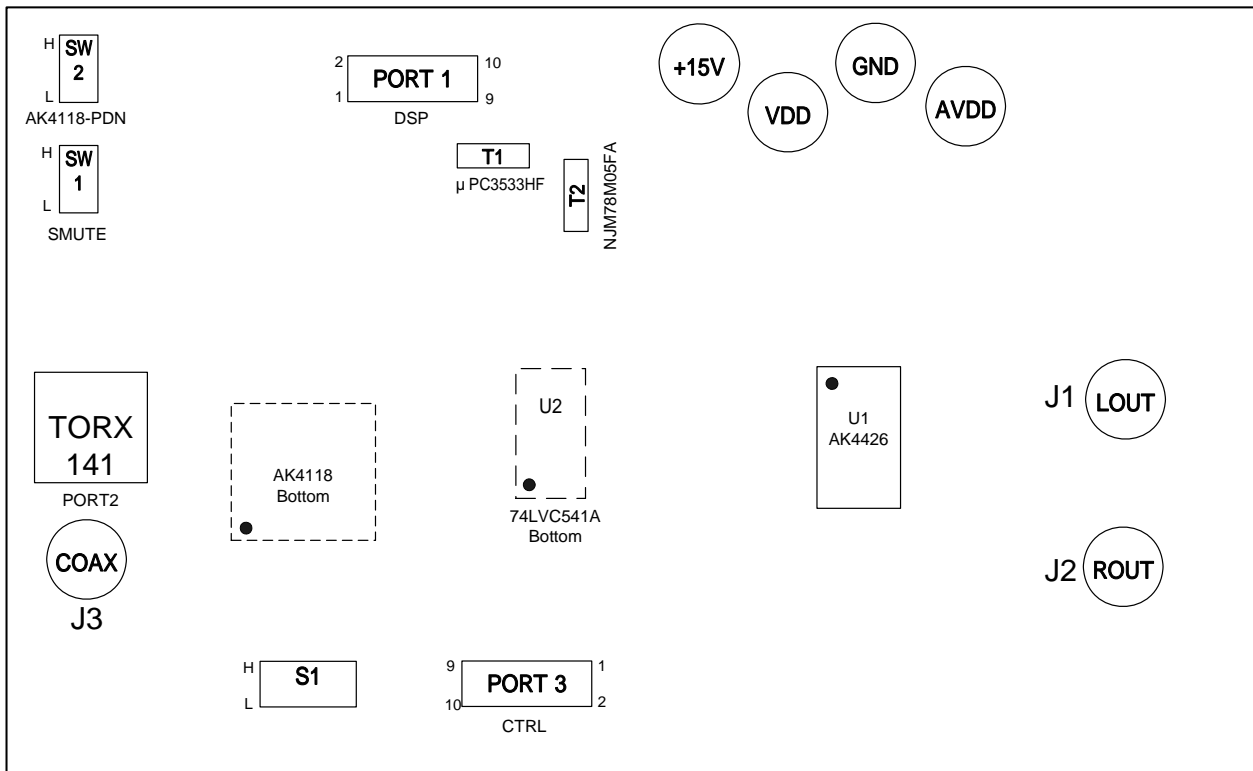


Figure 2. AKD4426-SA Outline Chart

■ Comment

- (1) LOUT, ROUT (BNC-JACK)
It is analog signal output Jack. The signal is output from LOUT/ROUT pins.
- (2) COAX, PORT1, PORT2 (Digital signal connector)
COAX (BNC-JACK): Digital signal (SPDIF, Fs: 8 ~ 192kHz) is input to the AK4118. (Default)
PORT1 (10 pin header): The clock and data can be input and output with this connector.
PORT2 (Optical Connector): Optical digital signal (SPDIF, Fs: 32 ~ 108kHz) is input to the AK4118.
- (3) PORT3 (10 pin header)
Control port. Connect the bundled cable into this port.
- (4) +15V, VDD, GND, AVDD
These are the power supply connectors. Connect power supply with these pins.
As for the detail comments, refer to the setup of power supply on the next page.
- (5) SW1, SW2, S1 (Switch)
SW1: This switch is not used on the AKD4426-SA.
SW2: Reset of AK4118. Keep "H" during normal operation.
S1: Setting of audio serial interface format and frequency of MCKO that is output from AK4118.

■ Operation sequence

1) Set up the power supply lines.

Each supply line should be distributed from the power supply unit.

Name of jack	Color of jack	Voltage Range	Using	Default Setting	Default
+15V	Red	+7~+20V	Regulator : VDD and AVDD for AK4426. The power supply for AK4118, 74LVC541 and other logic circuit.	Should be connected.	+15V
VDD	Orange	+4.5~+5.5V	VDD of AK4426	Should be connected. (Default, Note1)	+5V
AVDD	Orange	+4.5~+5.5V	AVDD of AK4426	Should be connected. (Default, Note2)	+5V
GND	Black	0V	Ground	Should be connected.	0V

Table 1. Set up of power supply lines

Note 1) VDD for AK4426 can supply to connect Regulator. In this case, should be to “short” of R58 and no connected “VDD” of jack.

Note 2) AVDD for AK4426 can supply to connect Regulator. In this case, should be to “short” of R59 and no connected “AVDD” of jack.

2) DIP Switch setting:

Refer to Table 2, Table 3 and Table 4.

3) Power Down:

The AK4118 should be reset once by bringing SW2 (AK4118 PDN) “L” upon power-up.

■ Evaluation mode

1. Using DIR (COAX) (Default)

The DIR generates MCLK, BICK, LRCK and SDATA from the received data through BNC connector (J3). It is possible to evaluate the AK4426 by using CD disk. Should be no connected to PORT1 (DSP).

Setting: R41: short (0Ω); R42: open

* COAX is recommended for an evaluation of the Sound quality.

2. Using DIR (Optical Link)

The DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector (PORT2: TORX141). It is possible to evaluate the AK4426 by using CD disk. Should be no connected to PORT1 (DSP).

Setting: R41: open; R42: short (0Ω)

3. Supply all interface signals that include master clock via PORT1 from external equipments..

Setting: R43, R44, R45, R46: open

R47, R48, R49, R50: short (0Ω)

Note) The above work of removing (open) or shorting resistors need to modify the connection by soldering.

■ **Setting of DIP switch**

[S1]: AK4118 setting (ON = “H”, OFF = “L”)

No.	Pin	OFF	ON	Default
1	DIF1	AK4118’s Audio Data Format setting		L
2	DIF0	Refer to Table 3		L
3	OCKS1	AK4118’s Master Clock setting		H
4	OCKS0	Refer to Table 4		L

Table 2. S1 setting

Mode	DIF2	DUF1	DIF0	SDTO	Default
4	H	L	L	24bit, Left justified	Default
5		L	H	24bit, I ² S	

Table 3. Audio Data Format setting

OCKS1	OCKS0	MCKO1	fs (max.)	Default
L	L	256fs	96kHz	Default
H	L	512fs	48kHz	
H	H	128fs	192kHz	

Table 4. MCKO clock setting

■ **Setting of SW1 and SW2 switch**

[SW1](SMUTE): Don’t use. SW1 must be always “L”.

[SW2](PDN): Reset of AK4118. Keep “H” during normal operation.

■ **Serial Control (I²C-bus Control Mode)**

The AK4426 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT1 (CTRL) with PC by 10 wire flat cable packed with the AKD4426-SA

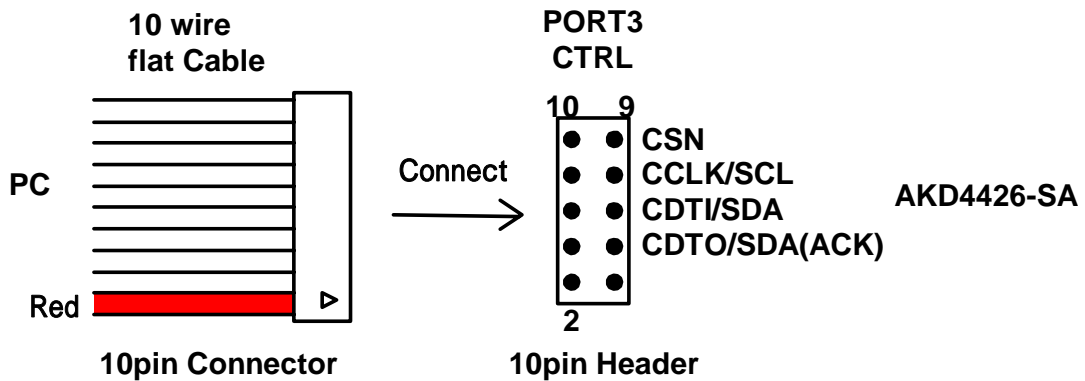


Figure 3. Connect of 10 wire flat cable

■ Analog Output Circuit

AOUTL and AOUTR pins are outputted from J1 (LOUT) and J2 (ROUT).

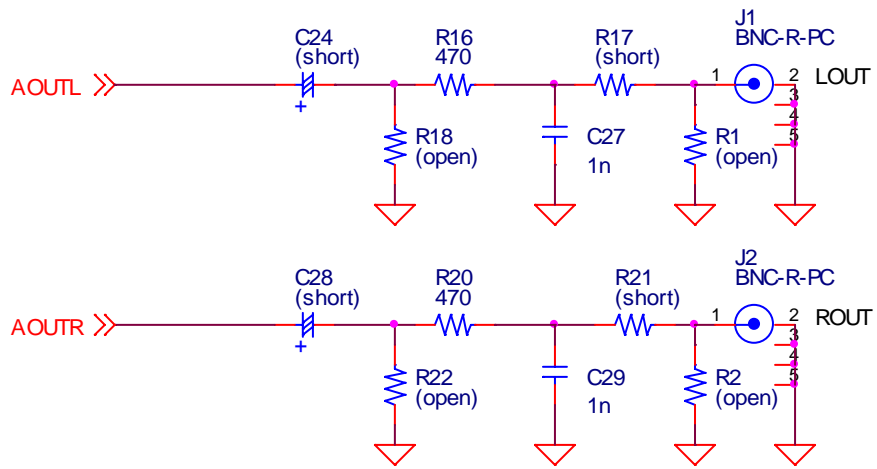


Figure 4. AOUTL / AOUTR Output Circuit

* AKM assumes no responsibility for the trouble when using the above circuit examples.

Control Soft Manual

■ Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect the evaluation board to an IBM PC/AT compatible PC by a 10wire flat cable. Be aware of the direction of the 10pin header. When running this control soft on the Windows 2000/XP, the driver which is included in the CD must be installed. Refer to the “Driver Control Install Manual for AKM Device Control Software” for installing the driver. When running this control soft on the windows 95/98/ME, driver installing is not necessary. This control soft does not support the Windows NT.
3. Proceed evaluation by following the process below.

■ Operation Screen

1. Start up the control program following the process above.

The operation screen is shown below.

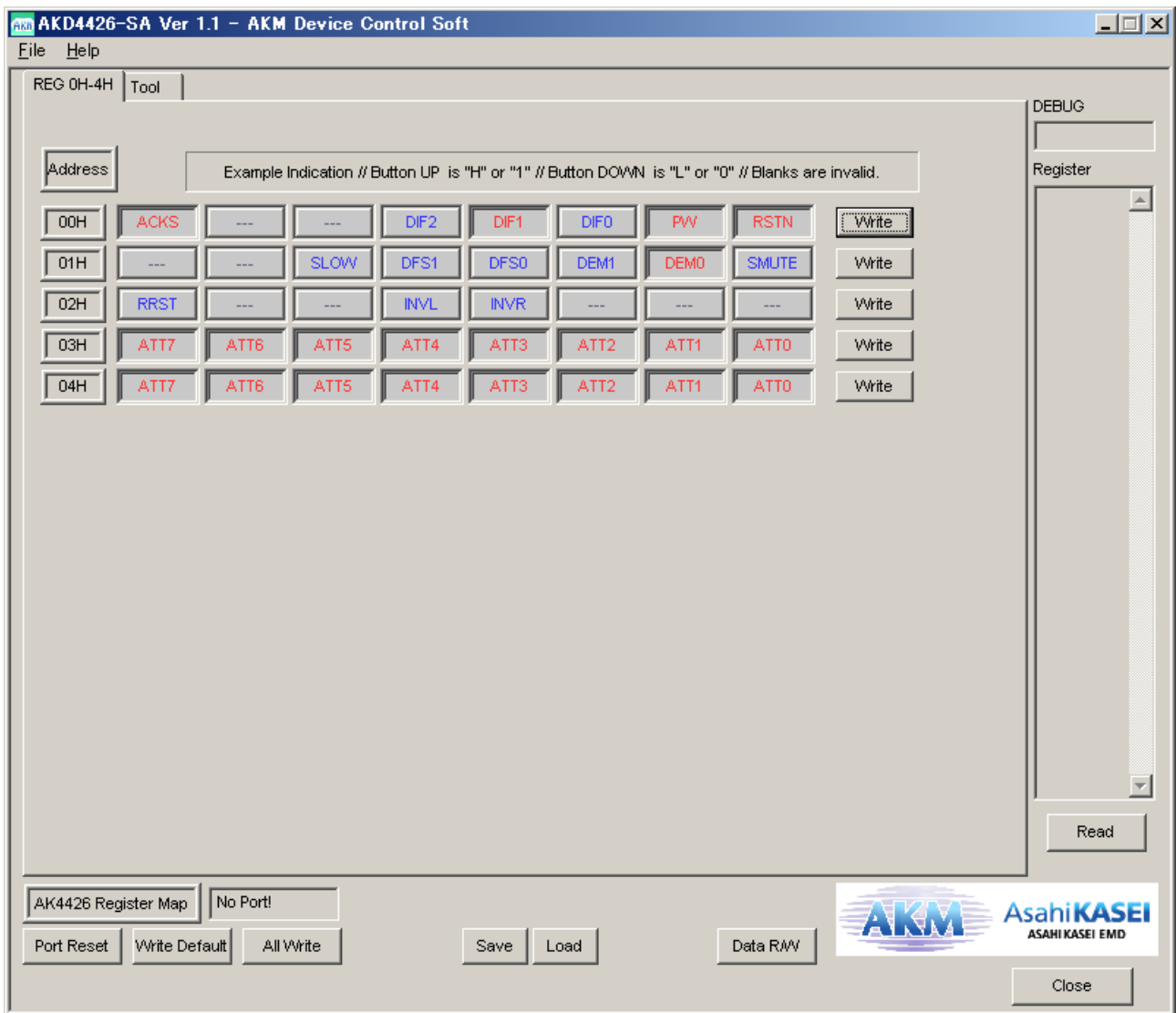


Figure 5. Window of [FUNCTION]

■ Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: For when connecting to USB I/F board (AKDUSBIF-A)
Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-A).
2. [Write Default]: Register Initializing
When the device is reset by a hardware reset, use this button to initialize the registers.
3. [All Write]: Executing write commands for all registers displayed.
4. [Save]: Saving current register settings to a file.
5. [Load]: Executing data write from a saved file.
6. [Data R/W]: “Data R/W” dialog box is popped up.

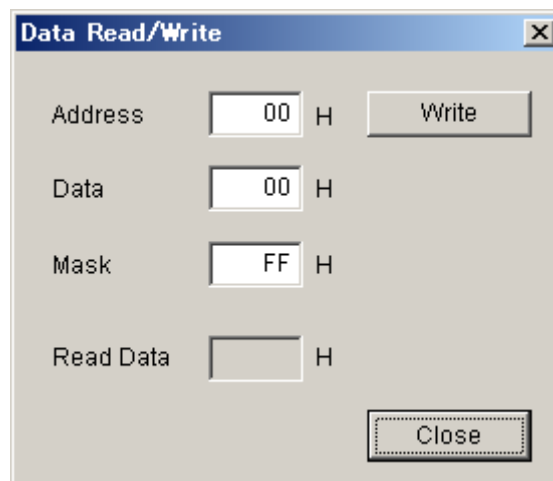


Figure 6. Window of [Data R/W]

2. [REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.

Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).

Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Grayout registers are Read Only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.

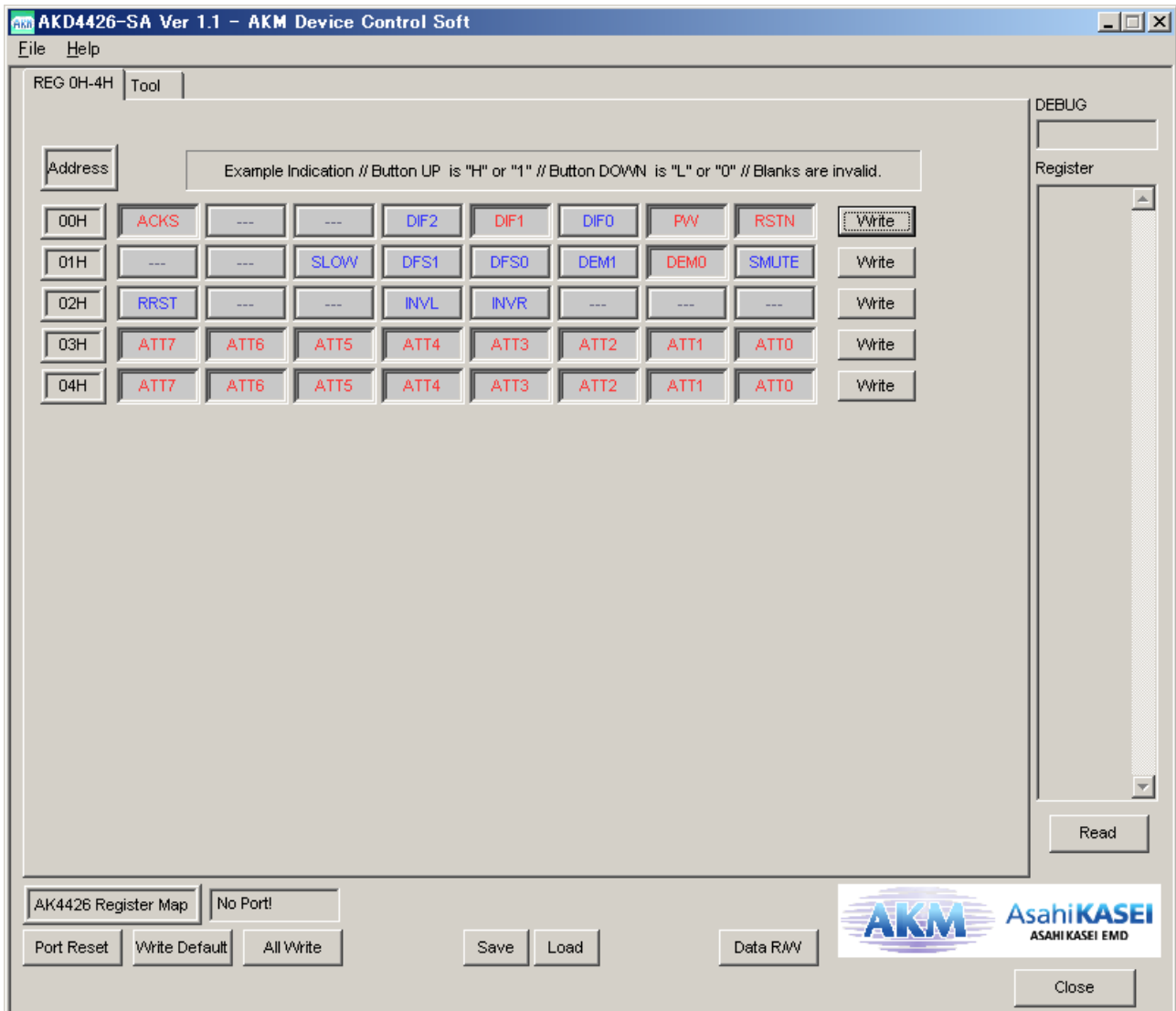


Figure 7. Window of [REG]

[Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.
When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or ”0”.
Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.

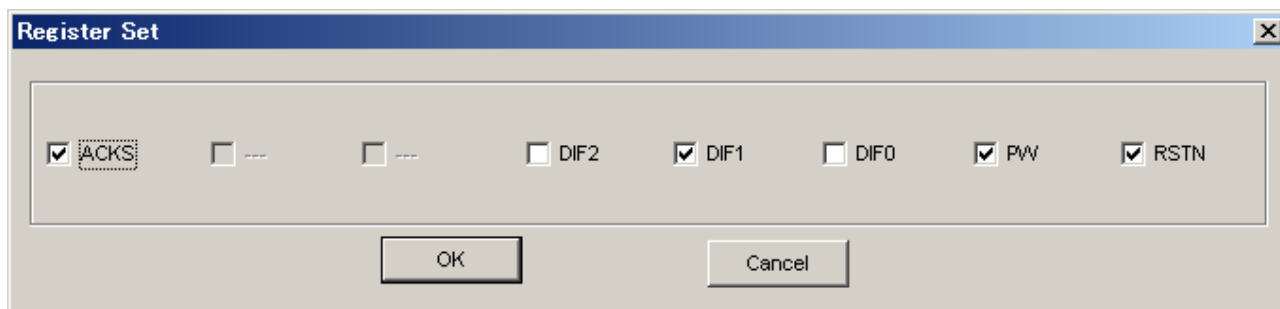


Figure 8. Window of [Register Set]

3. [Tool]: Testing Tools

This tab screen is for evaluation testing tool.
Click buttons for each testing tool.

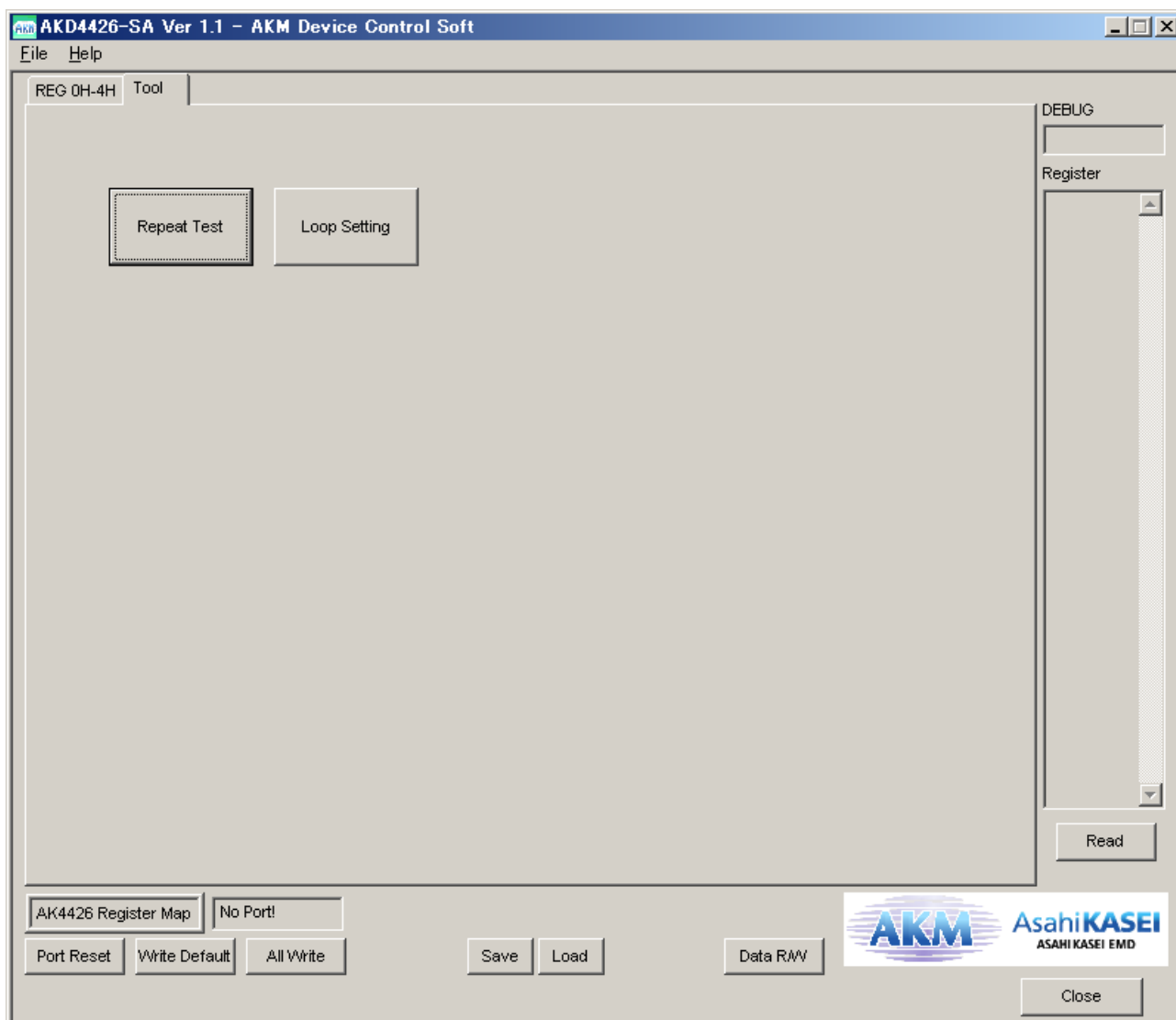
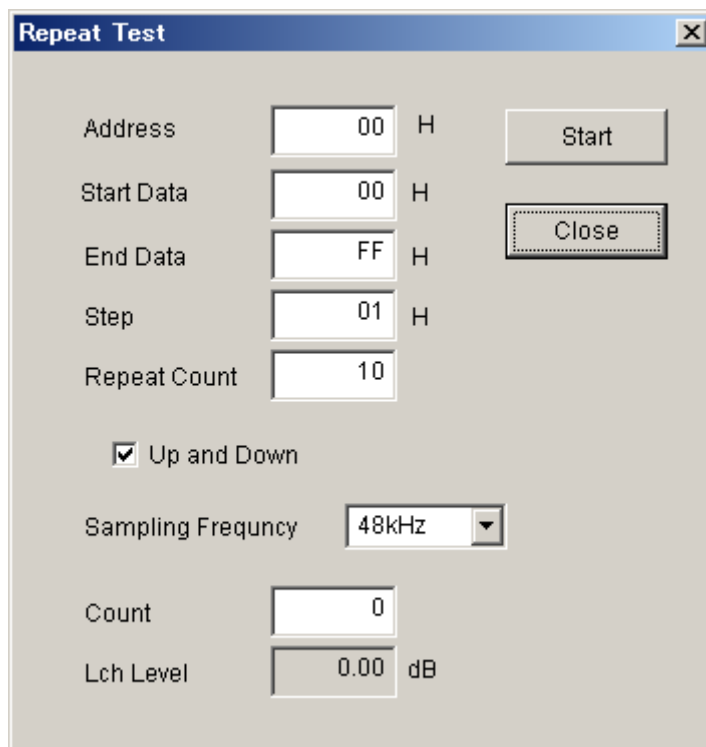


Figure 9. Window of [Tool]

■ Dialog Boxes

1. [All Req Write]: All Req Write dialog box

Click [All Reg Write] button in the main window to open register setting files.
Register setting files saved by [SAVE] button can be applied.



The 'Repeat Test' dialog box contains the following fields and controls:

- Address: 00 H
- Start Data: 00 H
- End Data: FF H
- Step: 01 H
- Repeat Count: 10
- Up and Down
- Sampling Frequency: 48kHz
- Count: 0
- Lch Level: 0.00 dB
- Start button
- Close button

Figure 10. Window of [Repeat Test]

2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.

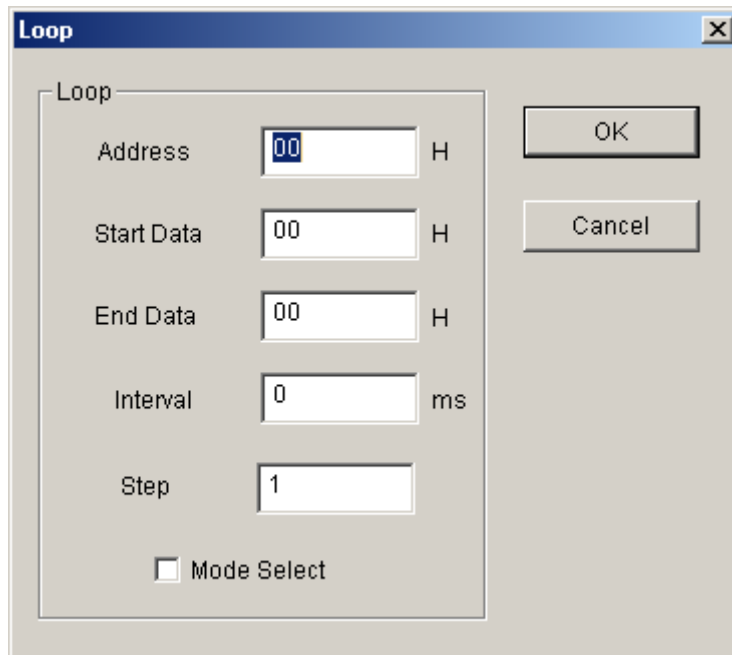


Figure 11. Window of [Loop]

Address Box: Input data address in hexadecimal numbers for data writing.

Data Box: Input data in hexadecimal numbers.

Mask Box: Input mask data in hexadecimal numbers.

This is “AND” processed input data.

[Write]: Writing to the address specified by “Address” box.

[Read]: Reading from the address specified by “Address” box.

The result will be shown in the Read Data Box in hexadecimal numbers.

[Close]: Closing the dialog box and finish the process.

Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.

Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision System two Cascade (AP2)
- MCLK : 512fs (fs = 44.1kHz), 256fs (fs = 96kHz), 128fs (fs = 192kHz)
- BICK : 64fs
- fs : 44.1kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : VDD=AVDD=5V
- Interface : DIR
- Temperature : Room

Table Data

fs=44.1kHz

Parameter	Input signal	Filter condition	Lch	Rch	Unit
S/(N+D)	1kHz, 0dB	20kLPF	91.8	91.6	dB
DR	1kHz, -60dB	20kHz SPCL, A-weighted	106.0	106.1	dB
S/N	"0" data	20kHz SPCL, A-weighted	106.3	106.4	dB

fs=96kHz

Parameter	Input signal	Filter condition	Lch	Rch	Unit
S/(N+D)	1kHz, 0dB	40kLPF	91.0	90.8	dB
DR	1kHz, -60dB	40kHz SPCL, A-weighted	106.0	106.1	dB
S/N	"0" data	40kHz SPCL, A-weighted	106.3	106.4	dB

fs=192kHz

Parameter	Input signal	Filter condition	Lch	Rch	Unit
S/(N+D)	1kHz, 0dB	40kLPF	91.6	91.4	dB
DR	1kHz, -60dB	40kHz SPCL, A-weighted	106.1	106.2	dB
S/N	"0" data	40kHz SPCL, A-weighted	106.2	106.3	dB

Plot Data

(1) fs = 44.1kHz (MCLK=512fs)

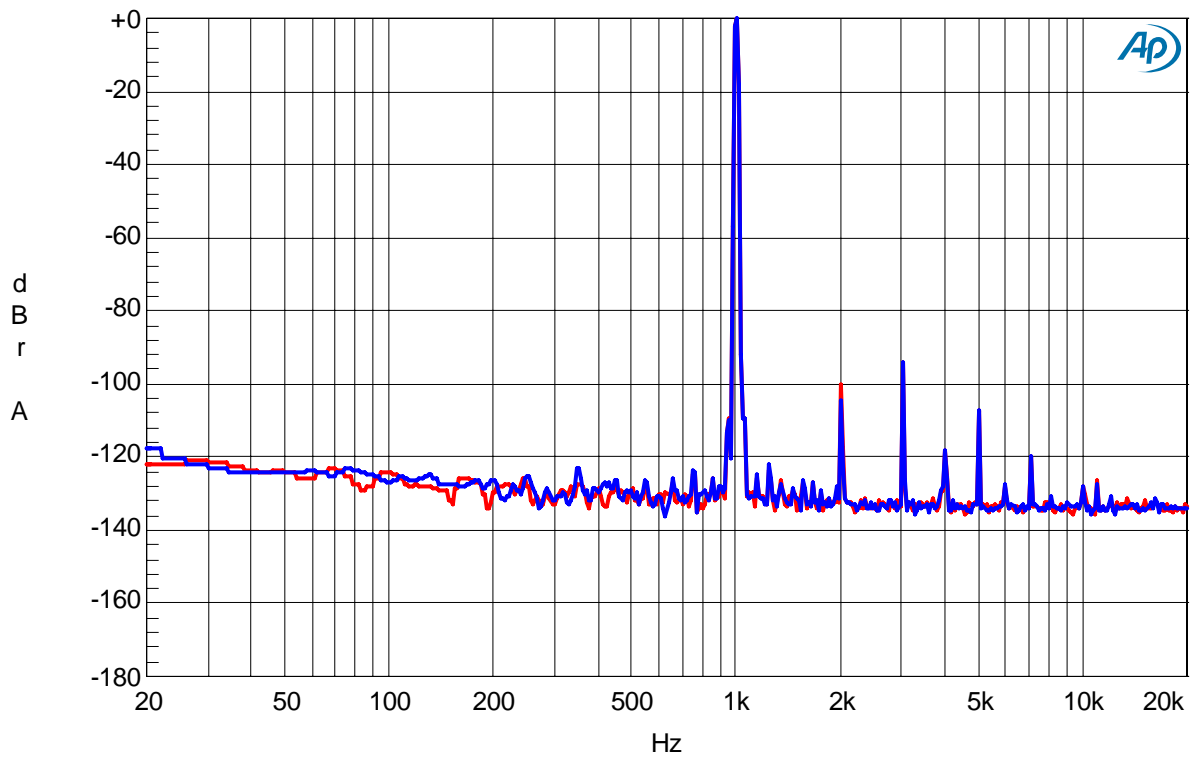


Figure 12. FFT (fin=1kHz, Input Level=0dBFS)

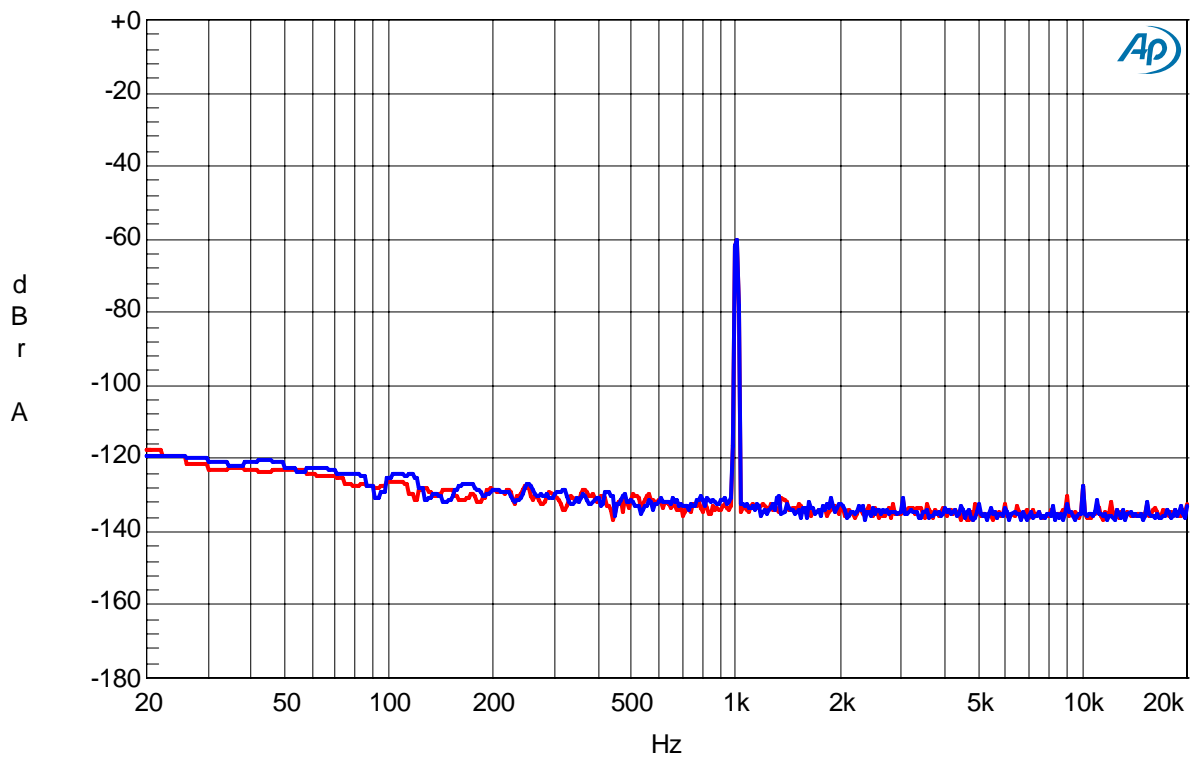


Figure 13. FFT (fin=1kHz, Input Level=-60dBFS)

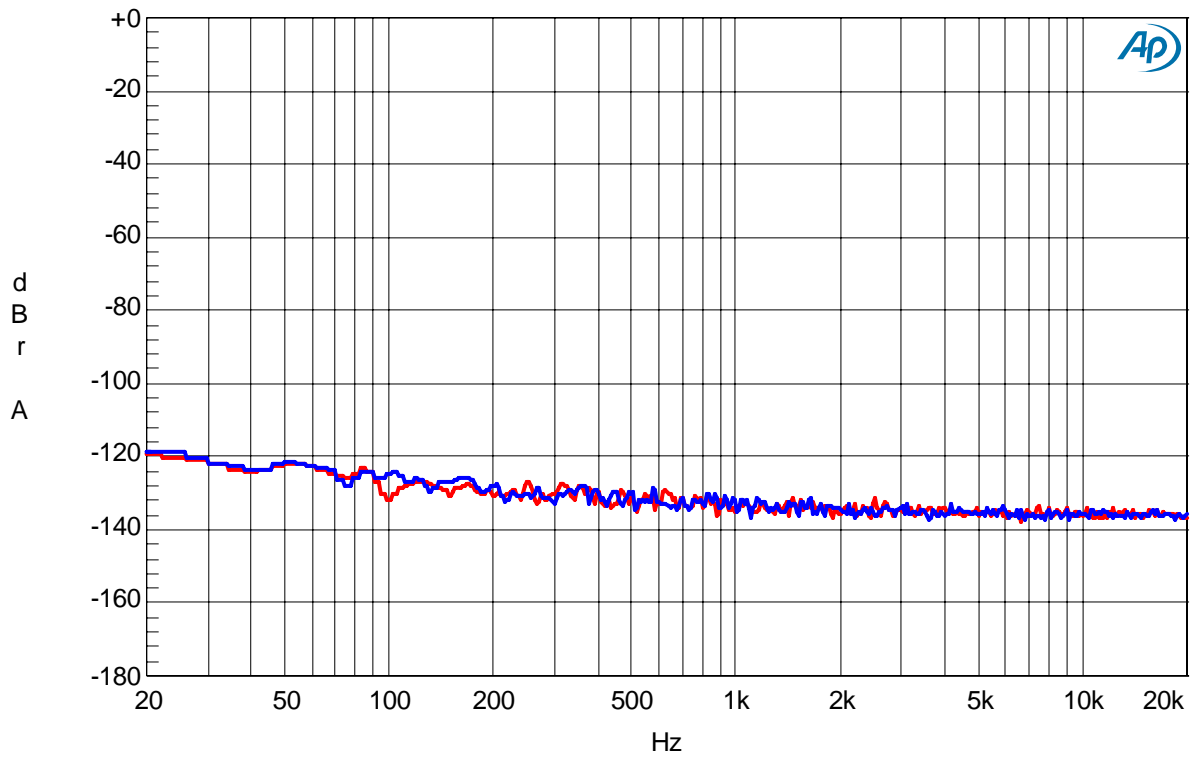


Figure 14. FFT (Noise Floor)

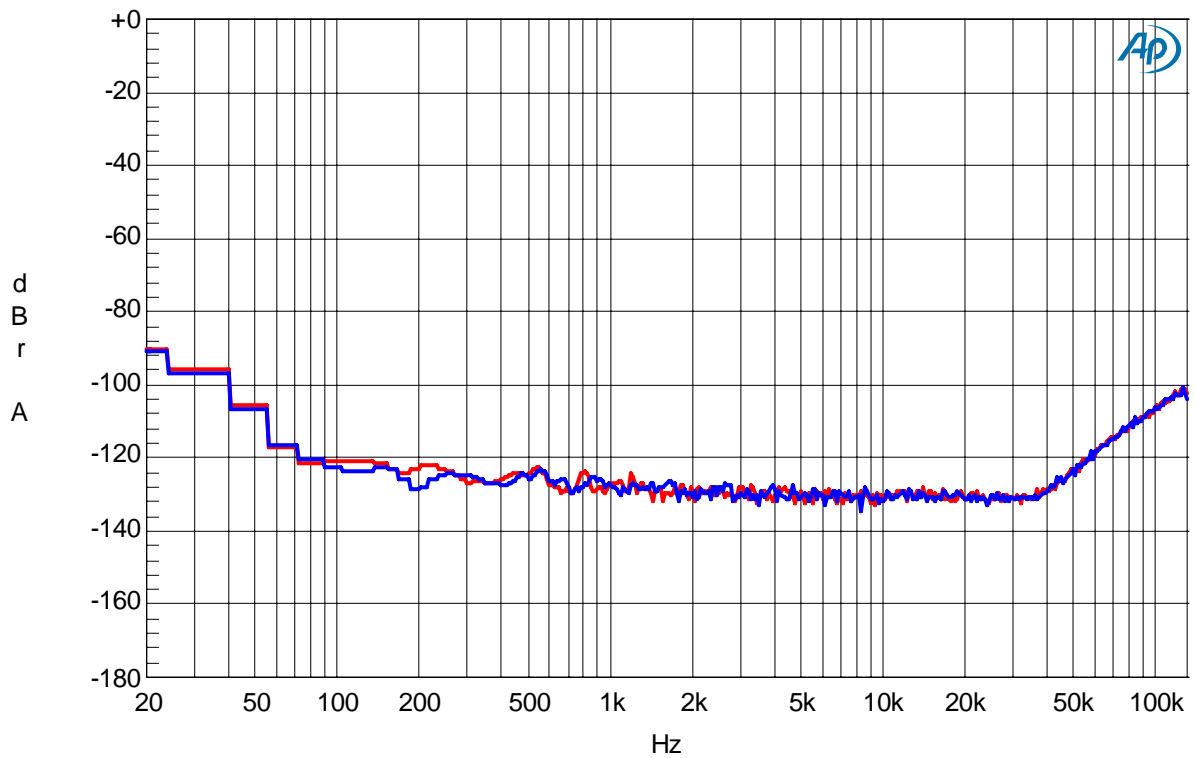


Figure 15. FFT (Out of band noise)

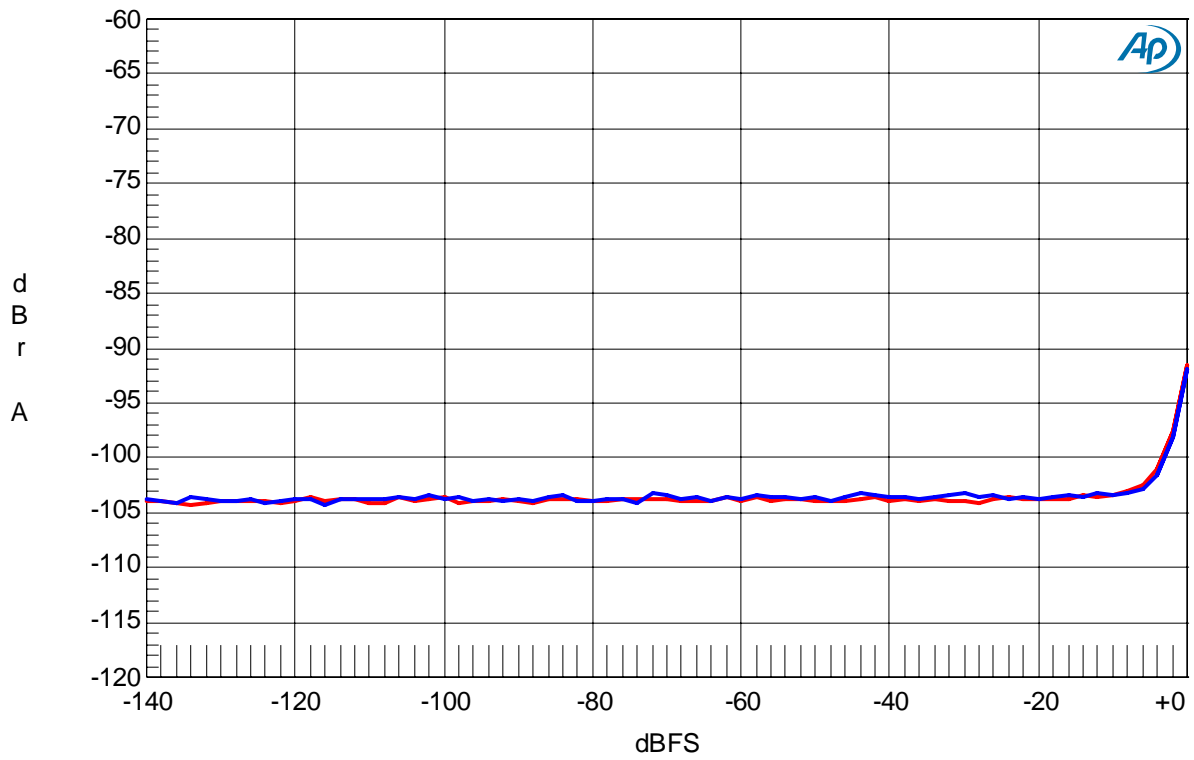


Figure 16. THD+N vs. Input level (fin=1kHz, 20kHz SPCL)

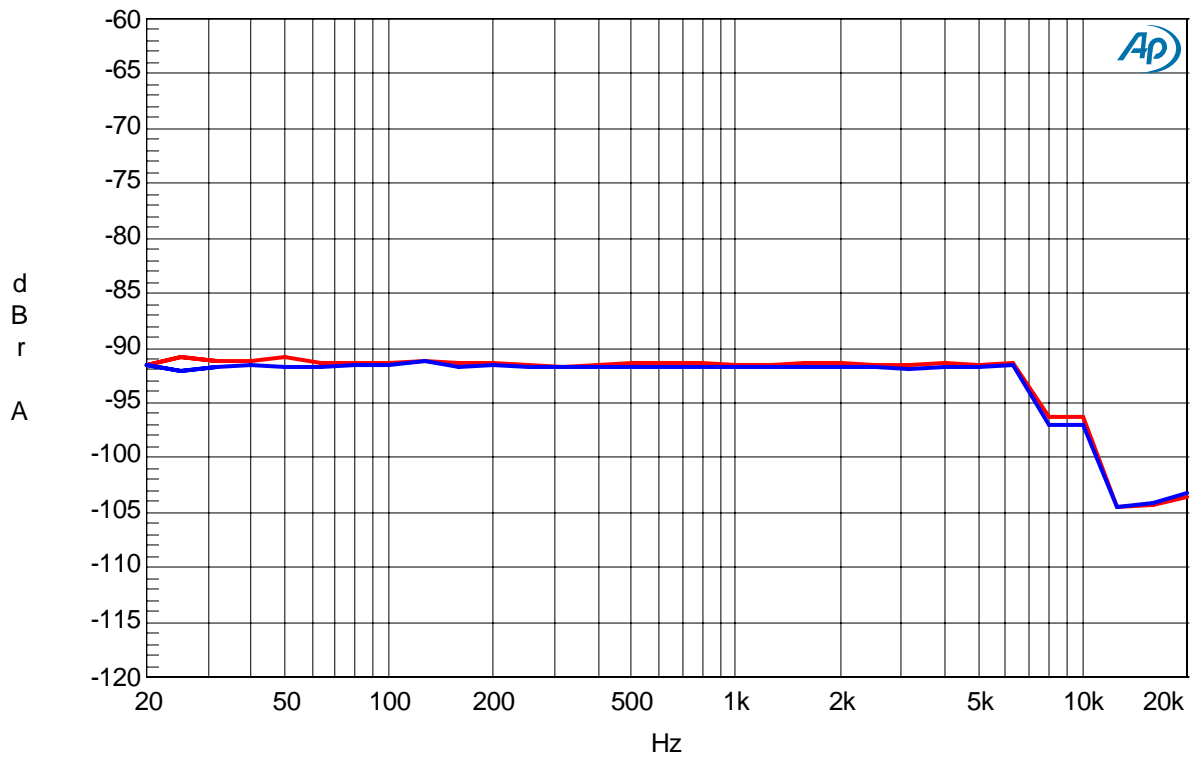


Figure 17. THD+N vs. Input Frequency (Input level=0dBFS, 20kHz SPCL)

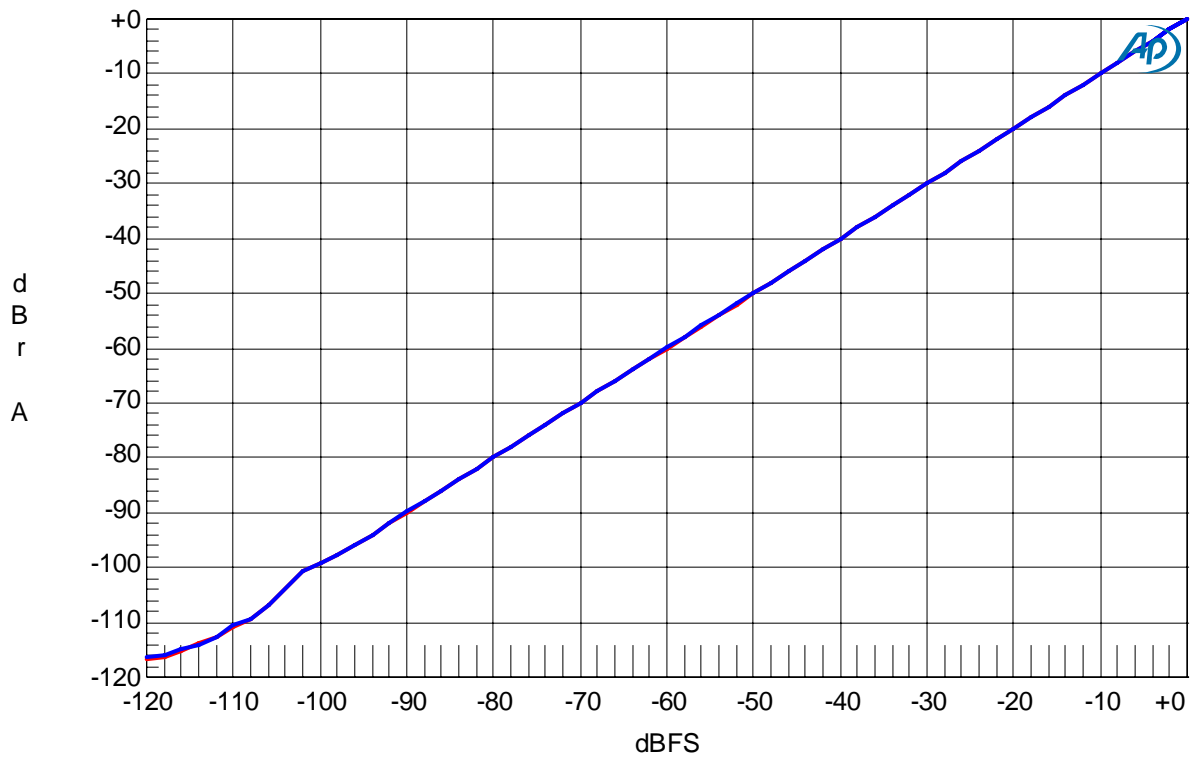


Figure 18. Linearity (fin=1kHz)

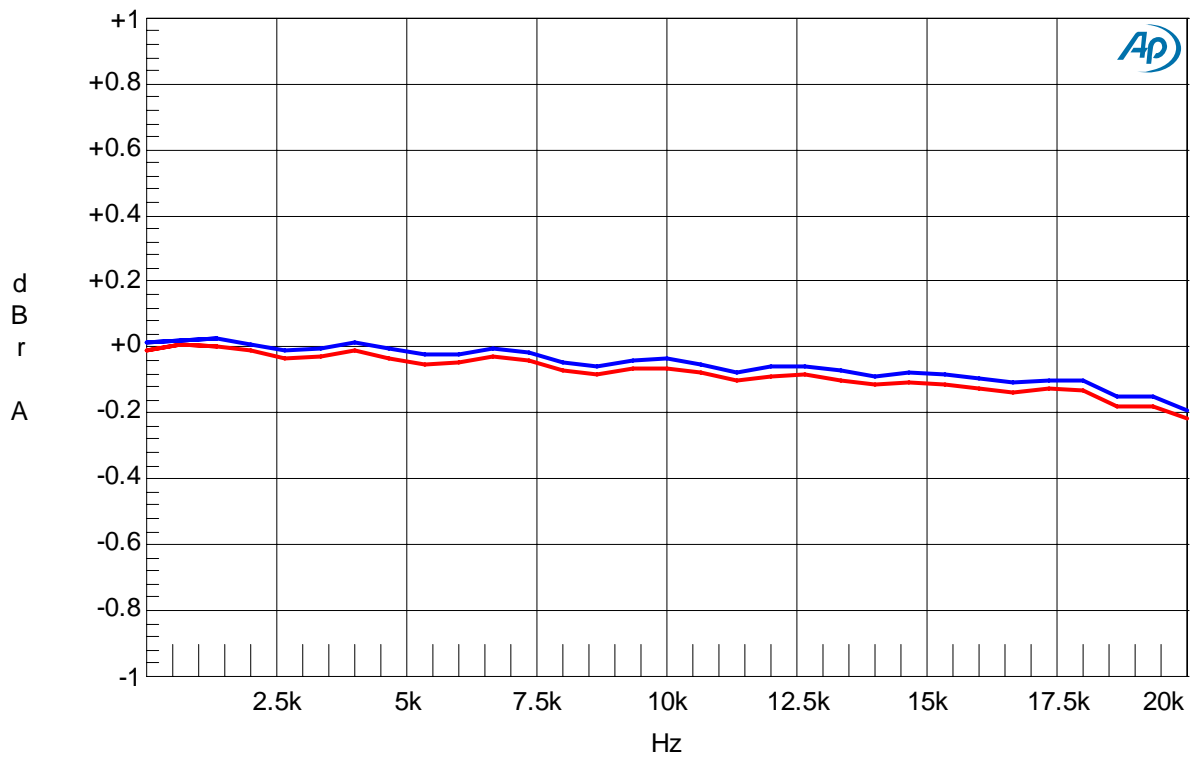


Figure 19. Frequency Response (Input level=0dBFS)

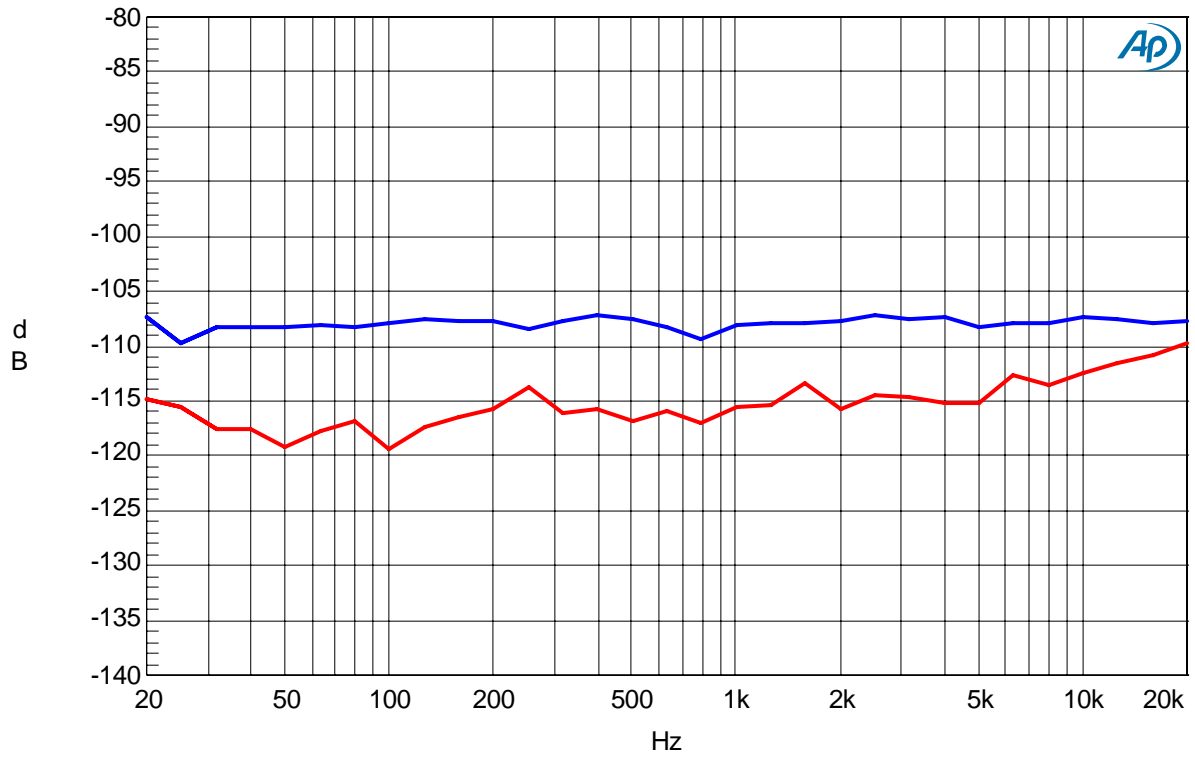


Figure 20. Crosstalk (Input level=0dBFS)
Red: Lch ← Rch, Blue: Rch ← Lch

(2) fs = 96kHz (MCLK=256fs)

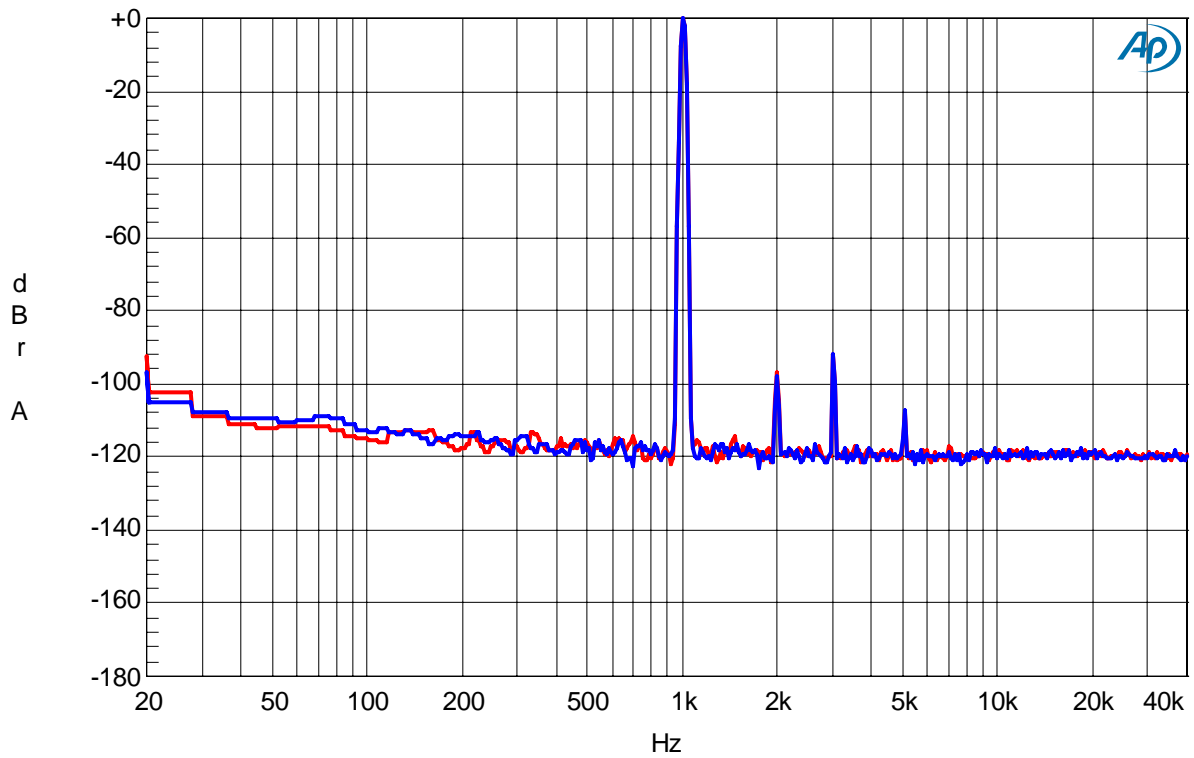


Figure 21. FFT (fin=1kHz, Input Level=0dBFS)

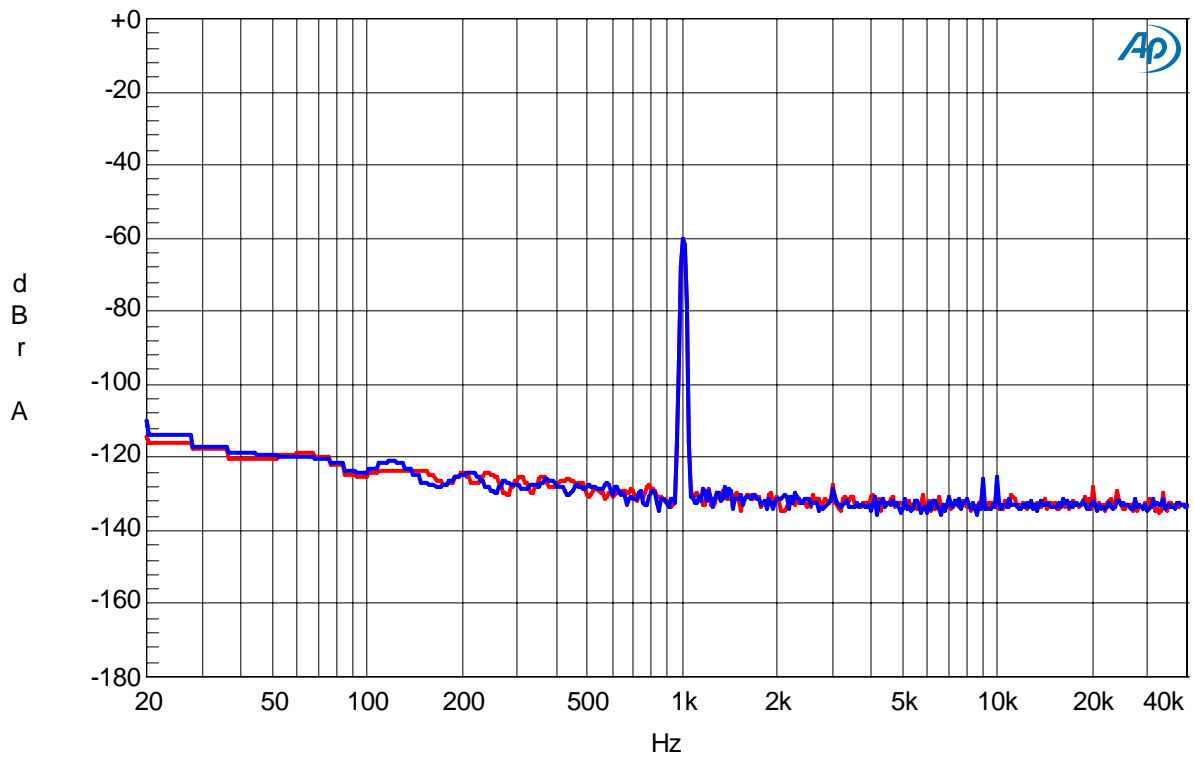


Figure 22. FFT (fin=1kHz, Input Level=-60dBFS)

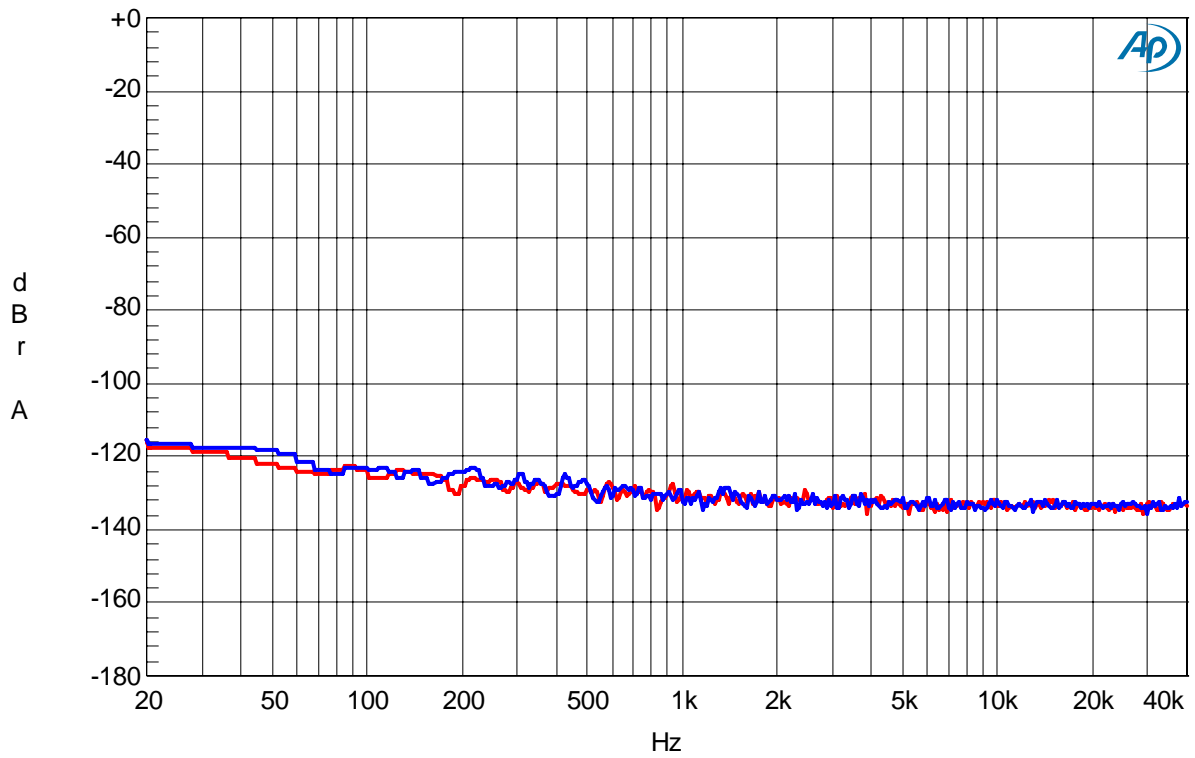


Figure 23. FFT (Noise Floor)

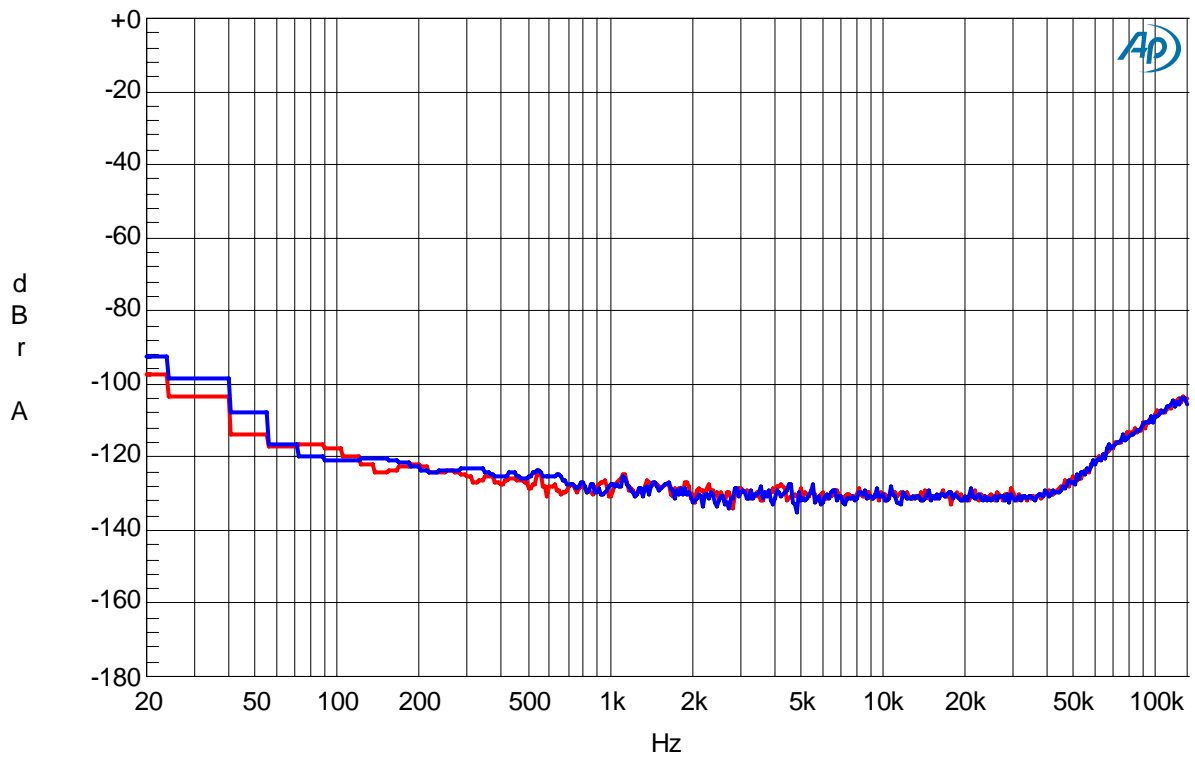


Figure 24. FFT (Out of band noise)

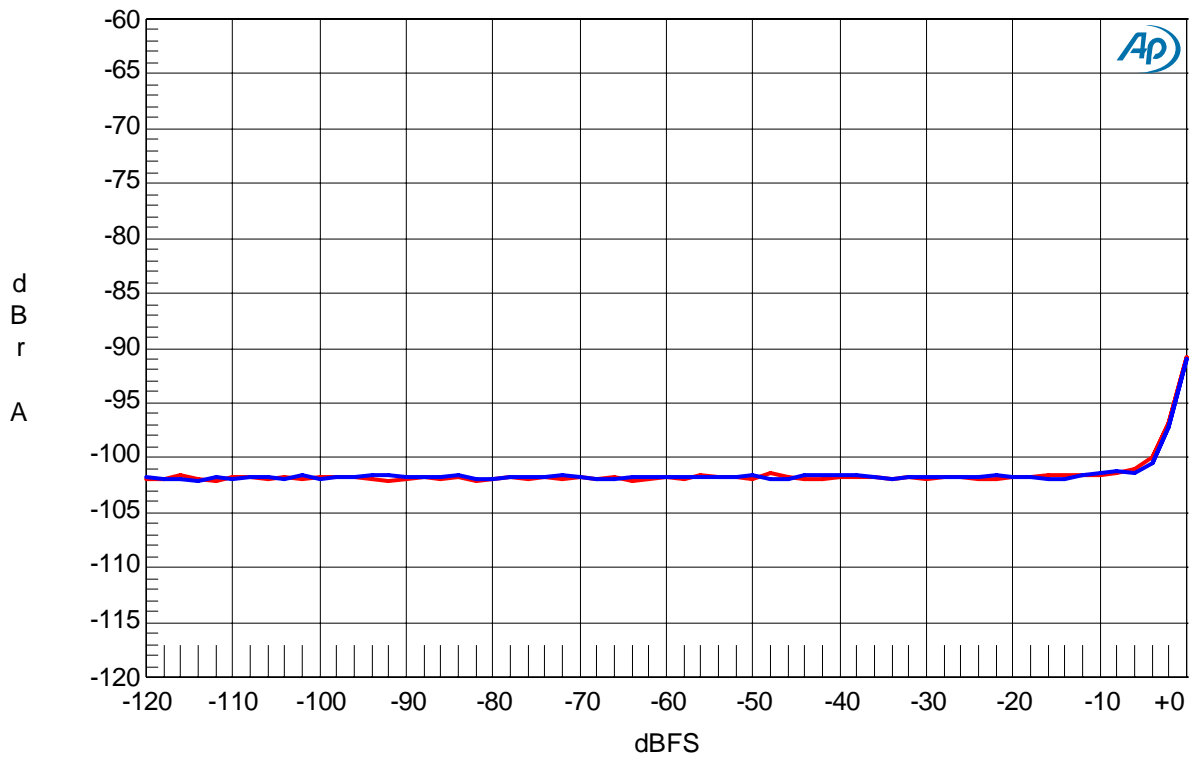


Figure 25. THD+N vs. Input level (fin=1kHz, 40kHz SPCL)

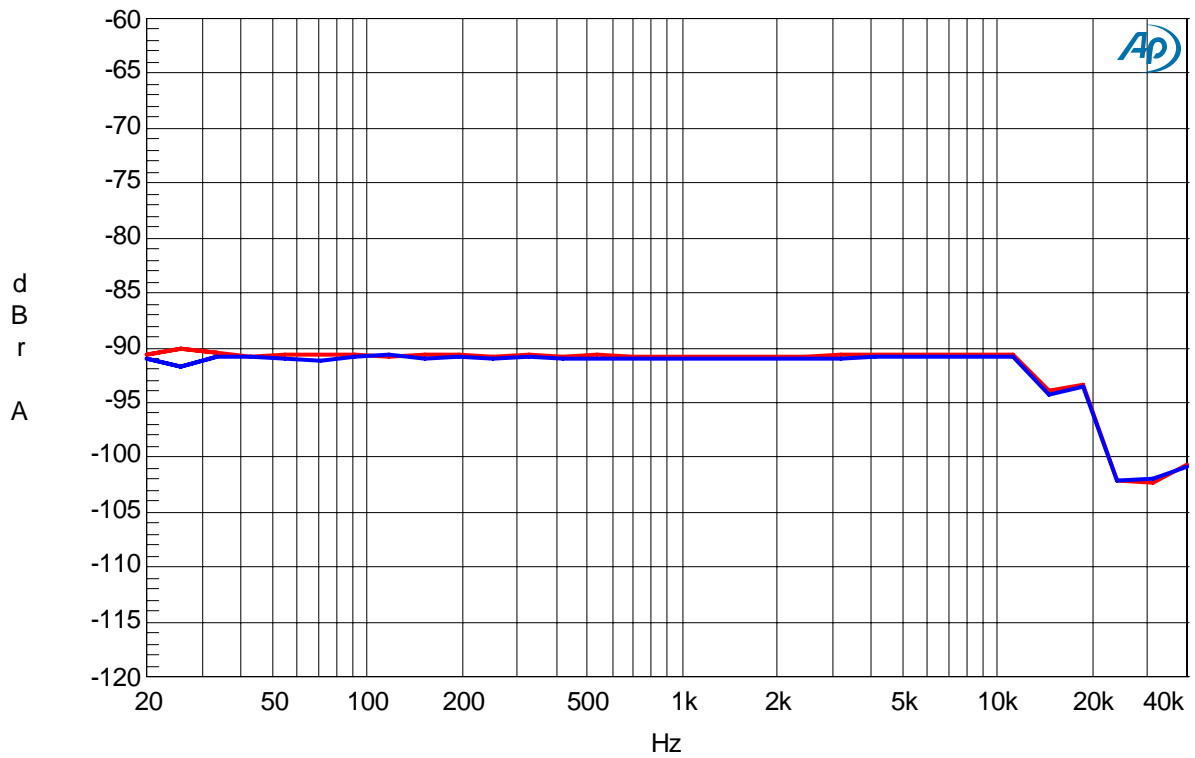


Figure 26. THD+N vs. Input Frequency (Input level=0dBFS)

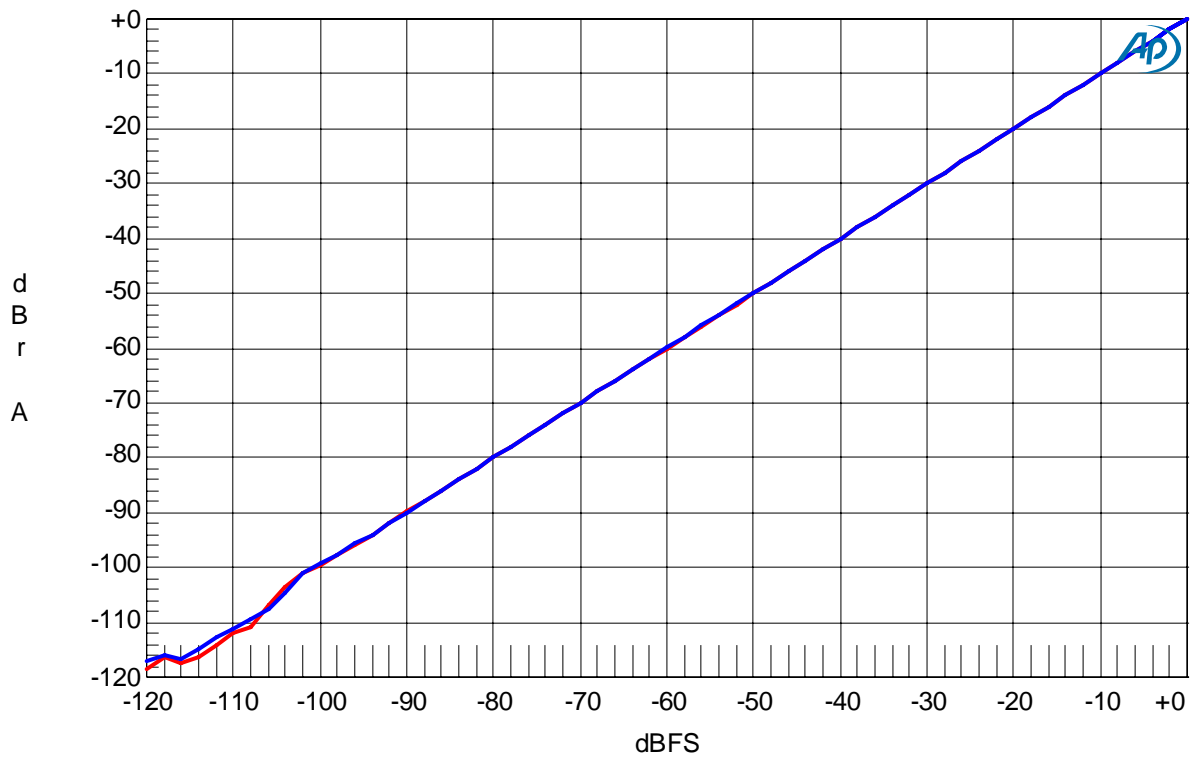


Figure 27 Linearity (f_{in}=1kHz)

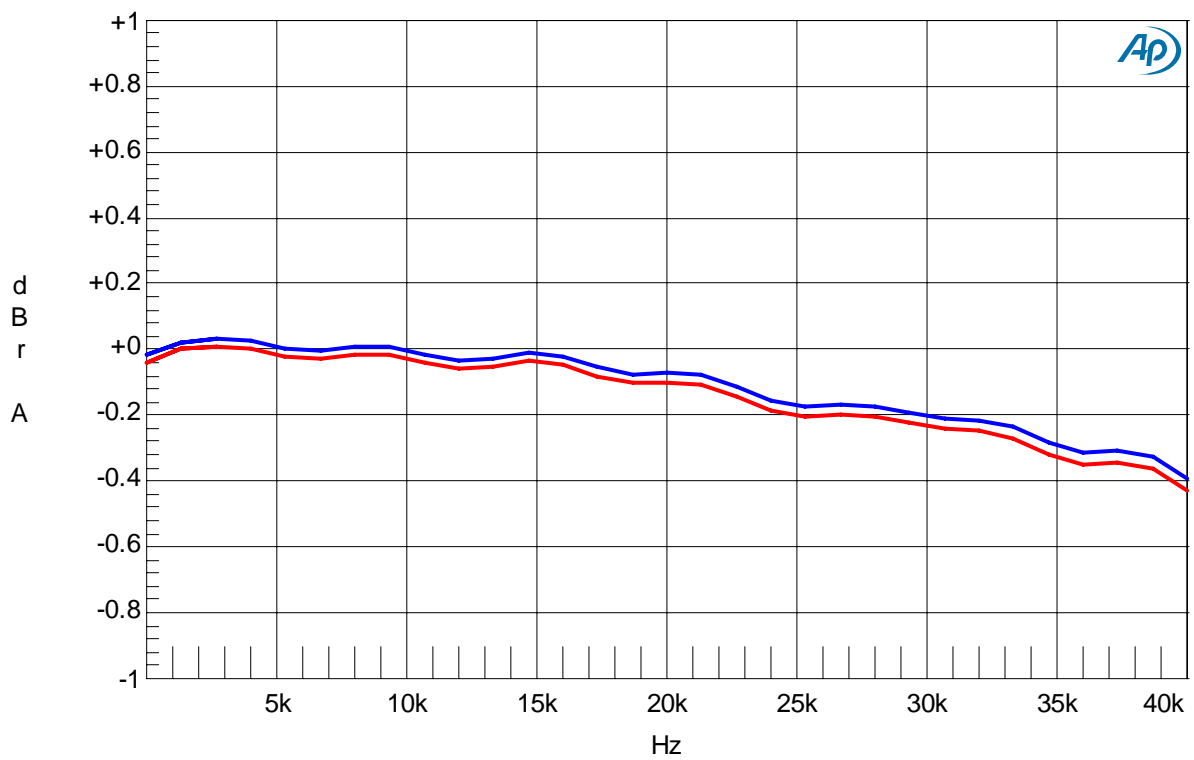


Figure 28. Frequency Response (Input level=0dBFS)

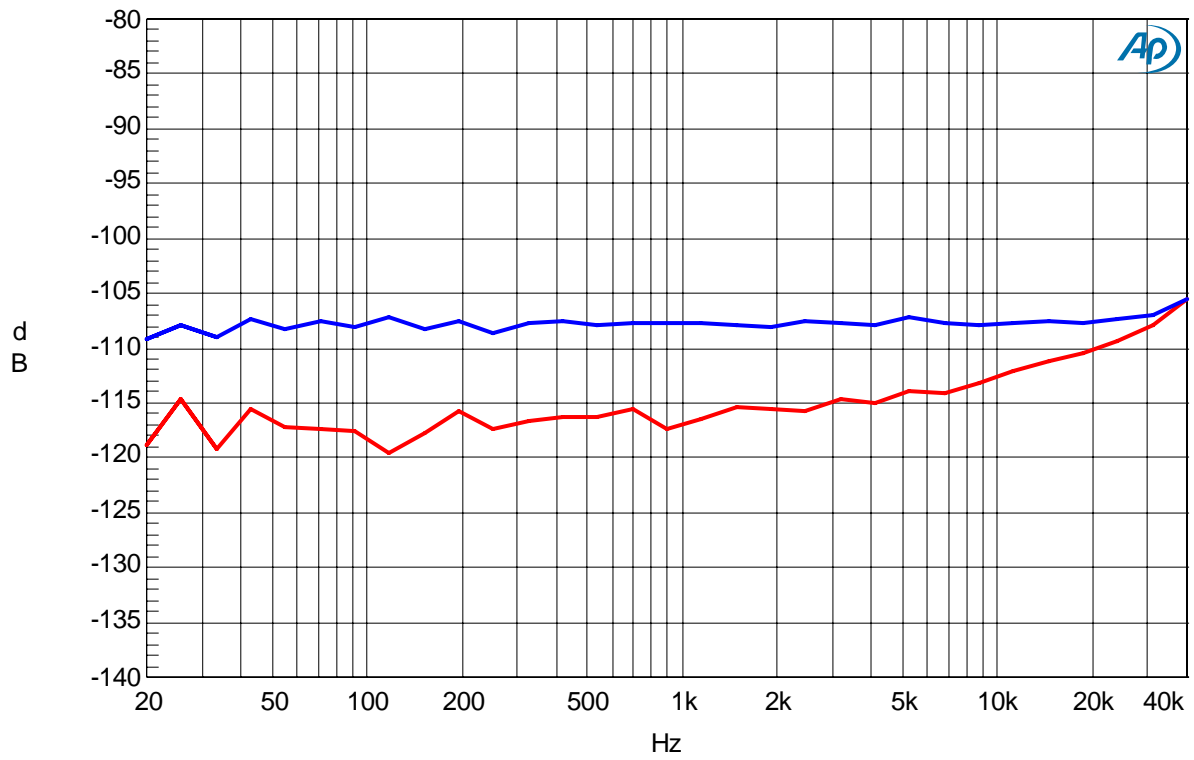


Figure 29. Crosstalk (Input level=0dBFS)
Red: Lch ← Rch, Blue: Rch ← Lch

(3) fs = 192kHz (MCLK=128fs)

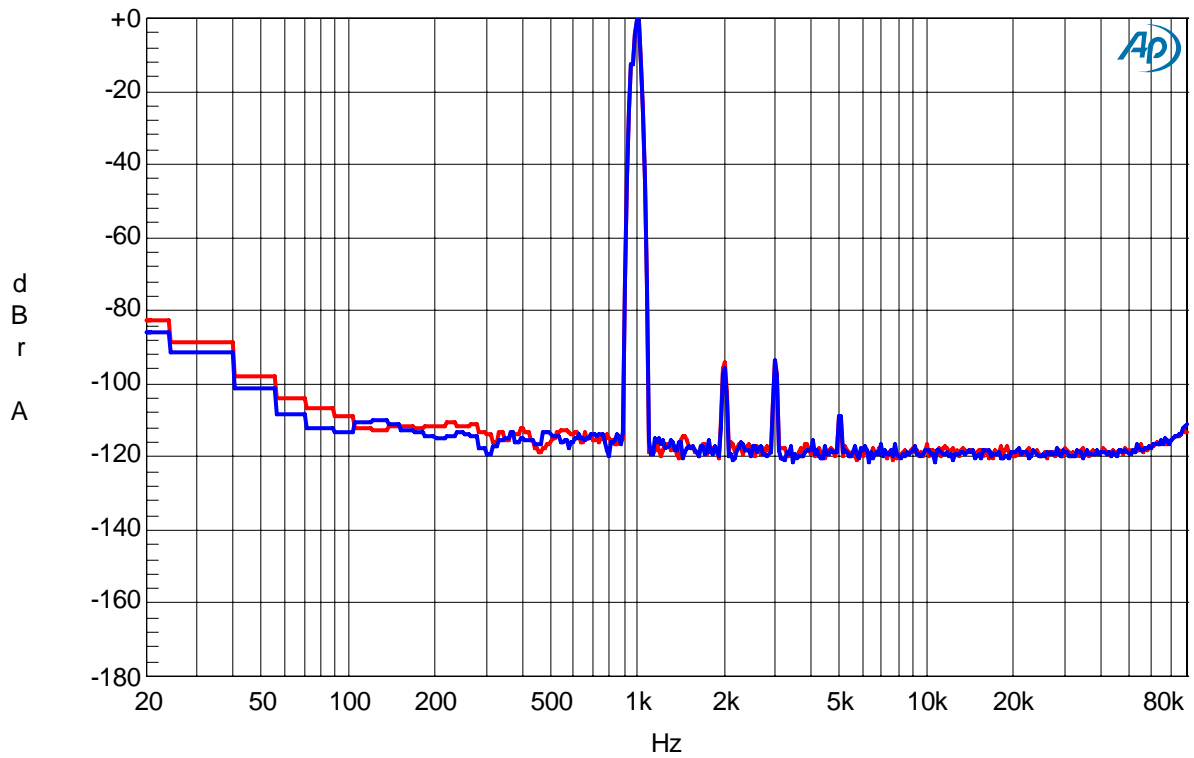


Figure 30. FFT (fin=1kHz, Input Level=0dBFS)

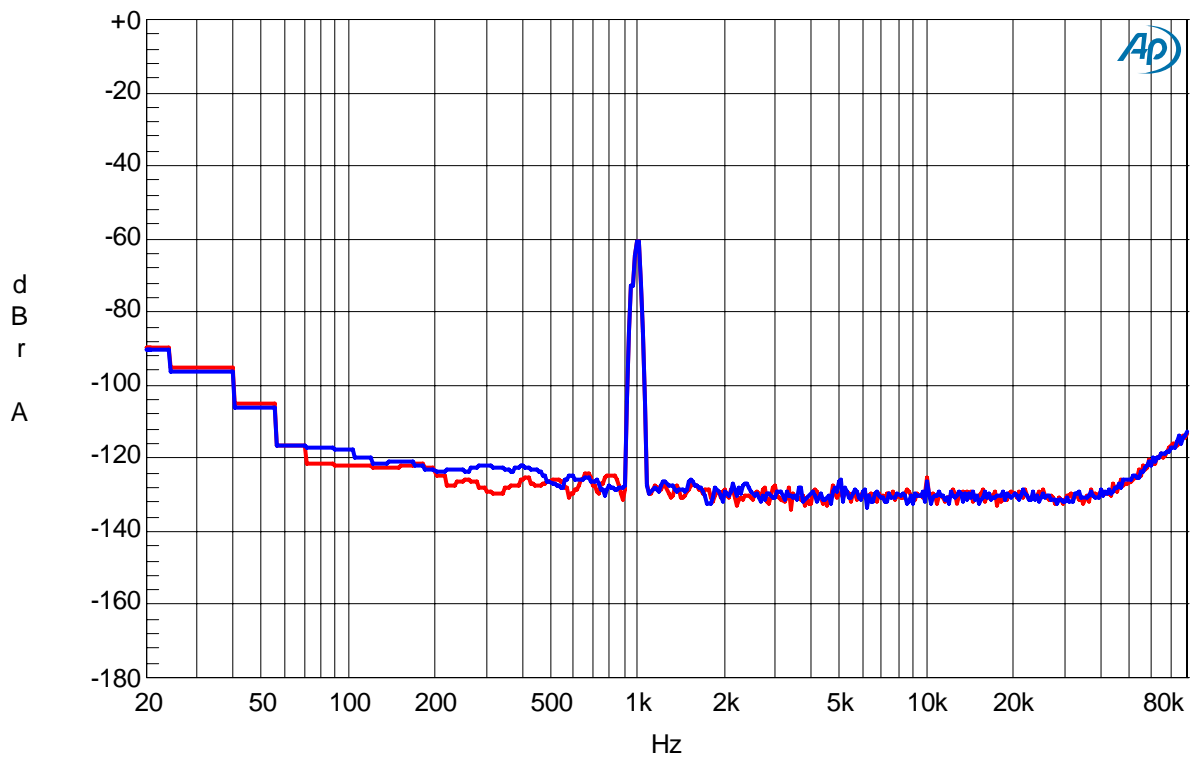


Figure 31. FFT (fin=1kHz, Input Level=-60dBFS)

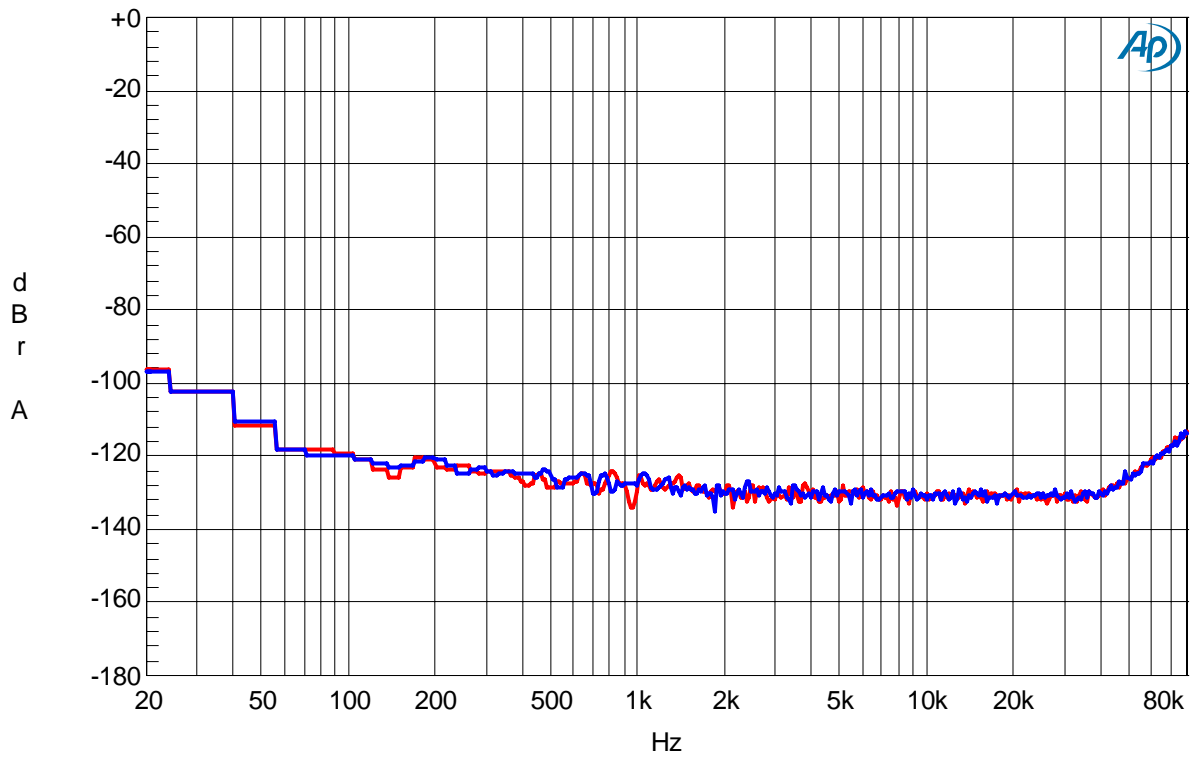


Figure 32. FFT (Noise Floor)

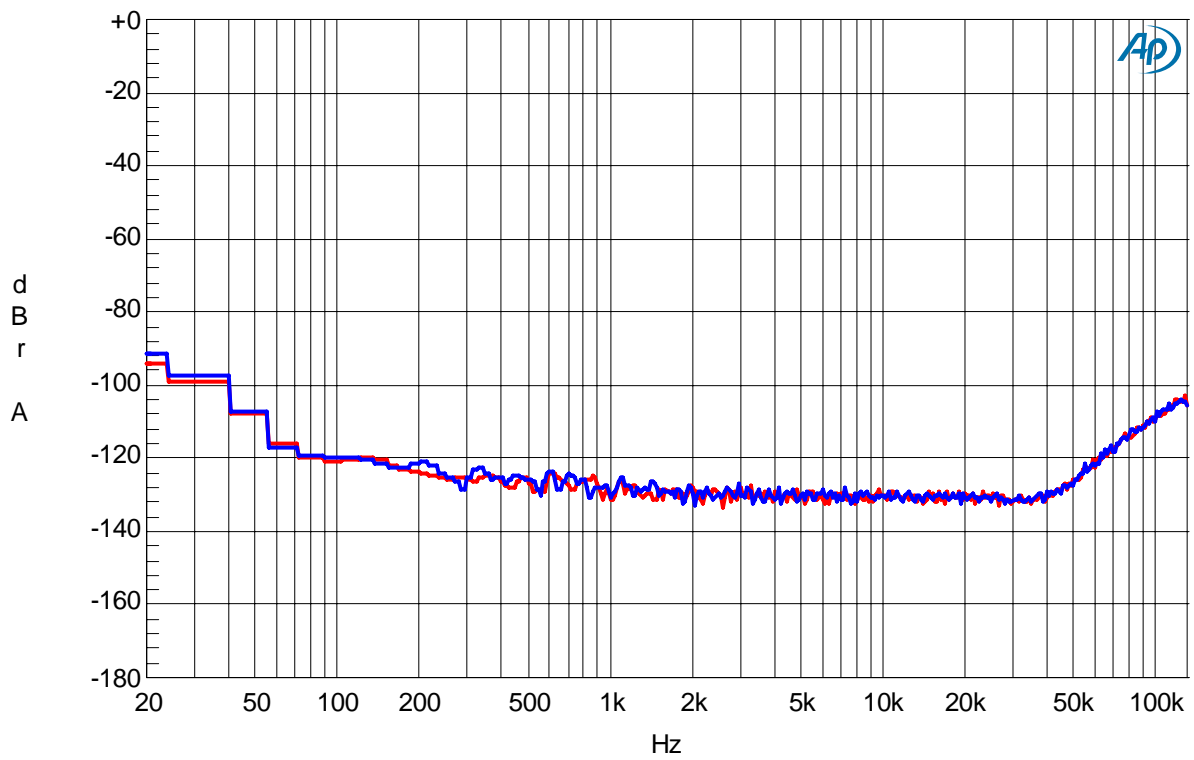


Figure 33. FFT (Out of band noise)

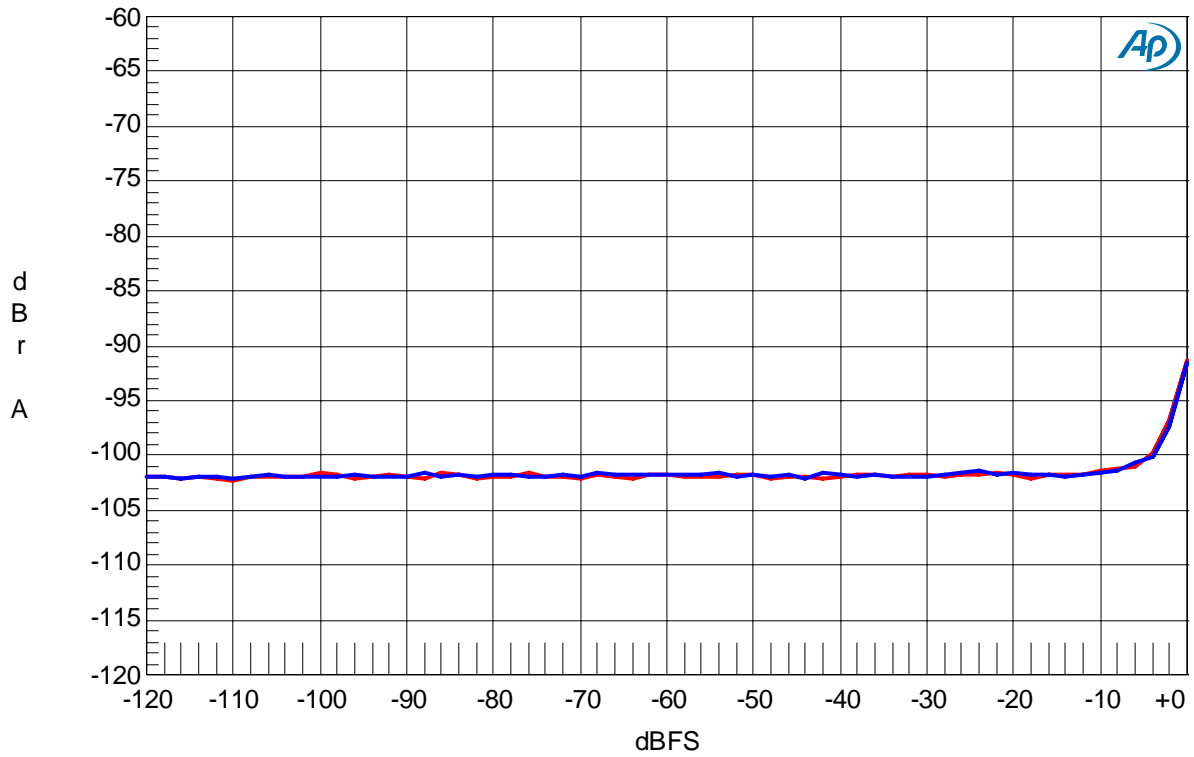


Figure 34. THD+N vs. Input level (fin=1kHz, 40kHz SPCL)

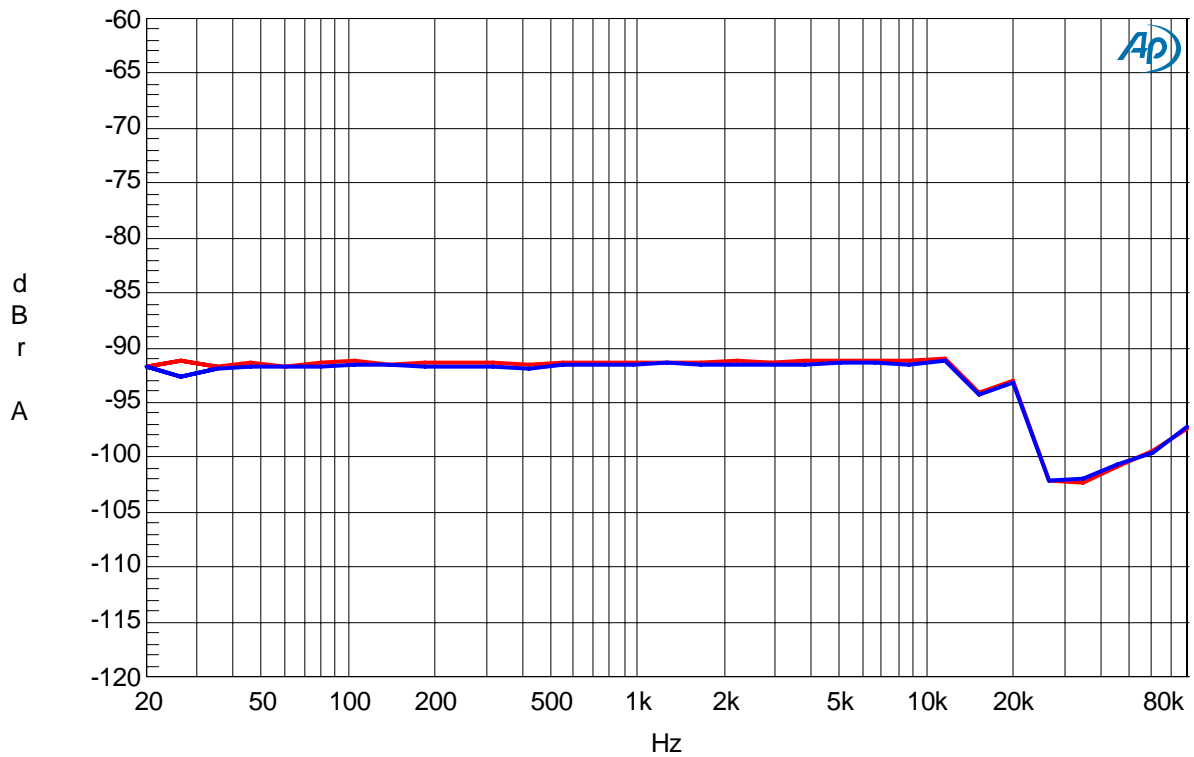


Figure 35. THD+N vs. Input Frequency (Input level=0dBFS)

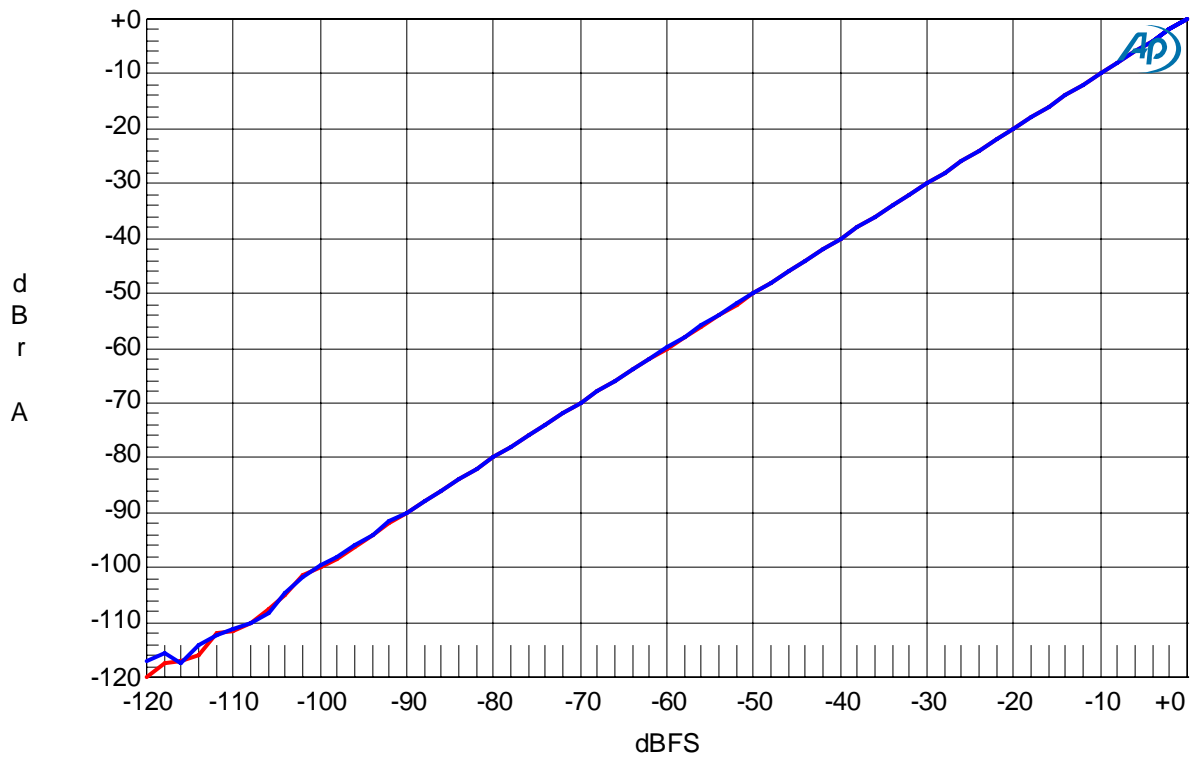


Figure 36. Linearity (f_{in}=1kHz)

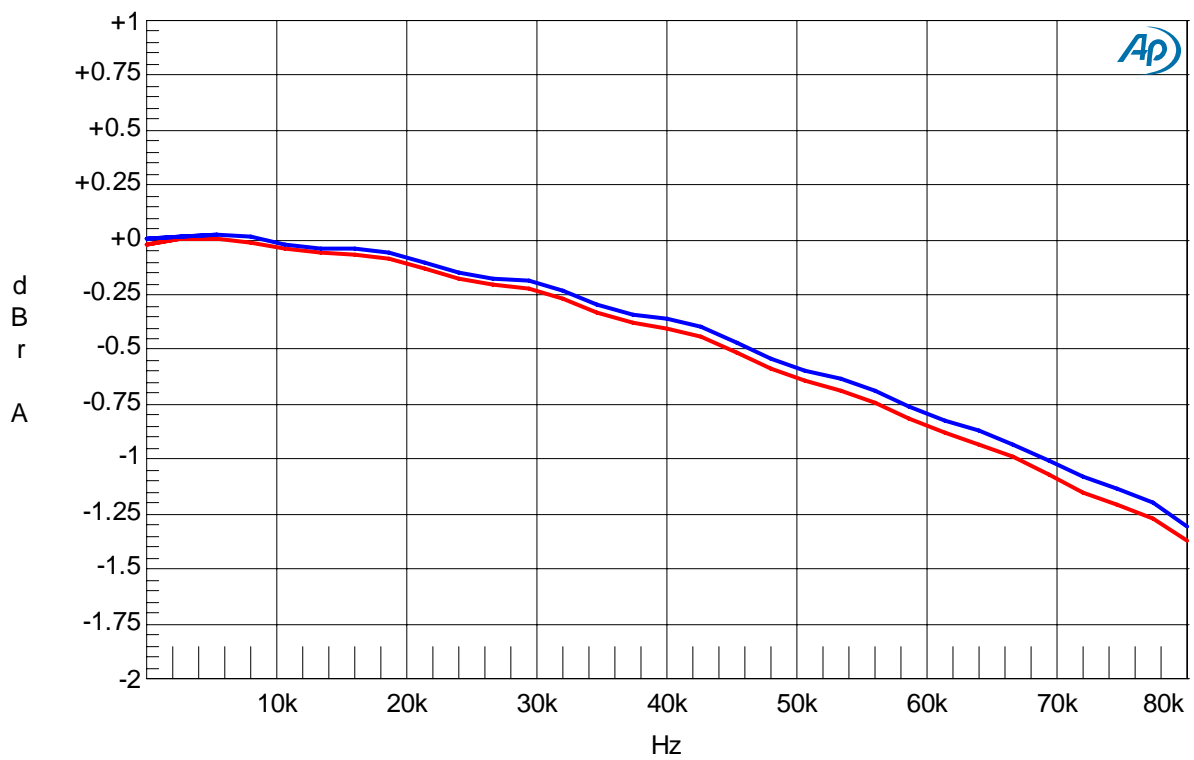


Figure 37. Frequency Response (Input level=0dBFS)

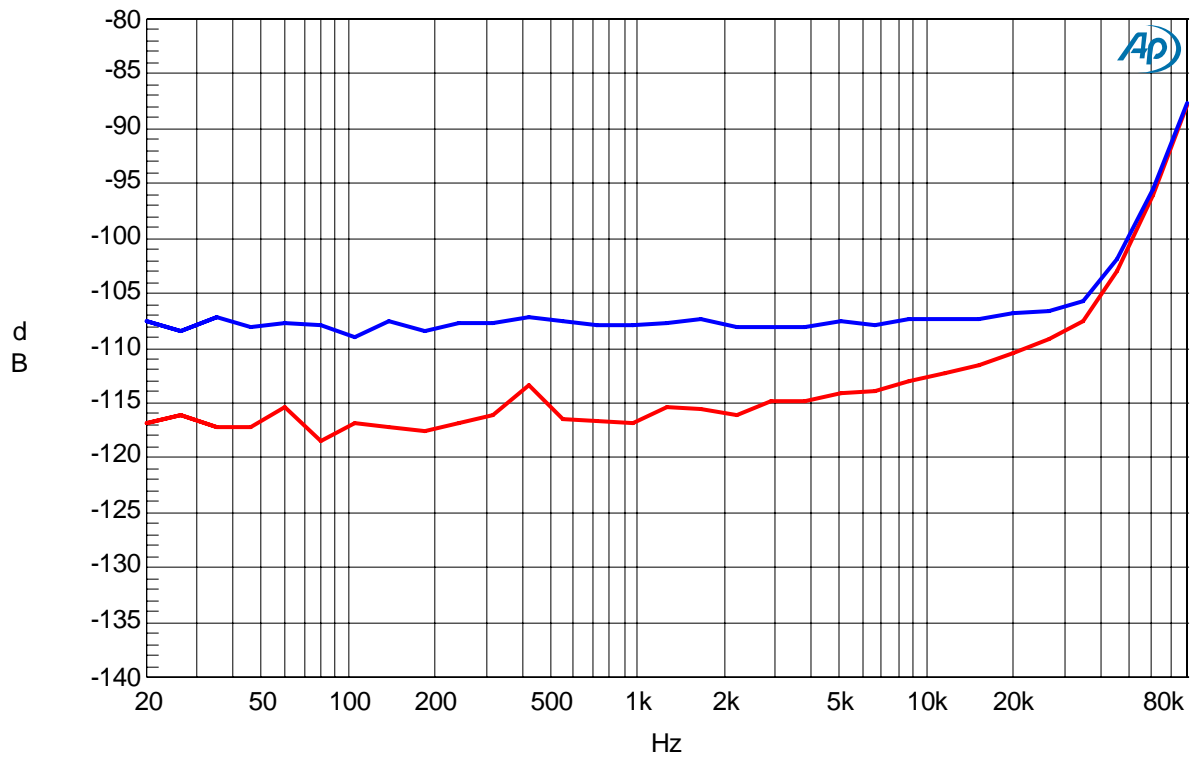


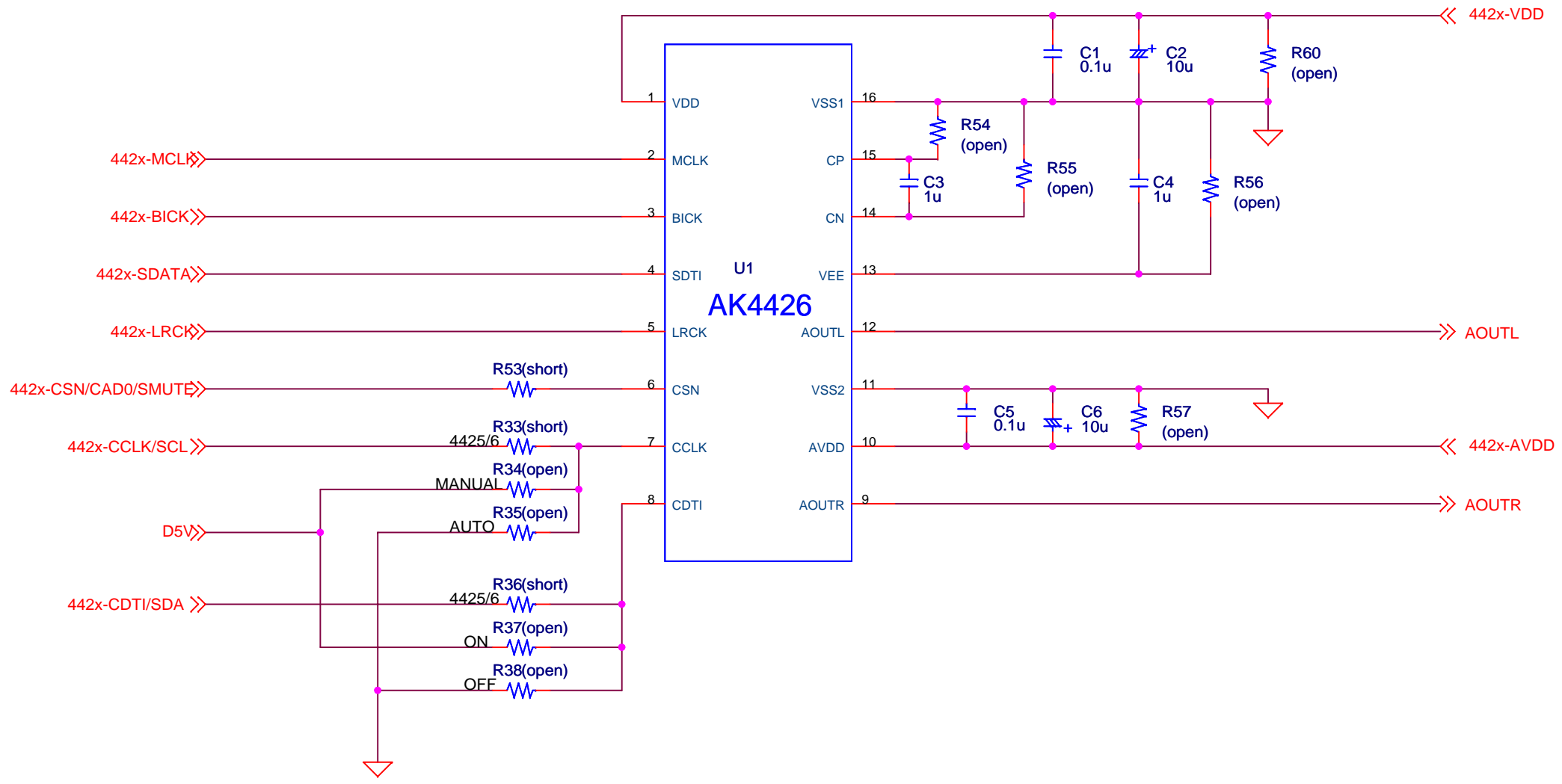
Figure 38. Crosstalk (Input level=0dBFS)
Red: Lch ← Rch, Blue: Rch ← Lch

REVISION HISTORY

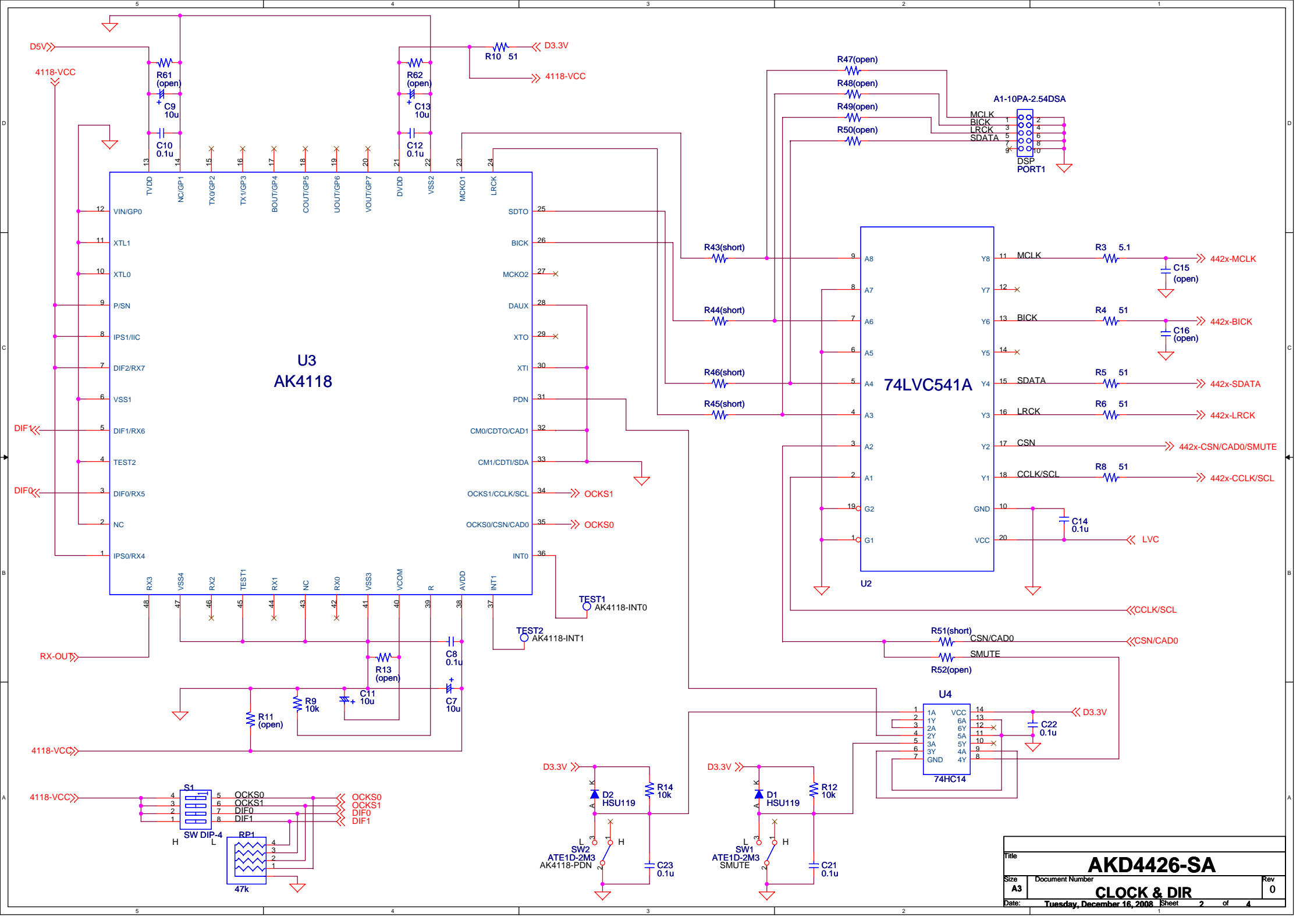
Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
2008/12/25	KM098500	0	First Edition		
2009/09/10	KM098501	1	Device Rev. changed		AK4426: Rev.B Rev.D
2010/02/19	KM098502	2	Device Rev. changed		AK4426: Rev.D Rev.E
				P13 ~ P28	Measurement Results updated

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Title		
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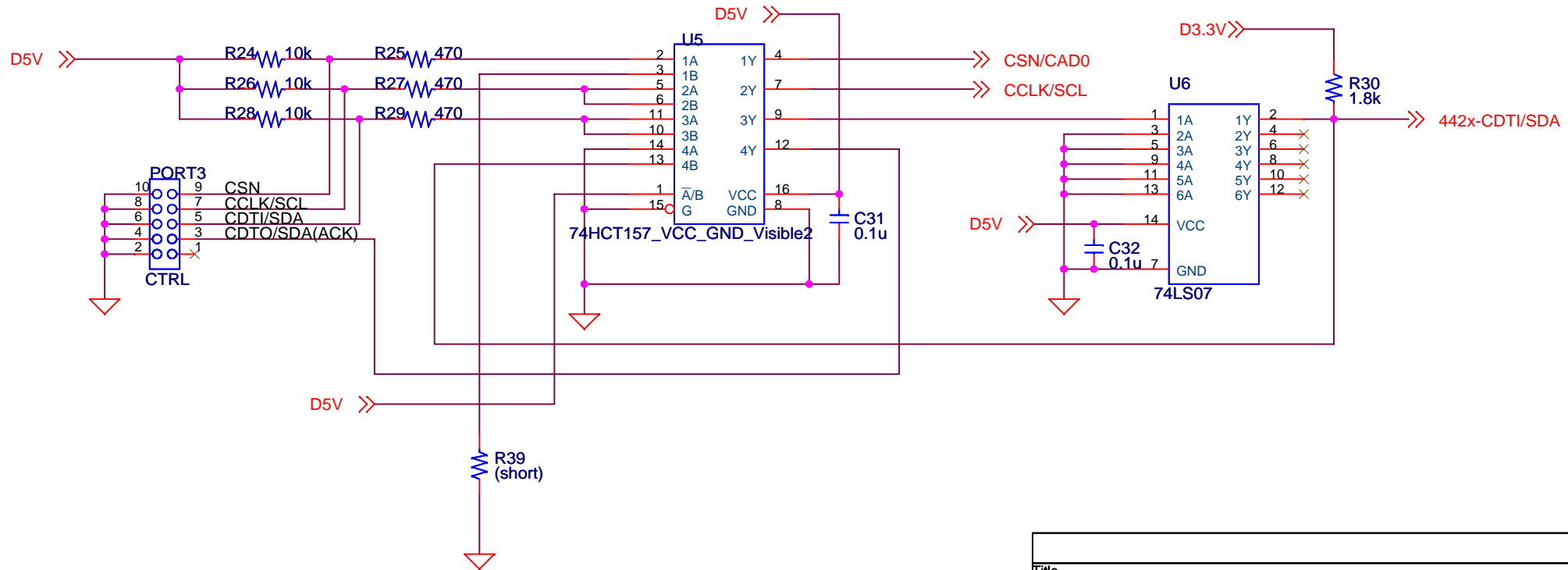
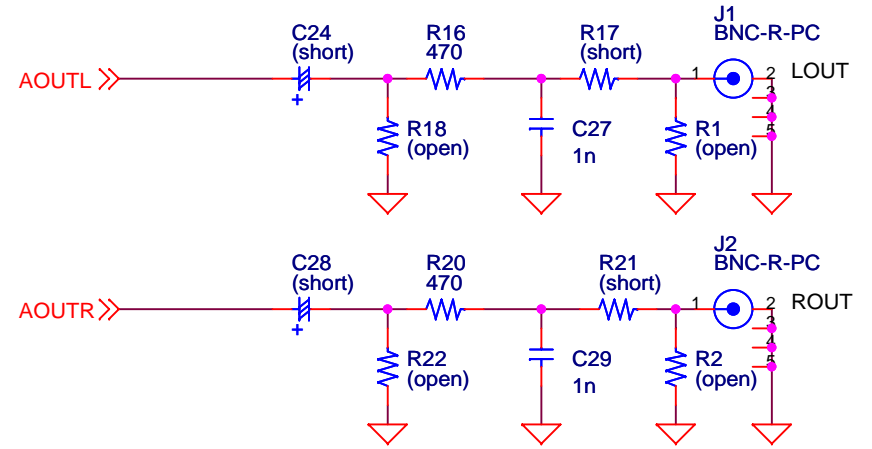
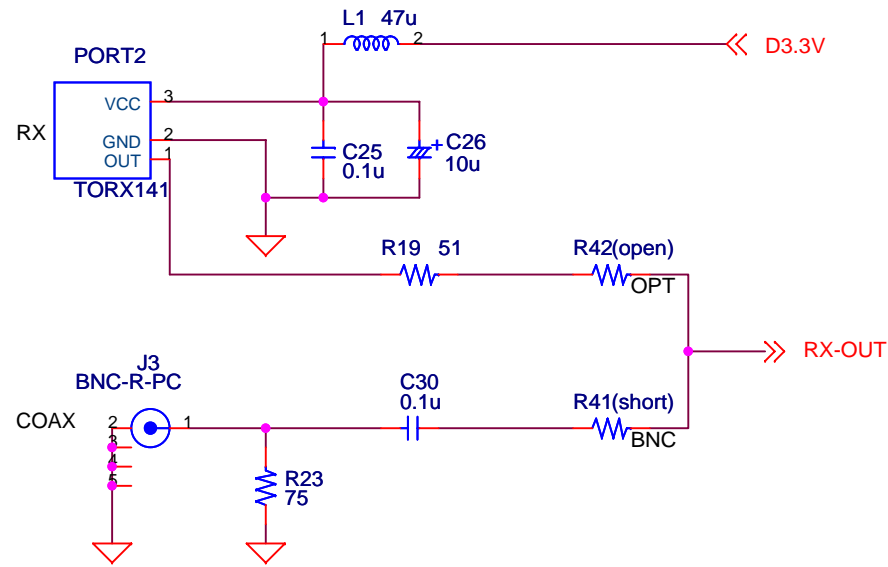
**U3
AK4118**

74LVC541A

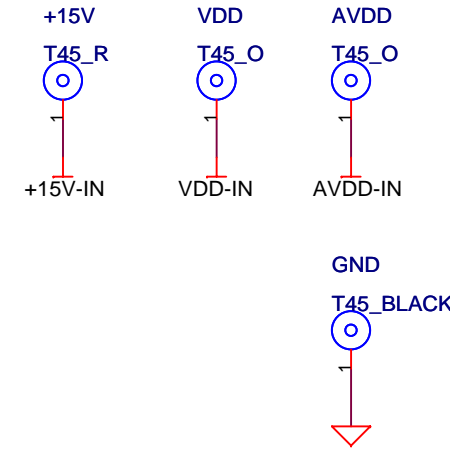
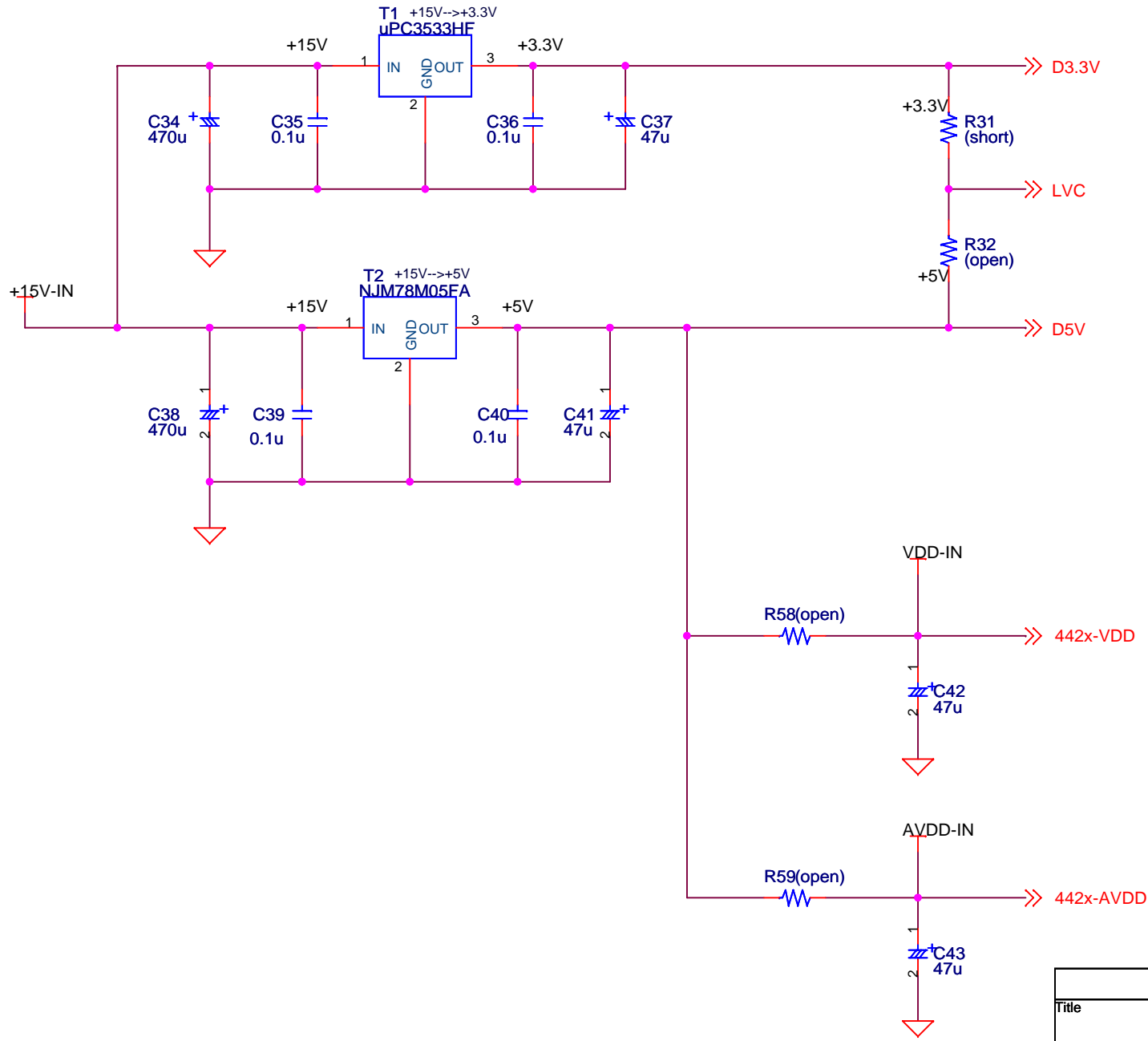
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