INIC-1606
USB to SATA Bridge
Specification

Version 0.1
November 2, 2006
Initio Corporation

Change History:
Create on 11/01/2006.

Table of Contents

1. Introduction:

The INIC-1606 provides an advanced solution to connect SATA devices to USB Host with integrated CPU and embedded SRAM/ROM. To provide high performance and cost effective solution, the INIC-1606 integrates USB-PHY Mass Storage Class Bulk-Only USB function, SATA link/PHY core and microprocessor into a single ASIC. The INIC-1606 provides the data transfer rate of up to 60 MB/sec connecting to a 1.5G SATA interface.

1.1 Feature Summary

- Integrates USB2.0 PHY IP core.
- Data transfer rate of up to 60 MB/sec.
- Integrated internal Turbo 8051 uP with 24KB embedded ROM and 2KB SRAM.
- External NVRAM supported(optional).
- Support HID.
- Up to 9 GPIO pins.
- Only one external crystal.
- Supports SATA (bridged SATA) Hard Disk drives, CD-RW devices, DVDs, Removable media devices, BD drive(Blue Ray)
- USB 1.1 and USB 2.0 compliant.
- USB Mass Storage Class Bulk-Only Transport Specification Compliant.
- SATA specification 1.0 (1.5 Gbps), SATA II and eSATA Compliant).
- Support ATA/ATAPI device DMA and PIO mode.
- 2k bytes of data buffer for data transfer.
- On-Chip 3.3V to 1.8V regulator.
- 64 pin LQFP, 7x7mm or 10x10mm

1.2 Firmware/Software Support

- USB Mass Storage Class Bulk-Only Transport support
- Provide software utilities for NVRAM upgraded.

1.3 Devices Support

- Hard disk drives
- CD-RW devices
- DVDs
- Removable media devices
- Blue Ray drive

2. INIC-1606 Block Diagram:

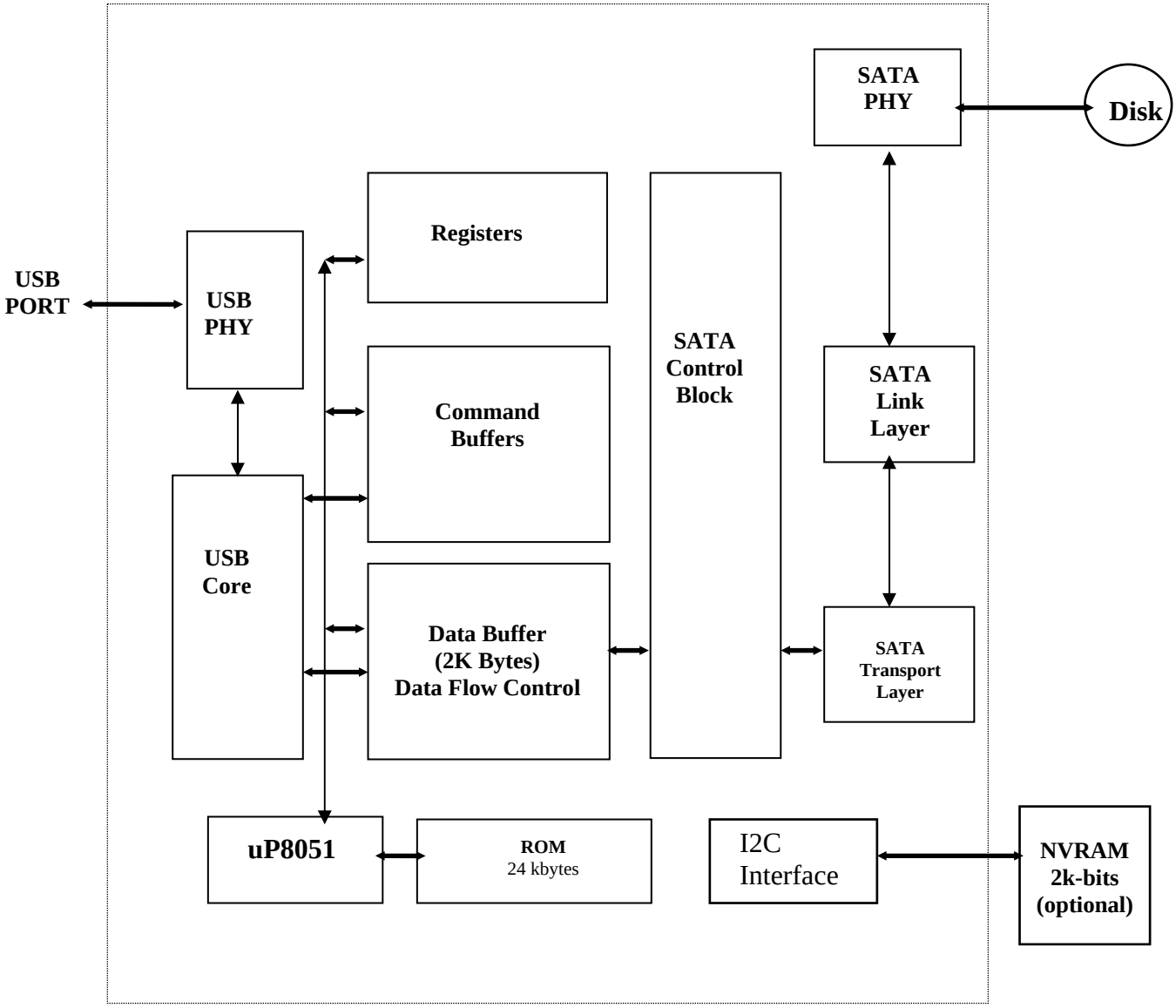
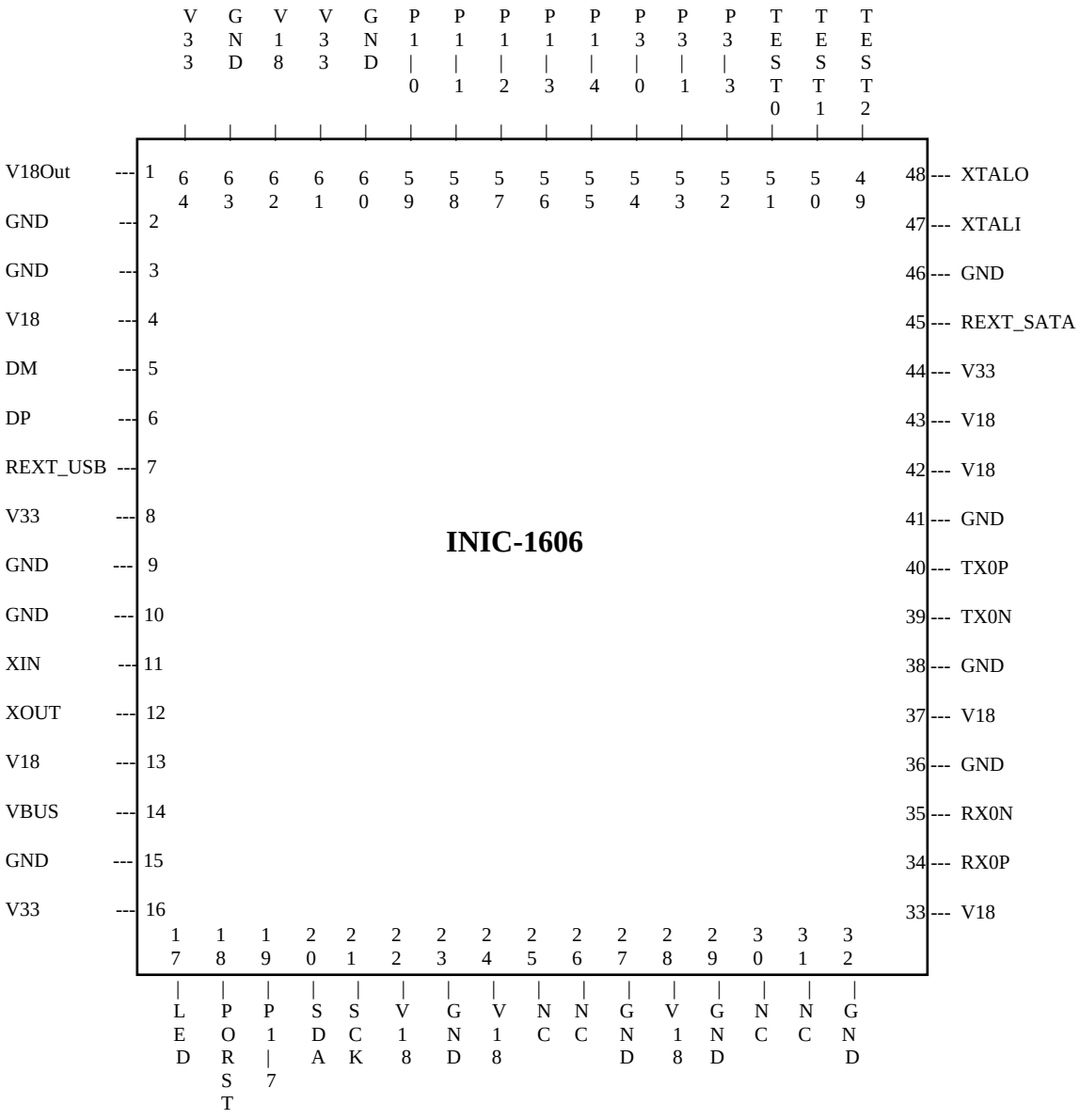


Figure1: USB to SATA Bridge Block Diagram

3. Pin-Out Diagram:



4. Pin Signal Description: (64-pin package)

4.1 USB Interface (Analog pins except VBUS)

Signal Name	Pin Number	I/O	Driver Type	Description
DP	6	I/O	USB high /full speed buffer (D+)	High/Full speed D+ signal
DM	5	I/O	USB high/full speed buffer (D-)	High/Full speed D- signal
REXT_USB	7	A	Power	PLL voltage reference. Current source for 330 ohm(1%) resistor connected to AVSS
VBUS	14	I	No internal pullup/down	Active HIGH. Indicates that VBUS is present.
XIN	11	I	A	Crystal oscillator input (12MHz)
XOUT	12	O	A	Crystal oscillator output (12MHz)

4.2 SATA Interface (Analog pins)

Signal Name	Pin Number	I/O	Driver Type	Description
TX0P (SATA Device)	40	O	SATA	Channel0 Differential Transmit positive signal line
TX0N (SATA Device)	39	O	SATA	Channel0 Differential Transmit negative signal line
RX0P (SATA Device)	34	I	SATA	Channel0 Differential Receive positive signal line
RX0N (SATA Device)	35	I	SATA	Channel0 Differential Receive negative signal line
NC	31	O	SATA	
NC	30	O	SATA	
NC	25	I	SATA	
NC	26	I	SATA	
XTALI	47	I	PX1W	crystal oscillator input (25MHz)
XTALO	48	O		Crystal oscillator output
REXT_SATA	45	I		External Reference Resister (6.19 K ohm)

4.3 System Interface

Signal Name	Pin Number	I/O	Driver Type	Description
PORST#	18	I	Internal pullup 80Kohm	Power On Reset.

4.4 Miscellaneous Interface

Signal Name	Pin Number	I/O	Driver Type	Description
TestMode[2:0]	49,50,51	I	Internal pulldown 80Kohm	Test Mode Select 000: Normal 111: USB PHY test(internal testing)

				100: SATA PHY test(internal testing) 101: Scan Test(ATPG tests) 110: Mbist Test (internal testing)

4.5 NVRAM Interface

Signal Name	Pin Number	I/O	Driver Type	Description
SDA/ P1.6	20	I/O	Internal pull down 80Kohm	1. NRAM data input/output. 2. This pin also configured as P1.6 if NVRAM is not used.
SCK/ P1.5	21	I/O	Internal pullup 80Kohm	1. NVRAM clock. 2. This pin also configured as P1.5 if NVRAM is not used

4.6 GPIO Interface

Signal Name	Pin Number	I/O	Driver Type	Description
LED	17	I/O	Internal pullup 80Kohm	LED: SATA Activity indicator.
P3.3/ INT1#	52	I/O	No internal pullup/down	uP8051 I/O port 3.3, can be used as GPIO
P3.1/ UART_TxD	53	I/O	Internal pullup 80Kohm	uP8051 I/O port 3.1, can be used as GPIOs
P3.0/ UART_RxD	54	I/O	Internal pullup 80Kohm	uP8051 I/O port 3.0, can be used as GPIOs
P1.7	19	I/O	Internal pullup 80Kohm	uP8051 I/O port 1.7, can be used as GPIOs
P1.4	55	I/O	Internal pullup 80Kohm	uP8051 I/O port 1.4, can be used as GPIOs OTB input if enable OTB
P1.3	56	I/O	Internal pullup 80Kohm	uP8051 I/O port 1.3, can be used as GPIOs
P1.2	57	I/O	Internal pullup 80Kohm	uP8051 I/O port 1.2, can be used as output GPIO
P1.1	58	I/O	Internal pull up 80Kohm	uP8051 I/O port 1.1, can be used as output GPIO
P1.0	59	I/O	Internal pullup 80Kohm	uP8051 I/O port 1.0, can be used as GPIOs

4.7 Power Regulator pins

Signal Name	Pin Number	I/O	Driver Type	Description
REG_VCC3	64	I		Total 1 pin
REG_GND	2	I		Total 1 pin
REG_V18Out	1	O		Total 1 pin

4.8 Power/GND

Signal Name	Pin Number	I/O	Driver Type	Description
VCC3	16,61			2 pins (Digital 3.3V)
VCC18	22,62			2 pins (Digital 1.8V)
GND	15,23,60,63			4 pins

USB_VCC3A	8			1 pin:Analog 3.3V (VD33P)
USB_GNDA	9			1 pin:Analog GND (VS33P)
USB_VCC18A	13			1 pin:Analog 1.8V (VDDA) for USB PLL
USB_GND18A	10			1 pin:Analog GND (VSSA) for USB PLL
USB_VCC18	4			1 pin:Digital 1.8V (VDDU)
USB_GND18	3			1 pin:Digital GND (VSSU)
SATA_VDDA	24,28,33,37			4 pins (Analog 1.8V)
SATA_VDDP	42,43			2 pins (SATA PLL 1.8V)
SATA_VDDO	44			1 pin (Xtal PWR 3.3V)
SATA_GNDA	27,29,32,36, 38,41,46			7 pins (Analog GND)

5. Programming Guide:

5.1 CPU Write NVRAM.

1. CPU write access address at register I2C_Addr(0x40E0).
2. CPU write data at register I2C_Data(0x40E1).
3. CPU write Control Code at register I2C_Ctrl(0x40E2).
4. CPU write Run and Read_Write direction(0) at register I2C_Comm(0x40E3).
5. CPU poll I2C_Comm bit 7, wait until cleared.
6. CPU may read register I2C_Status(0x40E4) to check write success or not.

5.2 CPU Read NVRAM.

1. CPU write access address at register I2C_Addr(0x40E0).
2. CPU write Control Code at register I2C_Ctrl(0x40E2).
3. CPU write Run and Read_Write direction(1) at register I2C_Comm(0x40E3).
4. CPU poll I2C_Comm bit 7, wait until cleared.
5. CPU read register I2C_Data(0x40E1).
6. CPU may read register I2C_Status(0x40E4) to check read success or not.

5.3 CPU Poll NVRAM.

After write data to NVRAM, NVRAM need certain time before next write operation can be accepted. CPU may poll NVRAM to decide NVRAM ready or not. It is done same as a NVRAM read. If I2C_Status(0x40E4) bit 0 is 1, the NVRAM not ready.

5.4 Host Read/Write 8051 data space from USB

1. Host send READ_CHIP_ID packet through control channel to read chip-ID, which is 0x29C5_1611 here. Default hardware report PID is 0x160f.
2. Host send HOLD_CPU packet through control channel to set HOLD_CPU bit.
3. Host may send DATA_WRITE/DATA_READ packet through control channel to WRITE/READ 8051 data space.

DATA_WRITE setup packet format is,

offset	field	size	value	Description
0	bmReqType	1	0x40	Vendor write
1	bReq	1	0x81	Data space write

2	wValue	2	Addr[7:0]	Address to be writen
3			Addr[15:8]	
4	wIndex	2	Data[7:0]	Data space data
5			0x00	Don't care
6	wLength	2	0x00	
7			0x00	

DATA_READ setup packet format is,

offset	field	size	value	data	Description
0	bmReqType	1	0xc0	Data from Data space	Vendor read
1	bReq	1	0x82		Data read
2	wValue	2	Addr[7:0]		Address to be writen
3			Addr[15:8]		
4	wIndex	2	0x00		Don't care
5			0x00		Don't care
6	wLength	2	0x01		
7			0x00		

READ_CHIP_ID setup packet format is:

Offset	**Field**	**Size**	**Value**	**Data**	**Description**
0	bmReqType	1	0xc0	Chip-ID **0x11**, **0x16**, 0xc9, 0x25	Vendor read
1	bReq	1	0x03		
2	wValue	2	0x00		
3			0x00		
4	wIndex	2	0x00		Don't care
5			0x00		Don't care
6	wLength	2	0x04		
7			0x00		

HOLD_CPU setup packet format is:

Offset	**Field**	**Size**	**Value**	**Description**
0	bmReqType	1	0x40	Vendor write
1	bReq	1	0x04	HOLD_CPU
2	wValue	2	0x00	Don't care
3			0x00	
4	wIndex	2	0x00	Don't care
5			0x00	Don't care
6	wLength	2	0x00	Don't care
7			0x00	Don't care

5.5 NVRAM Download from USB cable

The download utility may read/write NVRAM through access I2C registers similar as CPU does.

1. Host send READ_CHIP_ID packet through control channel to read chip-ID, which is 0x29C5_1606 here. Default hardware report PID is 0x160f.

2. Host send HOLD_CPU packet through control channel to set HOLD_CPU bit.

5.5.1 NVRAM Write.

3. Host send DATA_WRITE packet with wValue I2C_Addr(0x40E0) and wIndex[15:8] the NVRAM address to be accessed
4. Host send DATA_WRITE packet with wValue I2C_Data(0x40E1) and wIndex[15:8] the value to be write to NVRAM
5. Host send DATA_WRITE packet with wValue I2C_Ctrl(0x40E2) and wIndex[15:8] the Control Code to be write to NVRAM
6. Host send DATA_WRITE packet with wValue I2C_Comm(0x40E3) and wIndex[15:8] the Run bit[b7] and read/write direction 0 [b0]
7. Host poll bit 7 of I2C_Comm(0x40E3) until this bit is cleared by sending DATA_READ packet with wValue I2C_Comm(0x40BF)
8. Host send DATA_READ packet with wValue I2C_Status(0x40E4) to check write success or not

5.5.2 NVRAM Read.

9. Host send DATA_WRITE packet with wValue I2C_Addr(0x40E0) and wIndex[15:8] the NVRAM address to be accessed
10. Host send DATA_WRITE packet with wValue I2C_Ctrl(0x40E2) and wIndex[15:8] the Control Code to be write to NVRAM
11. Host send DATA_WRITE packet with wValue I2C_Comm(0x40E3) and wIndex[15:8] the Run bit[b7] and read/write direction 1 [b0]
12. Host poll bit 7 of I2C_Comm(0x40E3) until this bit is cleared by sending DATA_READ packet with wValue I2C_Comm(0x40E3)
13. Host send DATA_READ packet with wValue I2C_Data(0x40E1) to get the data from NVRAM.
14. Host send DATA_READ packet with wValue I2C_Status(0x40E4) to check write success or not

5.5.3 NVRAM Polling.

Just same as NVRAM Read. If I2C_Status(0x40E4) bit 0 is 1, NVRAM not ready for next write.

6. Electrical Information:

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
Vcc	Power Supply	-0.3	3.6	V
Vin	Input Voltage	-0.3	Vcc+0.3	V
Vout	Output Voltage	-0.3	Vcc+0.3	V
Tstg	Storage Temperature	-55	150	°C

6.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Power Supply	3.0	3.3	3.6	V
Vin	Input Voltage	0	-	Vcc	V
Tj	Commercial Junction Operating Temperature	0	25	115	°C
	Industrial Junction Operation Temperature	-40	25	125	°C

6.3 General DC Characteristics

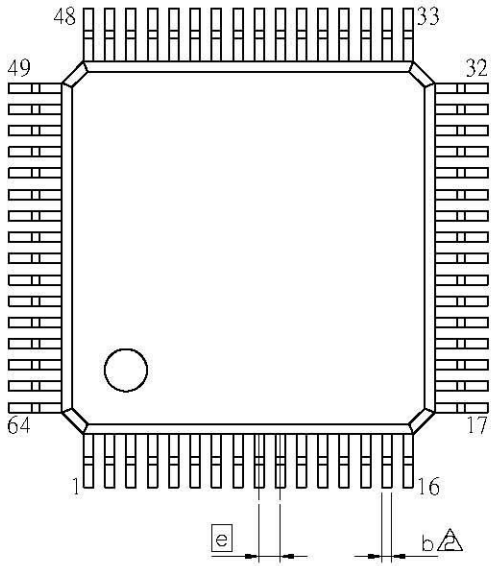
Symbol	Parameter	Min	Typ	Max	Units
Iil	Input Leakage Current	-1		1	μA
Ioz	Tristate Leakage Current	-1		1	μA
Cin	Input Capacitance		2.8		pF
Cout	Output Capacitance	2.7		4.9	pF
Cbid	Bi-directional Buffer Capacitance	2.7		4.9	pF

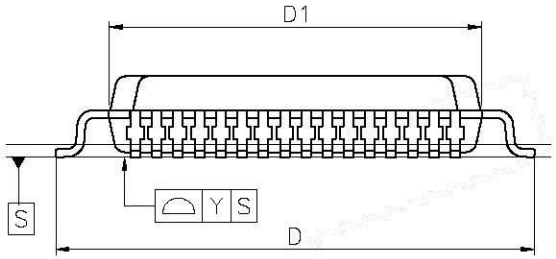
6.4 DC Electrical Characteristics for 3.3V Operation

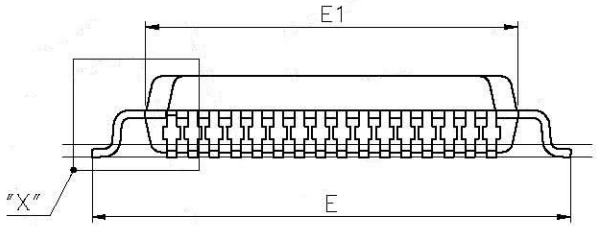
(Under Vcc=3.0-3.6V, Tj=0-115C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil	Input Low Voltage	CMOS	-0.3		0.8	V
Vih	Input High Voltage	CMOS	2.0		5.5	V
Vol	Output Low Voltage	Ioh-2-24mA			0.4	V
Voh	Output High Voltage	Ioh=2-24mA	2.4			V
Ri	Input Pullup/pulldown Resistance	Vil=0/Vih=Vcc		75		kΩ
Icc	Operating Supply Current	Vcc=3.3V			150	mA

7. Packaging Specification

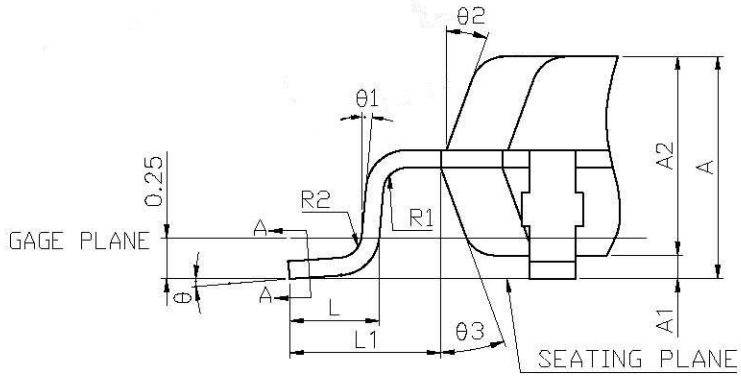






SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	8
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	9.00 BSC			354 BSC		
D1	7.00 BSC			276 BSC		
E	9.00 BSC			354 BSC		
E1	7.00 BSC			276 BSC		
e	0.40 BSC			15.8 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.10			4
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE:
1.REFER TO JEDEC MS-026(ISSUE C)/BBD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.



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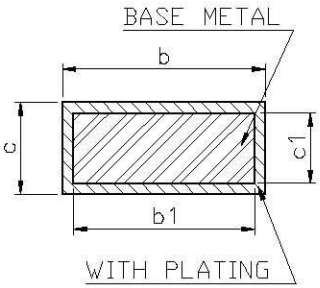

SECTION A-A

REV.	DESCRIPTION	PAGE	DATE	BY
2	Modify the dimension value	1~1		

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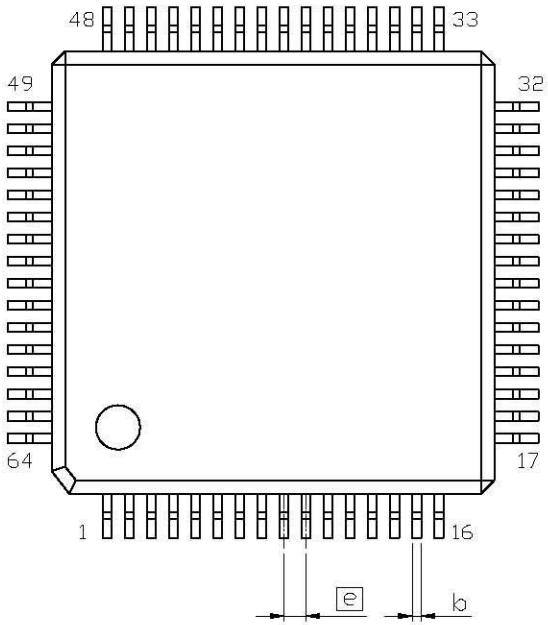
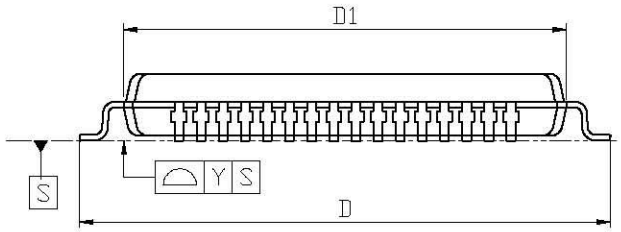
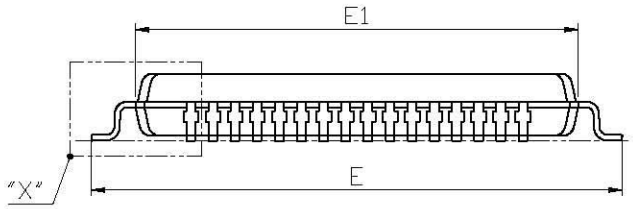
SIZE	A3	BY	DATE
DRAWN			
DESIGNED			
CHECKED			
APPROVED			

TITLE: LQFP64 (7x7x1.4mm)
PACKAGE OUTLINE
Footprint 2.0mm

SCALE: 10 : 1
SHEET: 1 OF 1
PROJ.







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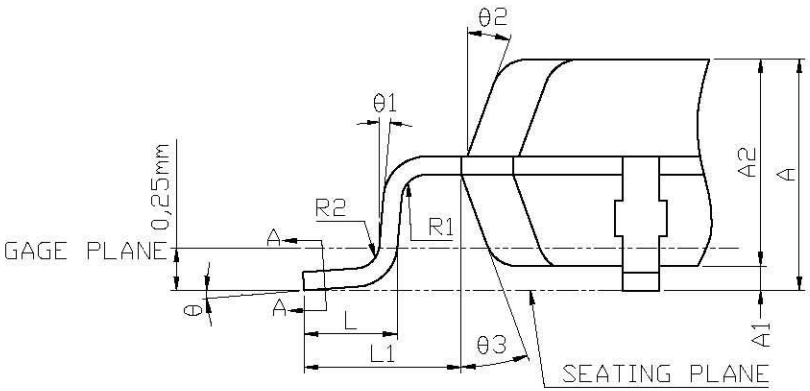
A1	0,05		0,15	2		6
A2	1,35	1,40	1,45	53	55	57
b	0,17	0,22	0,27	7	9	11
b1	0,17	0,20	0,23	7	8	12
c	0,09		0,20	4		8
c1	0,09		0,16	4		6
D	12,00 BSC			472 BSC		
D1	10,00 BSC			394 BSC		
E	12,00 BSC			472 BSC		
E1	10,00 BSC			394 BSC		
e	0,50 BSC			20 BSC		
L	0,45	0,60	0,75	18	24	30
L1	1,00 REF			39 REF		
R1	0,08			3		
R2	0,08		0,20	3		8
Y			0,075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°



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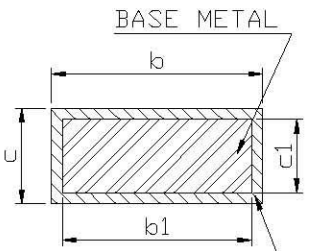

SECTION A-A

NOTES:
1.REFER TO JEDEC MS-026/BCD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

				PKG. CODE	DRAWING NUMBER	REV.
SIZE	A3	BY	DATE	TITLE	LQFP64 (10x10x1.4mm) PACKAGE OUTLINE Footprint 2.0mm	
DRAWN						
DESIGNED						
CHECKED				SCALE	8 : 1	PROJ.
APPROVED				SHEET	1 OF 1	