



**ST3414A** Pb  
Lead-free

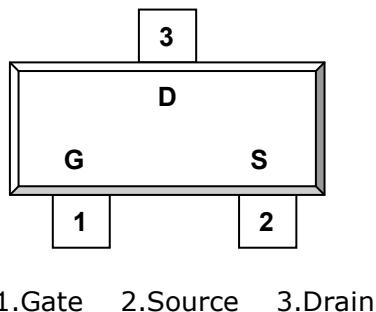
N Channel Enhancement Mode MOSFET

**3.0A**

## DESCRIPTION

ST3414A is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

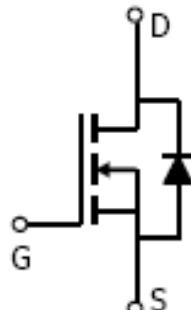
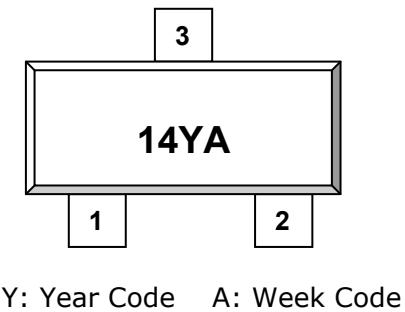
## PIN CONFIGURATION SOT-23



## FEATURE

- 20V/4.2A,  $R_{DS(ON)} = 45m\Omega$  (Typ.)  
@VGS = 4.5V
- 20V/3.4A,  $R_{DS(ON)} = 60 m\Omega$   
@VGS = 2.5V
- 20V/2.8A,  $R_{DS(ON)} = 80 m\Omega$   
@VGS = 1.8V
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

## PART MARKING SOT-23





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**ABSOULTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted )**

<b>Parameter</b>		<b>Symbol</b>	<b>Typical</b>	<b>Unit</b>
Drain-Source Voltage		V <sub>DSS</sub>	20	V
Gate-Source Voltage		V <sub>GSS</sub>	±12	V
Continuous Drain Current TJ=150°C)	T <sub>A</sub> =25°C T <sub>A</sub> =70°C	I <sub>D</sub>	3.0 2.2	A
Pulsed Drain Current		I <sub>DM</sub>	30	A
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	1.2	A
Power Dissipation	T <sub>A</sub> =25°C T <sub>A</sub> =70°C	P <sub>D</sub>	1.25 0.8	W
Operation Junction Temperature		T <sub>J</sub>	-55/150	°C
Storage Temperature Range		T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient		R <sub>θJA</sub>	125	°C/W



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**ELECTRICAL CHARACTERISTICS ( Ta = 25°C Unless otherwise noted )**

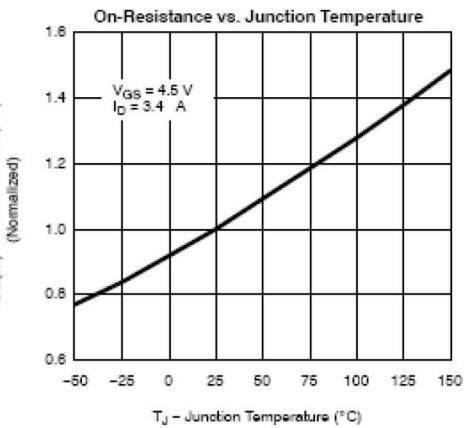
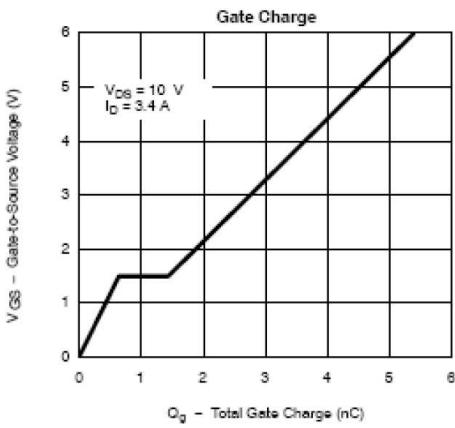
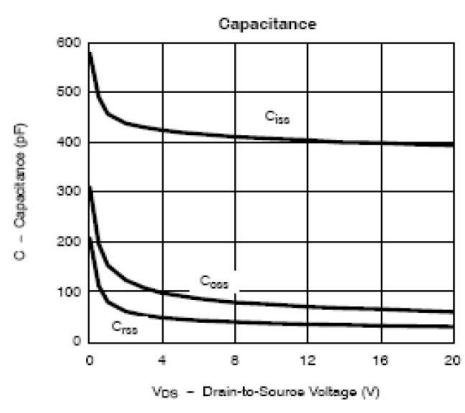
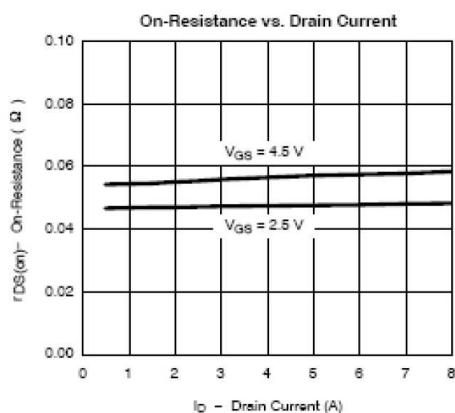
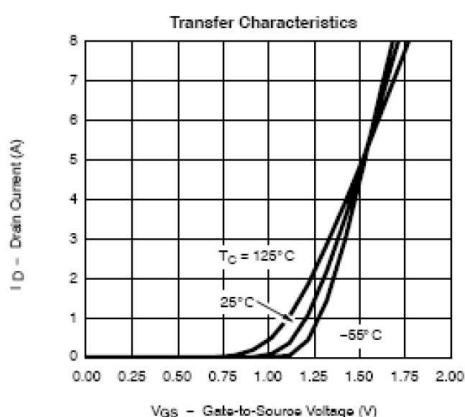
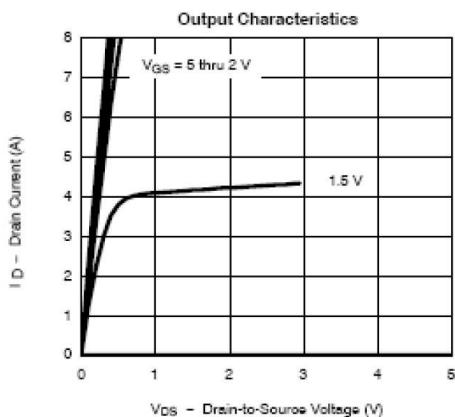
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	20			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	0.40		1.0	V
Gate Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V			1	uA
		V <sub>DS</sub> =20V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			5	
Drain-source On-Resistance	R <sub>D(on)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =3.2A V <sub>GS</sub> =2.5V, I <sub>D</sub> =2.4A V <sub>GS</sub> =1.8V, I <sub>D</sub> =1.8A	0.045 0.060 0.080			Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =4V, I <sub>D</sub> =3.6V		10		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =1.6A, V <sub>GS</sub> =0V		0.8	1.2	V
<b>Dynamic</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V V <sub>GS</sub> =4.5V I <sub>D</sub> =2.8A		4.8	8	nC
Gate-Source Charge	Q <sub>gs</sub>			1.0		
Gate-Drain Charge	Q <sub>gd</sub>			1.0		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =6V V <sub>GS</sub> =0V f=1MHz		485		pF
Output Capacitance	C <sub>oss</sub>			85		
Reverse Transfer Capacitance	C <sub>rss</sub>			40		
Turn-On Time	t <sub>d(on)</sub> tr	V <sub>DD</sub> =6V R <sub>L</sub> =6Ω I <sub>D</sub> =1.0A V <sub>GEN</sub> =4.5V R <sub>G</sub> =6Ω		8	14	nS
Turn-Off Time	t <sub>d(off)</sub> tf			12	18	
				30	35	
				12	16	



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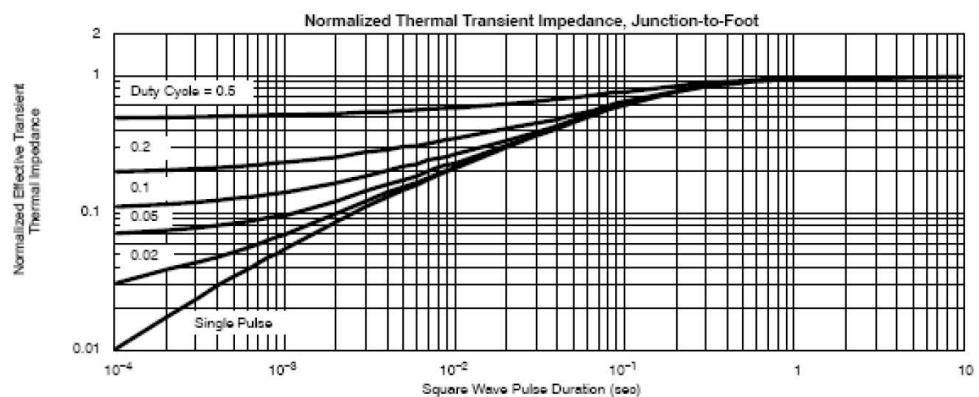
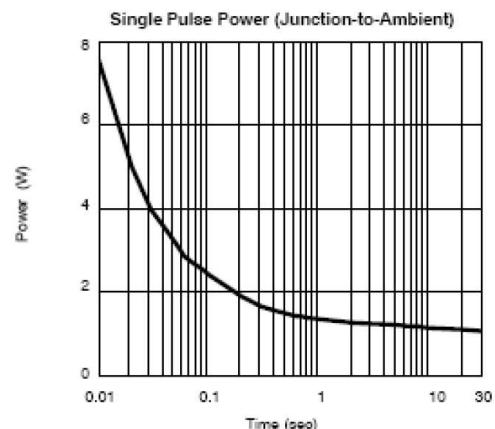
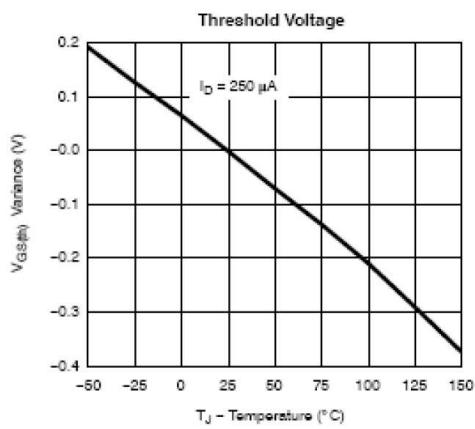
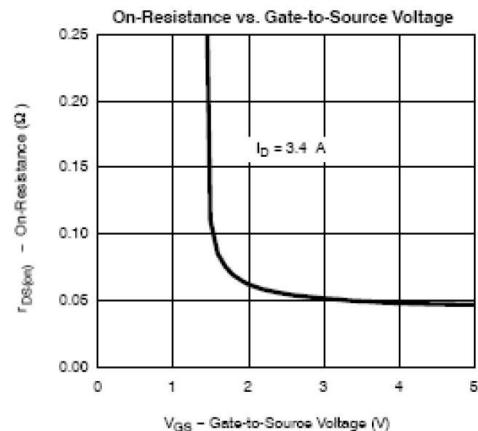
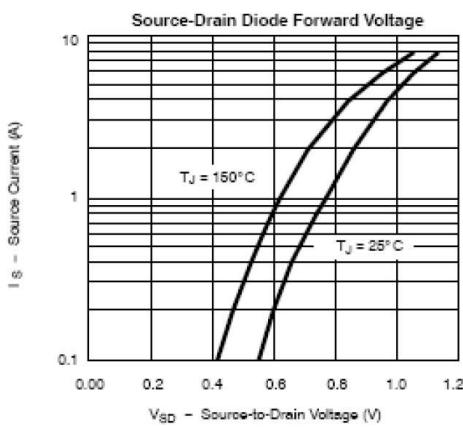




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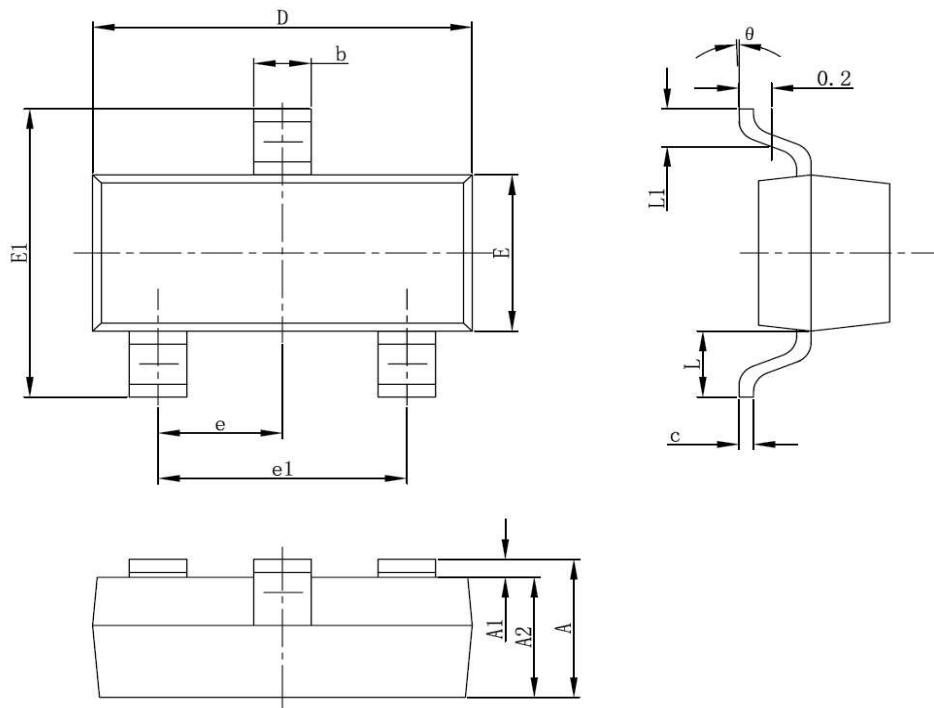




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### SOT-23- PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°