Am2909A/Am2911A

Microprogram Sequencers

DISTINCTIVE CHARACTERISTICS

- 4-bit slice cascadable to form longer word width
- Branch input for N-way branches
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions (Am2909 only)
- Am2909 in 28-pin package & Am2911A in 20-pin package

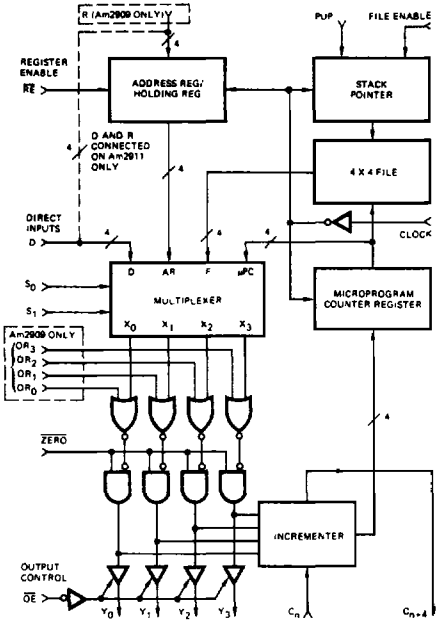
GENERAL DESCRIPTION

The Am2909A is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two Am2909As may be interconnected to generate an eight-bit address (256 words), and three may be used to generate a twelve-bit address (4K words).

The Am2909A can select an address from any of four sources. They are: 1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a four-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The Am2911A is an identical circuit to the Am2909A, except the four OR inputs are removed and the D and R inputs are tied together. The Am2911A is in a 20-pin, 0.3" centers package.

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



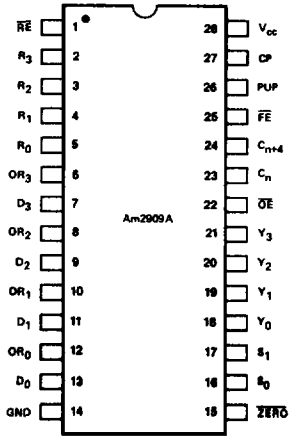
BD002171

03578B

Refer to Page 13-1 for Essential Information on Military Devices

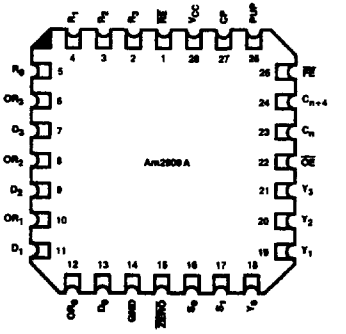
CONNECTION DIAGRAM
Top View

P-28, D-28



CD004332

CHIP-PAK™ L-28-1



CD004311

Note: Pin 1 is marked for orientation

RELATED PRODUCTS

Part No.	Description
Am2918	Pipeline Register
Am2922	Condition Code MUX
Am29803A	16-Way Branch Control Unit
Am29811A	Next Address Control
Am25LS163	4-Bit Counter
Am27S35	Registered PROM

For applications information, see Chapter 11 of **Bit Slice Microprocessor Design,** Mick & Brick, McGraw Hill Publications.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2909A
Am2911A

D — Package
- D – 28-pin CERDIP
- F – 28-pin flatpak
- L – 28-pin leadless chip carrier
- P – 28-pin plastic DIP
- X – Dice

C — Temperature (See Operating Range)
- C – Commercial (0°C to +70°C)
- M – Military (–55°C to +125°C)

B — Screening Option
- Blank – Standard processing
- B – Burn-in

Device type
Microprogram Sequencers

Valid Combinations	
Am2909A Am2911A	PC DC, DCB, DMB FMB LC, LMB XC, XM

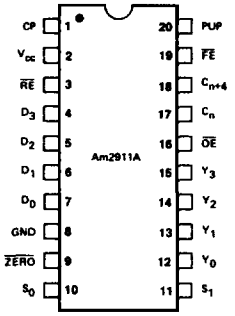
Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

Chip-Pak is a registered trademark of Advanced Micro Devices.

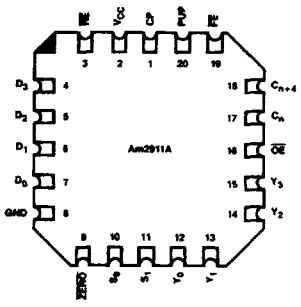
CONNECTION DIAGRAM
Top View

P-20,D-20



CD004321

CHIP PAK™
L-20-1

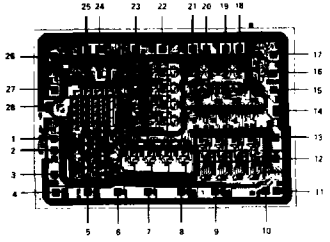


CD004301

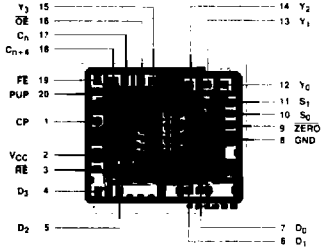
Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT

Am2909A



Am2911A



DIE SIZE 86 x 98 Mils

Chip-Pak is a register trademark of Advanced Micro Devices.

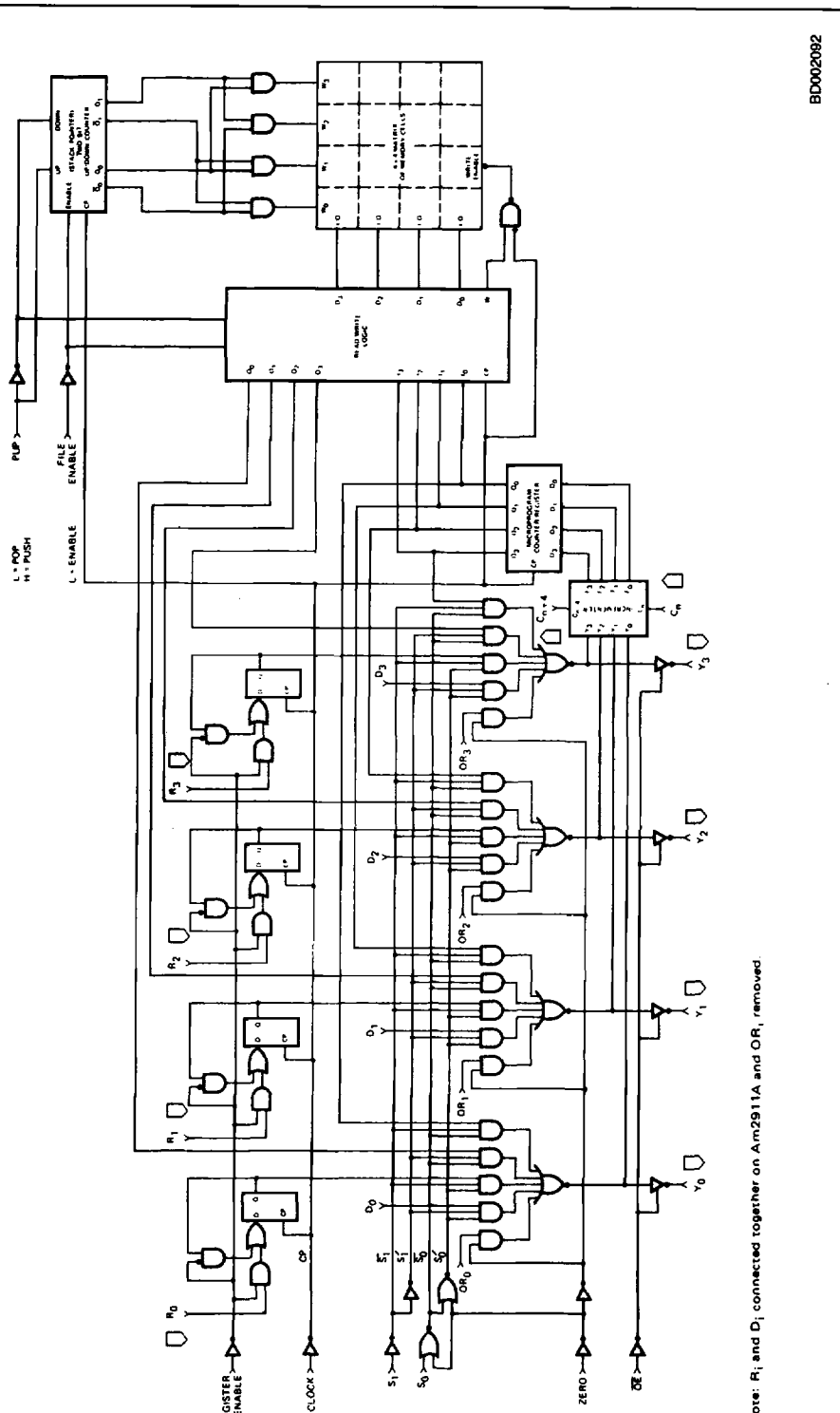


Figure 1. Microprogram Sequencer Block Diagram.

03578B

PIN DESCRIPTION

Pin No.	Name	I/O	Description
17, 16/11, 10	S_1, S_0	I	Control lines for address source selection.
25, 26/19, 20	$\overline{FE}$, PUP	I	Control lines for push/pop stack
1/3	$\overline{RE}$	I	Enable line for internal address register.
6, 8, 10, 12	OR_i	I	Logic OR inputs on each address output line. (2909A ONLY)
15/9	$\overline{ZERO}$	I	Logic AND input on the output lines.
22/16	$\overline{OE}$	I	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance).
23/17	C_n	I	Carry-in to the incrementer.
2, 3, 4, 5	R_i	I	Inputs to the internal address register. (2909A ONLY)
7, 9, 11, 13/4-7	D_i	I	Direct inputs to the multiplexer.
27/1	CP	I	Clock input to the AR and μPC register and Push-Pop stack.
18-21/12-15	Y_i	O	Address outputs from Am2909A. (Address inputs to control memory.)
24/18	C_{n+4}	O	Carry out from the incrementer

ARCHITECTURE OF THE Am2909A/ Am2911A

The Am2909A/Am2911A are bipolar microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256-words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 1.

The device contains a four-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S_0 and S_1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a four-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the Am2911A, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The Am2909A/Am2911A contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out ($C_n + 4$) such that cascading to larger word lengths is straightforward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y + 1 \rightarrow \mu PC$.) Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle ($Y \rightarrow \mu PC$). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last source available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage – the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops or stack references can be achieved. One microinstruction subroutines can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The Am2909A/Am2911A feature three-state Y outputs. These can be particularly useful in designs requiring external equipment to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/ PROM.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL	I_{OH} = −1.0mA	2.4			Volts
			COM'L	I_{OH} = −2.6mA	2.4			
V_{CC} = MIN V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA, 2909A/11A				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL, 2909A/11A			0.7	Volts
				All others			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	C_n				−1.08	mA
			Push/Pop, $\overline{OE}$				−0.72	
			Others (Note 6)				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	C_n				40	μA
			Push/Pop, $\overline{OE}$				40	
			Others (Note 6)				20	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V	C_n, Push/Pop				0.2	mA
			Others (Note 6)				0.1	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 6V V_{OUT} = 0.5V		Y_0-Y_3	−30		−100	mA
				C_{n+4}	−30		−85	
I_{CC}	Power Supply Current	V_{CC} = MAX (Note 4)	COM'L Only	T_A = 0 to +70°C			130	mA
			MIL Only	T_C = −55 to +125°C			140	
				T_C = +125°C			110	
I_{OZL}	Output OFF Current	V_{CC} = MAX, $\overline{OE}$ = 2.7	Y_0-3	V_{OUT} = 0.4V			−20	μA
I_{OZH}				V_{OUT} = 2.7V			20	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply GND to C_n, R_0, R_1, R_2, R_3, OR_0, OR_1, OR_2, OR_3, D_0, D_1, D_2 and D_3. Other inputs high. All outputs open. Measured after a LOW-to-HIGH clock transition.
5. For the Am2911A, D_i and R_i are internally connected. Loading is doubled (to same values as Push/Pop).

03578B

Refer to Page 13-1 for Essential Information on Military Devices

Am2909A/Am2911A SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables I, II and III below define the timing characteristics of the Am2909A/Am2911A over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading.

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

Time	COMMERCIAL	MILITARY
Minimum Clock LOW Time	20	20
Minimum Clock HIGH Time	20	20

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS

(all in ns, C_L = 50pF (except output disable tests))

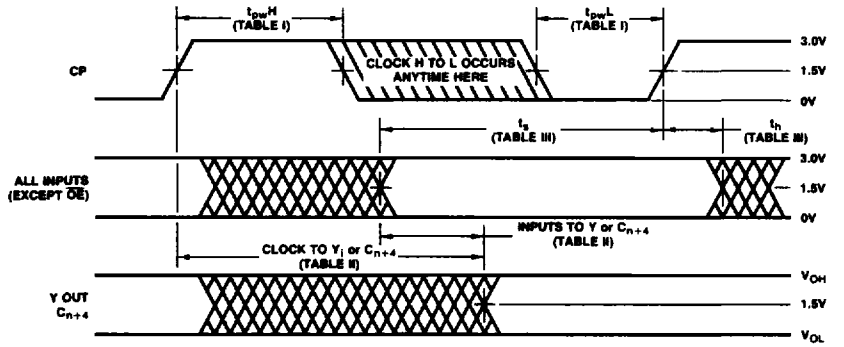
From Input	COMMERCIAL		MILITARY	
	Y	C_{n+4}	Y	C_{n+4}
D_i	17	22	20	25
S_0, S_1	29	34	29	34
OR_i	17	22	20	25
C_n	–	14	–	16
$\overline{ZERO}$	29	34	30	35
OE LOW (enable)	25	–	25	–
OE HIGH (disable)*	25	–	25	–
Clock ↑ S_1S_0 = LH	39	44	45	50
Clock ↑ S_1S_0 = LL	39	44	45	50
Clock ↑ S_1S_0 = HL	44	49	53	58

*C_L = 5pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	COMMERCIAL		MILITARY	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
$\overline{RE}$		19	4	19	5
R_i	2	10	4	12	5
PUP		25	4	27	5
$\overline{FE}$		25	4	27	5
C_n		18	4	18	5
D_i		25	0	25	0
OR_i		25	0	25	0
S_0, S_1		25	0	29	0
$\overline{ZERO}$		25	0	29	0

Notes: 1. All times relative to clock LOW-to-HIGH transition.
2. On Am2911A, R_i and D_i are internally connected together and labeled D_i. Use R_i set-up and hold times when D inputs are used to load register.



WF002600

OPERATION OF THE Am2909A/Am2911A

Figure 2 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Figure 2 also shows the truth table for the output control and for the control of the push/pop stack. Figure 3 shows in detail the effect of S_0, S_1, $\overline{FE}$ and PUP on the Am2909A. These four signals define what address appears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

Address Selection

S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
L	L	Microprogram Counter	μPC
L	H	Address/Holding Register	AR
H	L	Push-Pop stack	STK0
H	H	Direct inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 2.

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N	L L L L	J	K	Ra	Rb	Rc	Rd	J	Pop Stack	End
N + 1	—	J + 1	K	Rb	Rc	Rd	Ra	—		Loop
N	L L L H	J	K	Ra	Rb	Rc	Rd	J	Push μPC	Set-up
N + 1	—	J + 1	K	J	Ra	Rb	Rc	—		Loop
N	L L H X	J	K	Ra	Rb	Rc	Rd	J	Continue	Continue
N + 1	—	J + 1	K	Ra	Rb	Rc	Rd	—		
N	L H L L	J	K	Ra	Rb	Rc	Rd	K	Pop Stack;	End
N + 1	—	K + 1	K	Rb	Rc	Rd	Ra	—	Use AR for Address	Loop
N	L H L H	J	K	Ra	Rb	Rc	Rd	K	Push μPC;	JSR AR
N + 1	—	K + 1	K	J	Ra	Rb	Rc	—	Jump to Address in AR	
N	L H H X	J	K	Ra	Rb	Rc	Rd	K	Jump to Address in AR	JMP AR
N + 1	—	K + 1	K	Ra	Rb	Rc	Rd	—		
N	H L L L	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0;	RTS
N + 1	—	Ra + 1	K	Rb	Rc	Rd	Ra	—	Pop Stack	
N	H L L H	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0;	
N + 1	—	Ra + 1	K	J	Ra	Rb	Rc	—	Push μPC	
N	H L H X	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0	Stack Ref
N + 1	—	Ra + 1	K	Ra	Rb	Rc	Rd	—		(Loop)
N	H H L L	J	K	Ra	Rb	Rc	Rd	D	Pop Stack;	End
N + 1	—	D + 1	K	Rb	Rc	Rd	Ra	—	Jump to Address on D	Loop
N	H H L H	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D;	JSR D
N + 1	—	D + 1	K	J	Ra	Rb	Rc	—	Push μPC	
N	H H H X	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D	JMP D
N + 1	—	D + 1	K	Ra	Rb	Rc	Rd	—		

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH
Note: STK0 is the location addressed by the stack pointer.

Figure 3. Output and Internal Next-Cycle Register States for Am2909A/Am2911A.

Figure 4 illustrates the execution of a subroutine using the Am2909A. The configuration of Figure 6 is assumed. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also control (indirectly, perhaps) the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the Am2909A at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J + 2, the sequence control portion of the microinstruction contains the command "Jump to subroutine at A". At the time T_2, this instruction is in the μWR, and the Am2909A inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J + 3 is pushed onto the stack. The return instruction is executed at T_5. Figure 5 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J - 1	–
T_0	J	–
T_1	J + 1	–
T_2	J + 2	JSR A
T_6	J + 3	–
T_7	J + 4	–
	–	–
	–	–
	–	–
	–	–
	–	–
T_3	A	I(A)
T_4	A + 1	–
T_5	A + 2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock Signals											
Am2909A Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	J + 4	J + 5		
	STK0	–	–	–	J + 3	J + 3	J + 3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
Am2909A Output	Y	J + 1	J + 2	A	A + 1	A + 2	J + 3	J + 4	J + 5		
ROM Output	(Y)	I(J + 1	**JSR A**	I(A)	I(A + 1)	**RTS**	I(J + 3)	I(J + 4)	I(J + 5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J + 1)	**JSR A**	I(A)	I(A + 1)	**RTS**	I(J + 3)	I(J + 4)		

C_N = HIGH

Figure 4. Subroutine Execution.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J - 1	–
T_0	J	–
T_1	J + 1	–
T_2	J + 2	JSR A
T_9	J + 3	–
	–	–
	–	–
	–	–
	–	–
	–	–
T_3	A	–
T_4	A + 1	–
T_5	A + 2	JSR B
T_7	A + 3	–
T_8	A + 4	RTS
	–	–
	–	–
	–	–
	–	–
T_6	B	RTS
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock Signals											
Am2909A Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	B + 1	A + 4	A + 5	J + 4
	STK0	–	–	–	J + 3	J + 3	J + 3	A + 3	J + 3	J + 3	–
	STK1	–	–	–	–	–	–	J + 3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
Am2909A Output	Y	J + 1	J + 2	A	A + 1	A + 2	B	A + 3	A + 4	J + 3	J + 4
ROM Output	(Y)	I(J + 1)	**JSR A**	I(A)	I(A + 1)	**JSR B**	**RTS**	I(A + 3)	**RTS**	I(J + 3)	I(J + 4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J + 1)	**JSR A**	I(A)	I(A + 1)	**JSR B**	**RTS**	I(A + 3)	**RTS**	I(J + 3)

C_N = HIGH

Figure 5. Two Nested Subroutines. Routine B Is Only One Instruction.

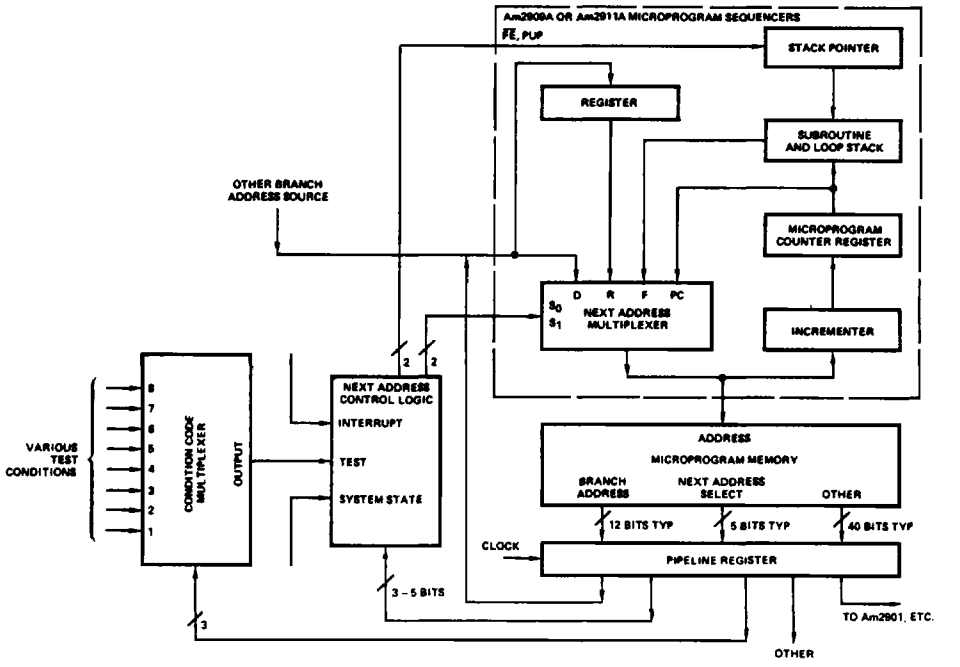
USING THE Am2909A AND Am2911A

The Am2909A and Am2911A are four-bit slice sequencers which are cascaded to form a microprogram memory address generator. Both products make available to the user several lines which are used to directly control the internal holding register, multiplexer and stack. By appropriate control of these lines, the user can implement any desired set of sequence control functions; by cascading parts he can generate any desired address length. These two qualities set the Am2909A and Am2911A apart from the Am2910, which is architecturally similar, but is fixed at 12 bits in length and has a fixed set of 16 sequence control instructions. The Am2909A or Am2911A should be selected instead of the Am2910 under the following conditions:

- Address less than 8 bits and not likely to be expanded
- Address longer than 12 bits
- More complex instruction set needed than is available on Am2910

Architecture of the Control Unit

The recommended architecture using the Am2909A or Am2911A is shown in Figure 6. Note that the path from the pipeline register output through the next address logic, multiplexer, and microprogram memory is all combinational. The pipeline register contains the current microinstruction being executed. A portion of that microinstruction consists of a sequence control command such as "continue", "loop", "return-from-subroutine", etc. The bits representing this sequence command are logically combined with bits representing such things as test conditions and system state to generate the required control signals to the Am2909A or Am2911A. The block labeled "next address logic" may consist of simple gates, a PROM or a PLA, but it should be all combinational.



AF001371

Figure 6. Recommended Computer Control Unit Architecture Using the Am2911A or Am2909A.

The Am29811A is a combinational circuit which implements 16 sequence control instructions; it may be used with either an Am2909A or an Am2911A. The set of instructions is nearly identical to that implemented internally in the Am2910.

Figure 7 shows the CCU of Figure 6 with the Am29811A in place. The Am29811A, in addition to controlling the Am2911A, also controls a loop counter and several branch address sources. The instructions which are implemented by the Am29811A are shown in Figure 8, along with the Am29811A outputs for each instruction. Generating any instruction set consists simply of writing a truth table and designing combinational logic to implement it. For more detailed information refer to "The Microprogramming Handbook".

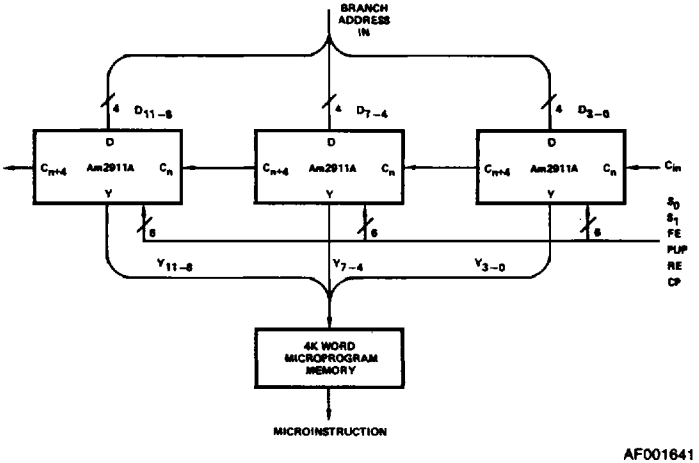


Figure 9. Twelve Bit Sequencer.

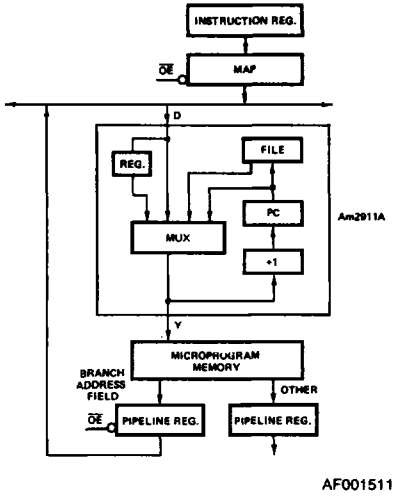


Figure 10. Branch Address Structures.

Expansion of the Am2909A or Am2911A

Figure 9 shows the interconnection of three Am2911A's to form a 12-bit sequencer. Note that the only interconnection between packages, other than the common clock and control lines, is the ripple carry between μPC incrementors. This carry path is not in the critical speed path if the Am2911A Y outputs drive the microprogram memory, because the ripple carry occurs in parallel with the memory access time. If, on the other hand, a micro-address register is placed at the Am2911A output, then the carry may lie in the critical speed path, since the last carry-in must be stable for a set-up time prior to the clock.

Selecting Between the Am2909A and Am2911A

The difference between the Am2909A and the Am2911A involves two signals: the data inputs to the holding register and the "OR" inputs. In the Am2909A, separate four-bit fields are provided for the holding register and the direct branch inputs to the multiplexer. In the Am2911A, these fields are internally tied together. This may affect the design of the branch address system, as shown in Figure 10. Using the Am2909A, the register inputs may be connected directly to the microprogram memory; the internal register replaces part of the pipeline register. The direct (D) inputs may be tied to the mapping logic which translates instruction op codes into microprogram addresses. While the same technique might be used with the Am2911A, it is more common to connect the Am2911A's D inputs to a branch address bus onto which various sources may be enabled. Shown in Figure 10 is a pipeline register and a mapping ROM. Other sources might also be applied to the same bus. The internal register is used only for temporary storage of some previous branch address.

MNEMONIC	FUNCTION	INPUTS					OUTPUTS							
							NEXT ADDR SOURCE		FILE		COUNTER			
		I_3	I_2	I_1	I_0	TEST	S_1	S_0	$\overline{FE}$	PUP	$\overline{LOAD}$	$\overline{EN}$	$\overline{MAP\ E}$	$\overline{PL\ E}$
	PIN NO.	14	13	12	11	10	4	5	3	2	6	7	1	9
JZ	JUMP ZERO	L L	L L	L L	L L	L H	H H	H H	H H	H H	L L	L L	H H	L L
CJS	CON JSB PL	L L	L L	L L	H H	L H	L H	L H	H L	H H	H H	H H	H H	L L
JMAP	JUMP MAP	L L	L L	H H	L L	L H	H H	H H	H H	H H	H H	H H	L L	H H
CJP	COND JUMP PL	L L	L L	H H	H H	L H	L H	L H	H H	H H	H H	H H	H H	L L
PUSH	PUSH/COND LD CNTR	L L	H H	L L	L L	L H	L L	L L	L L	H H	H L	H H	H H	L L
JSRP	COND JSB R/PL	L L	H H	L L	H H	L H	L H	H H	L L	H H	H H	H H	H H	L L
CVJ	COND JUMP VECTOR	L L	H H	H H	L L	L H	L H	L H	H H	H H	H H	H H	H H	H H
JRP	COND JUMP R/PL	L L	H H	H H	H H	L H	L H	H H	H H	H H	H H	H H	H H	L L
RFCT	REPEAT LOOP, CTR # 0	H	L	L	L	H	L	L	L	L	H	H	H	L
RPCT	REPEAT PL, CTR # 0	H H	L L	L L	H H	L H	H L	H L	H H	H H	H H	L H	H H	L L
CRTN	COND RTN	H H	L L	H H	L L	L H	L H	L L	H L	L L	H H	H H	H H	L L
CJPP	COND JUMP PL & POP	H H	L L	H H	H H	L H	L H	L H	H L	L L	H H	H H	H H	L L
LDCT	LD CNTR & CONTINUE	H H	H H	L L	L L	L H	L L	L L	H H	H H	L L	H H	H H	L L
LOOP	TEST END LOOP	H H	H H	L L	H H	L H	H L	L L	H L	L L	H H	H H	H H	L L
CONT	CONTINUE	H H	H H	H H	L L	L H	L L	L L	H H	H H	H H	H H	H H	L L
JP	JUMP PL	H H	H H	H H	H H	L H	H H	H H	H H	H H	H H	H H	H H	L L

L = LOW
H = HIGH

Figure 8. AM29811A TRUTH TABLE

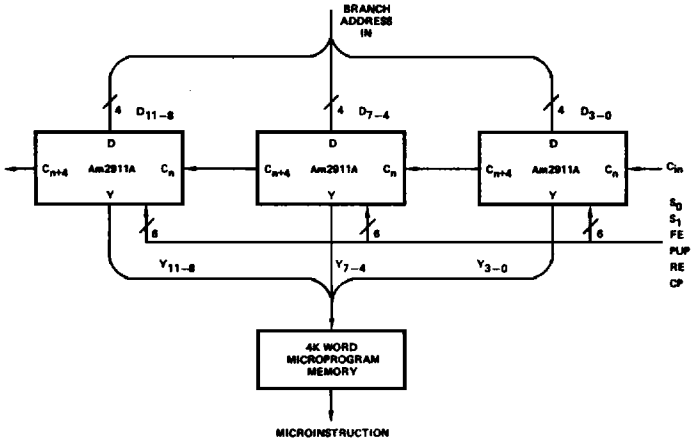


Figure 9. Twelve Bit Sequencer.

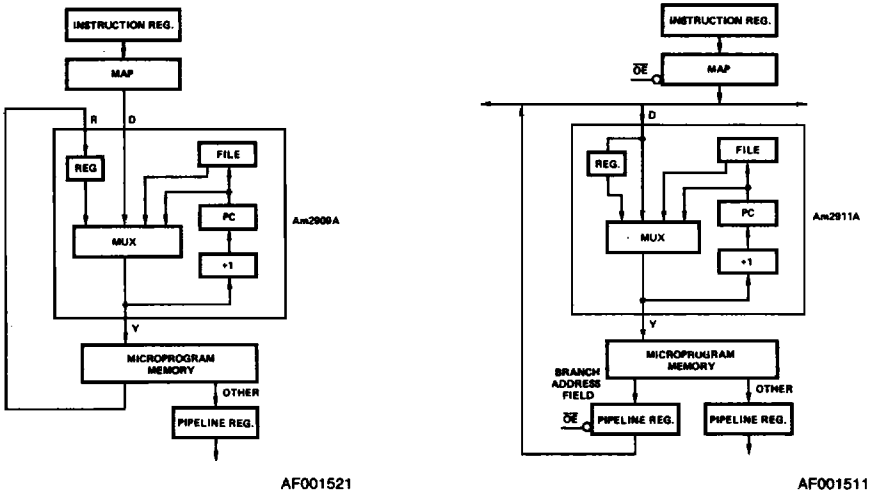
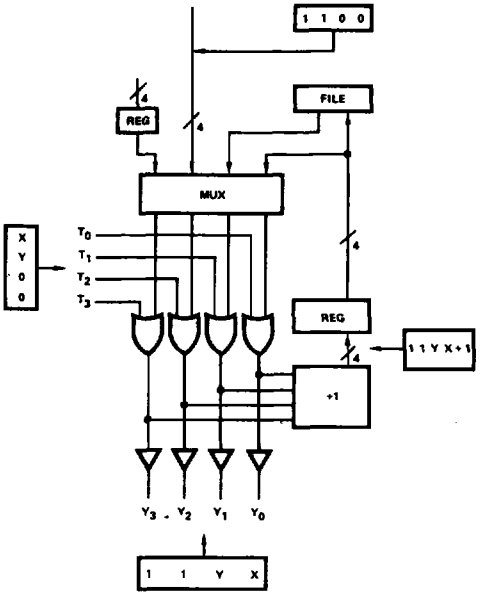


Figure 10. Branch Address Structures.

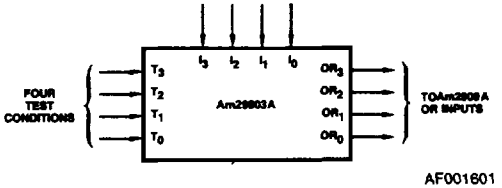
The second difference between the Am2909A and Am2911A is that the Am2909A has OR inputs available on each address output line. These pins can be used to generate multi-way single-cycle branches by simply tying several test conditions into the OR lines. See Figure 11. Typically, a branch is taken to an address with zeroes in the least significant bits. These bits are replaced with 1's or 0's by test conditions applied to the OR lines. In Figure 11, the states of the two test conditions X and Y result in a branch to 1100, 1101, 1110, or 1111.



AF001610

Figure 11. Use of OR Inputs to Obtain 4 - Way Branch.

The Am29803A has been designed to selectively apply any or all of four different test conditions to an Am2909A. Figure 12 shows the truth table for this device. A nice trade off between flexibility and board space is achieved by using a single 28-pin Am2909A for the least significant four bits of a sequencer, and using the space-saving 20-pin Am2911A's for the remainder of the bits. A detailed logic design for such a system is contained in "The Microprogramming Handbook."



AF001601

Figure 12.

How to Perform Some Common Functions with the Am2909A or Am2911A

1. CONTINUE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
PC	HOLD	H	L	L	H	X

Contents of PC placed on Y outputs; PC incremented.

2. BRANCH

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	HOLD	H	H	H	H	X

Feed data on D inputs straight through to memory address lines. Increment address and place in PC.

3. JUMP-TO-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	PUSH	H	H	H	L	H

Subroutine address fed from D inputs to memory address. Current PC is pushed onto stack, where it is saved for the return.

4. RETURN-FROM-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
STACK	POP	H	H	L	L	L

The address at the top of the stack is applied to the microprogram memory, and is incremented for PC on the next cycle. The stack is popped to remove the return address.

Am29803 FUNCTION TABLE

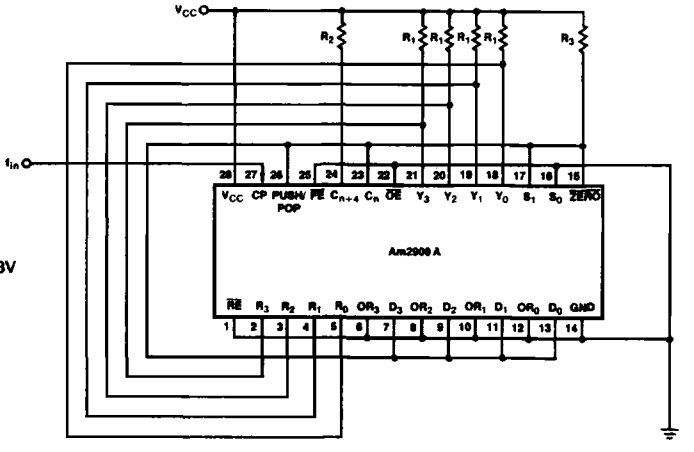
	BRANCH ON	I_3	I_2	I_1	I_0	OR_3	OR_2	OR_1	OR_0
NONE	NONE	L	L	L	L	L	L	L	L
Two-way Branches	T_0	L	L	L	H	L	L	L	T_0
	T_1	L	L	H	L	L	L	L	T_1
	T_2	L	H	L	L	L	L	L	T_2
	T_3	H	L	L	L	L	L	L	T_3
Four-Way Branches	T_1 & T_0	L	L	H	H	L	L	T_1	T_0
	T_2 & T_0	L	H	L	H	L	L	T_2	T_0
	T_3 & T_0	H	L	L	H	L	L	T_3	T_0
	T_2 & T_1	L	H	H	L	L	L	T_2	T_1
	T_3 & T_1	H	L	H	L	L	L	T_3	T_1
	T_3 & T_2	H	H	L	L	L	L	T_3	T_2
Eight-Way Branches	T_2, T_1, T_0	L	H	H	H	L	T_2	T_1	T_0
	T_3, T_1, T_0	H	L	H	H	L	T_3	T_1	T_0
	T_3, T_2, T_0	H	H	L	H	L	T_3	T_2	T_0
	T_3, T_2, T_1	H	H	H	L	L	T_3	T_2	T_1
Sixteen-Way Branch	T_3, T_2, T_1, T_0	H	H	H	H	T_3	T_2	T_1	T_0

Burn-In Circuit for Am2909A (Flatpack and CERDIP)

Notes:
Max. I_{CC} = 200mA
T_A = +125°C
Resistors = ±5%

R_1 = 390Ω
R_2 = 560Ω
R_3 = 1kΩ
f_{in} = 100kHz, 50% duty-cycle, 0-3V

V_{CC} min. = 5.0V
V_{CC} max. = 5.1V



BC000011

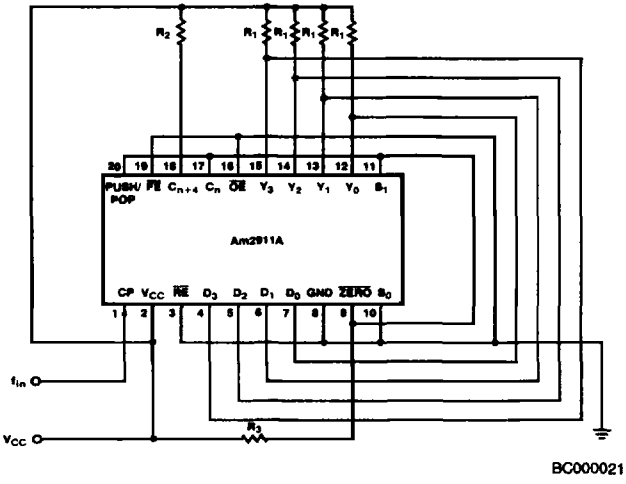
This circuit conforms to MIL-STD-883, Method 1005 and 1015, Condition D. Parallel excitation.

Burn-In Circuit for Am2911A

Notes:
Max. I_{CC} = 200mA
T_A = +125°C
Resistors = ±5%

R_1 = 390Ω
R_2 = 560Ω
R_3 = 1kΩ
f_{in} = 100kHz, 50% duty-cycle, 0-3V

From clock buffer on each board:
V_{CC} min. = 5.0V
V_{CC} max. = 5.1V

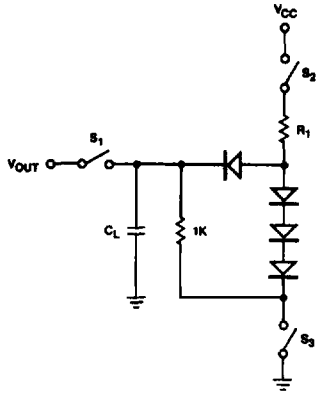


BC000021

This circuit conforms to MIL-STD-883, Method 1005 and 1015, Condition D. Parallel excitation.

SWITCHING TEST CIRCUIT

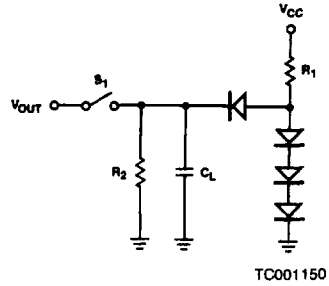
A. THREE-STATE OUTPUTS



TC001140

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



TC001150

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in text fixture.
2. S_1, S_2, S_3 are closed during function tests all and AC tests except output enable tests.
3. S_1 and 3_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS

			Am2909A	
Pin #	**Pin Label**	**Test Circuit**	**R_1**	**R_2**
18-21	Y_{0-3}	A	220	1K
24	C_{n+4}	B	220	2.4K

TEST OUTPUT LOADS

			Am2911A	
Pin #	**Pin Label**	**Test Circuit**	**R_1**	**R_2**
12-15	Y_{0-3}	A	220	1K
18	C_{n+4}	B	220	2.4K

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.