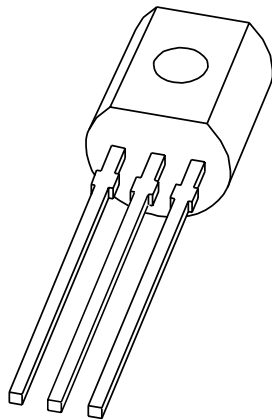


DATA SHEET



PBSS5350SA

50 V low V_{CEsat} PNP transistor

Objective specification
Supersedes data of 2002 Oct 22

2004 Aug 23

50 V low V_{CEsat} PNP transistor

PBSS5350SA

FEATURES

- Low collector-emitter saturation voltage V_{CEsat} and corresponding R_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain h_{FE}
- Less heat generation leading to higher efficiency.

APPLICATIONS

- Low and medium power DC/DC convertors
- Low voltage regulation (LDO)
- MOSFET drivers
- Supply line switching
- Battery chargers.

DESCRIPTION

PNP low V_{CEsat} transistor in a SOT54 plastic package.
NPN complement: PBSS4350SA.

MARKING

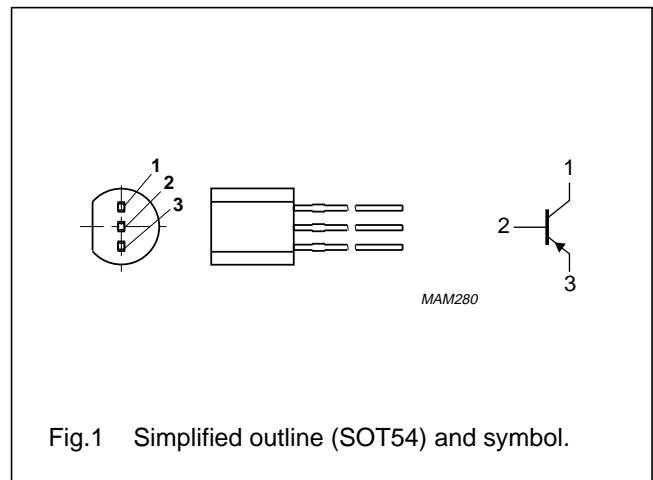
TYPE NUMBER	MARKING CODE
PBSS5350SA	5350SA

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	-50	V
I_C	collector current (DC)	-2	A
I_{CRP}	repetitive peak collector current	-3	A
R_{CEsat}	equivalent on-resistance	135	m Ω

PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter



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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–50	V
V_{CEO}	collector-emitter voltage	open base	–	–50	V
V_{EBO}	emitter-base voltage	open collector	–	–5	V
I_C	collector current (DC)		–	–2	A
I_{CRP}	repetitive peak collector current	note 1	–	–3	A
I_{CM}	peak collector current	single peak	–	–5	A
I_B	base current (DC)		–	–0.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 2	–	830	mW
		$T_{amb} \leq 25\text{ °C}$; note 3	–	900	mW
		$T_{amb} \leq 25\text{ °C}$; notes 1 and 2	–	1.2	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Operated under pulsed conditions: pulse width $t_p \leq 100\text{ ms}$; duty cycle $\delta \leq 0.25$.
2. Device mounted on a printed-circuit board; single sided copper; tinplated; standard footprint.
3. Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector 1 cm^2 .

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air; notes 1 and 2	104	K/W
		in free air; note 3	127	K/W
		in free air; note 2	150	K/W

Notes

1. Operated under pulsed conditions: pulse width $t_p \leq 100\text{ ms}$; duty cycle $\delta \leq 0.25$.
2. Device mounted on a printed-circuit board; single sided copper; tinplated; standard footprint.
3. Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector 1 cm^2 .

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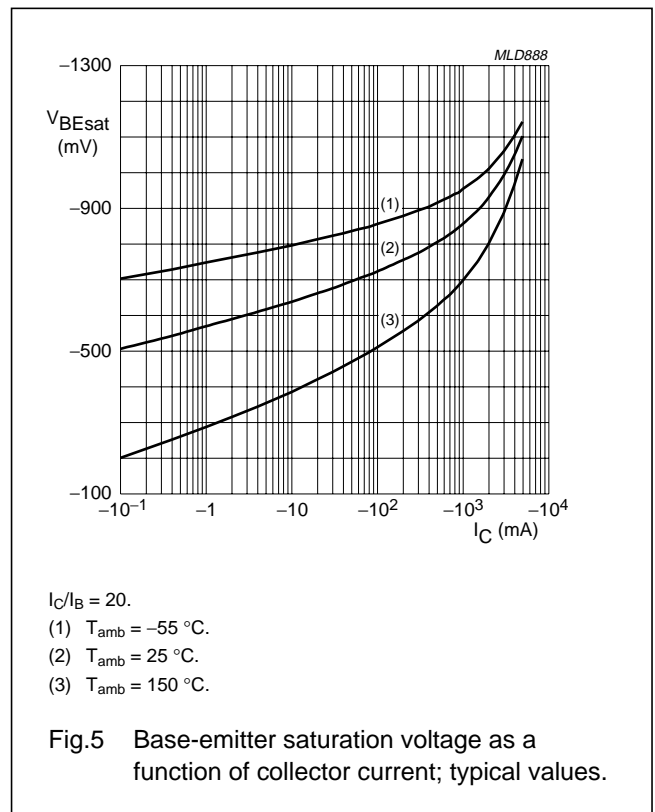
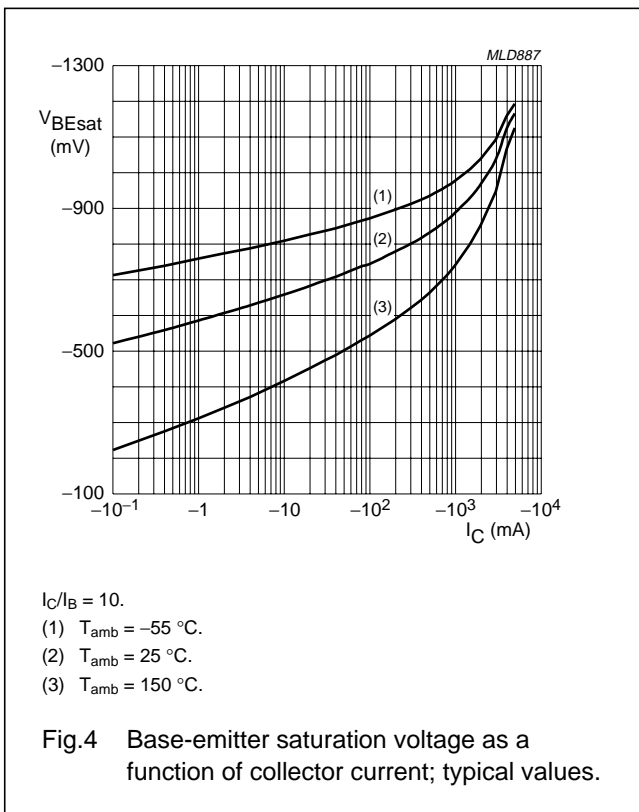
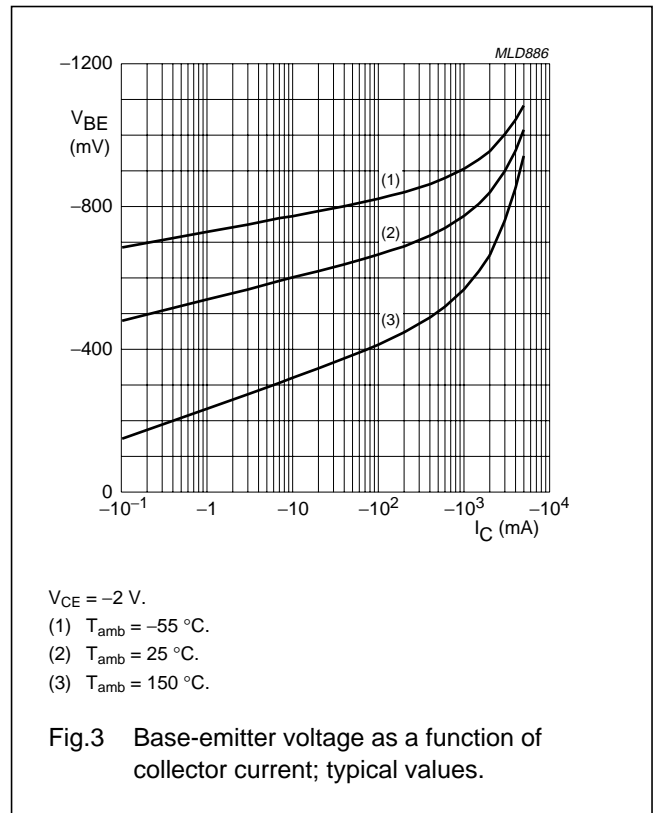
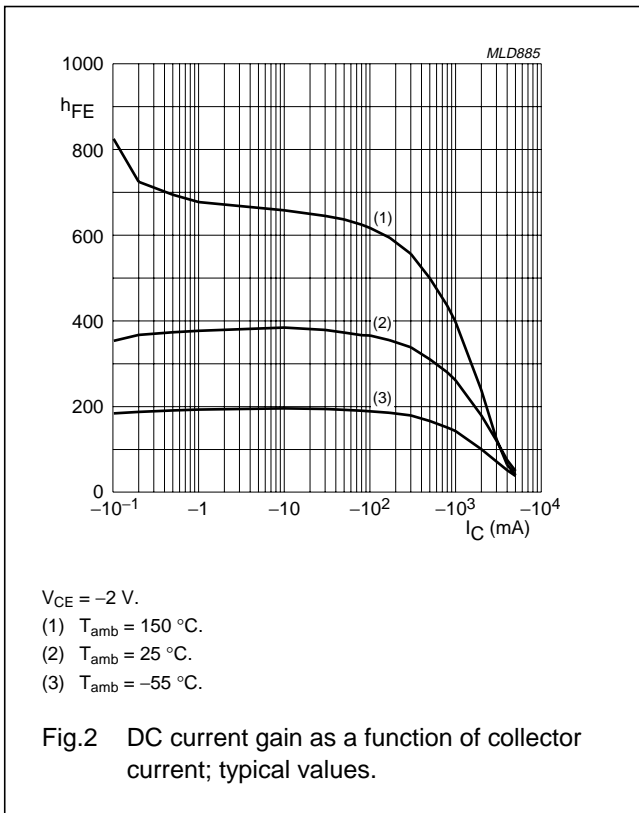
CHARACTERISTICS $T_{amb} = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = -50\text{ V}; I_E = 0$	–	–	–100	nA
		$V_{CB} = -50\text{ V}; I_E = 0; T_j = 150\text{ °C}$	–	–	–50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0$	–	–	–100	nA
h_{FE}	DC current gain	$V_{CE} = -2\text{ V}; I_C = -100\text{ mA}$	200	–	–	
		$V_{CE} = -2\text{ V}; I_C = -500\text{ mA}$	200	–	–	
		$V_{CE} = -2\text{ V}; I_C = -1\text{ A}; \text{note 1}$	200	–	–	
		$V_{CE} = -2\text{ V}; I_C = -2\text{ A}; \text{note 1}$	130	–	–	
		$V_{CE} = -2\text{ V}; I_C = -3\text{ A}; \text{note 1}$	80	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	–	–	–90	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	–	–	–180	mV
		$I_C = -2\text{ A}; I_B = -100\text{ mA}; \text{note 1}$	–	–	–320	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	–	–270	mV
		$I_C = -3\text{ A}; I_B = -300\text{ mA}; \text{note 1}$	–	–	–390	mV
R_{CEsat}	equivalent on-resistance	$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	90	135	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = -2\text{ A}; I_B = -100\text{ mA}; \text{note 1}$	–	–	–1.1	V
		$I_C = -3\text{ A}; I_B = -300\text{ mA}; \text{note 1}$	–	–	–1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -1\text{ A}; \text{note 1}$	–	–	–1.2	V
f_T	transition frequency	$I_C = -100\text{ mA}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	100	–	–	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	–	–	35	pF

Note1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

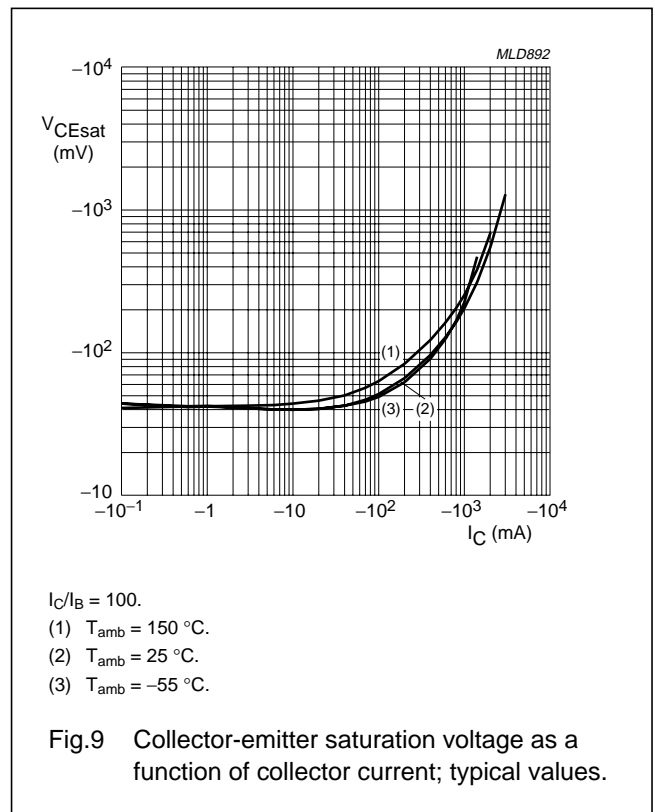
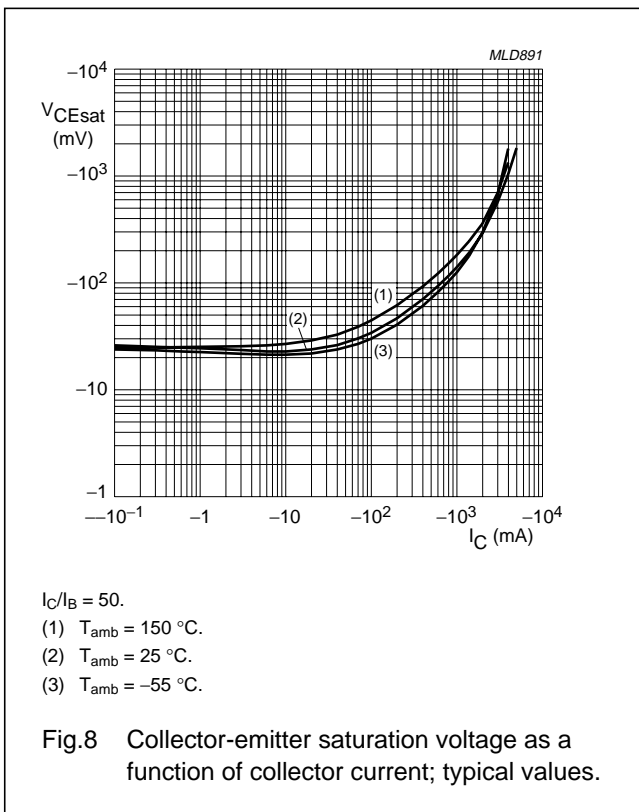
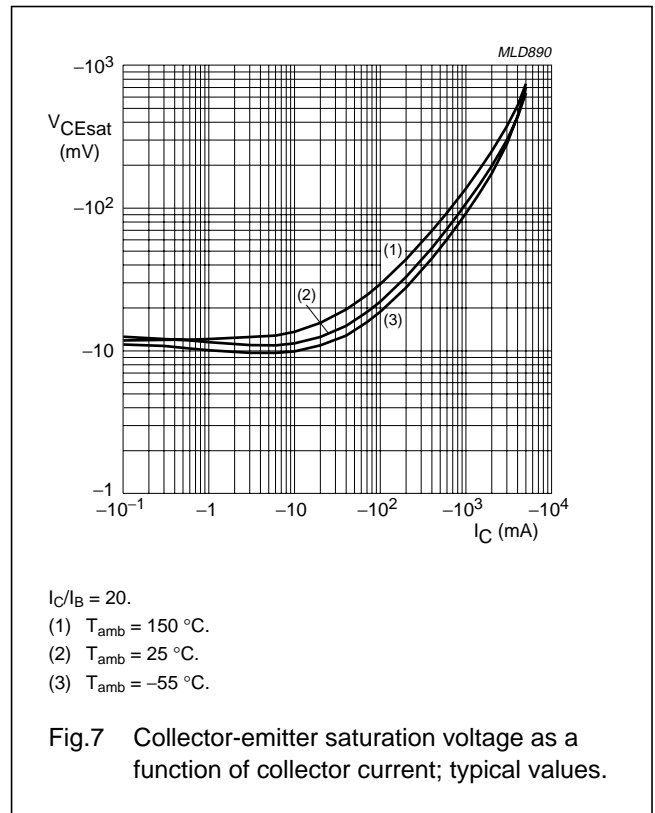
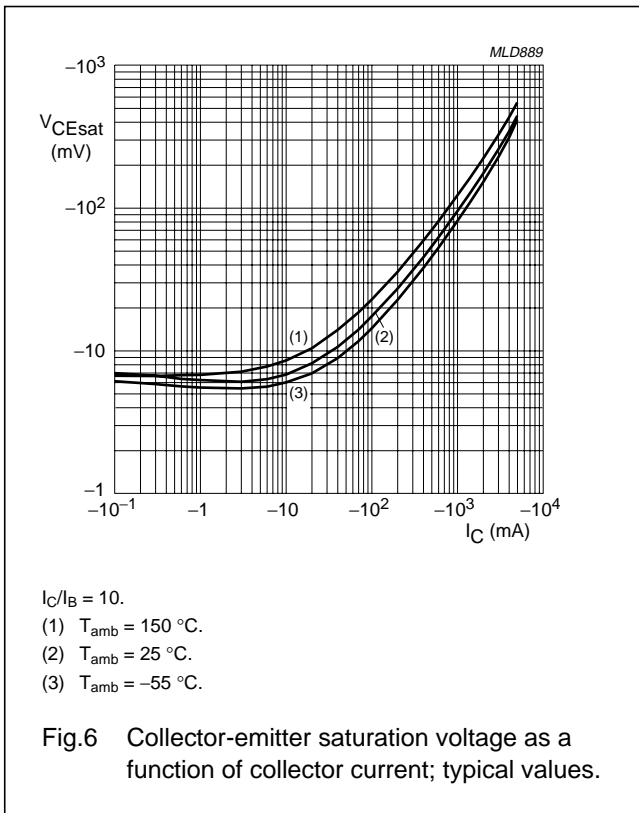
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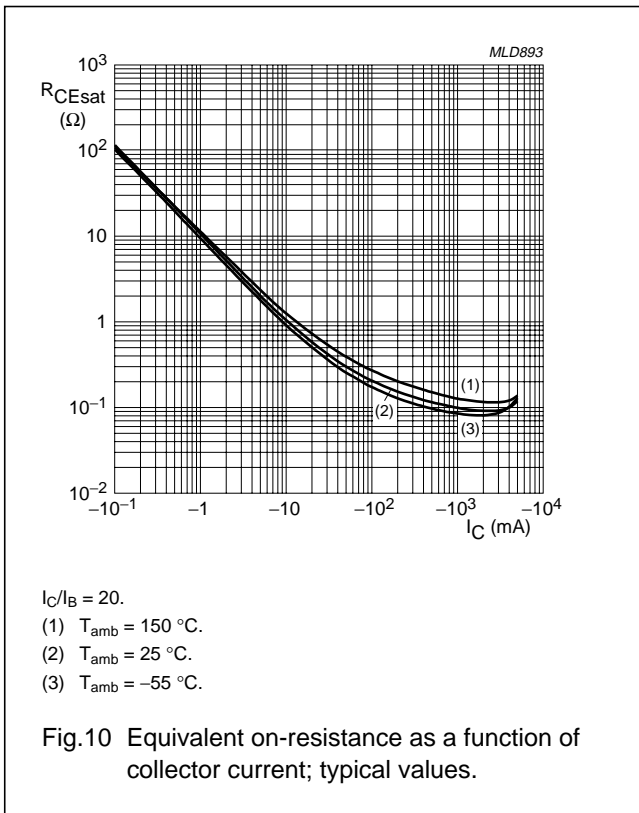
50 V low V_{CEsat} PNP transistor

PBSS5350SA



50 V low V_{CEsat} PNP transistor

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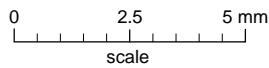
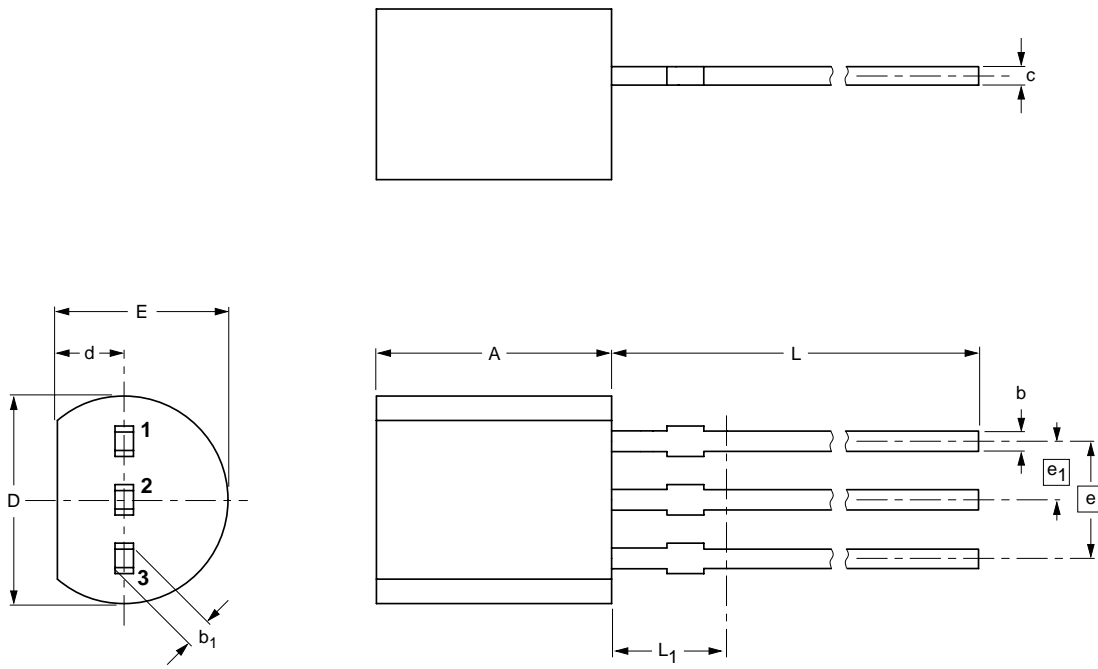
50 V low V_{CEsat} PNP transistor

PBSS5350SA

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		-97-02-28 04-06-28

50 V low V_{CEsat} PNP transistor

PBSS5350SA

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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