CATALYST

CAT24WC164
16K-Bit Serial EEPROM, Cascadable

HALOGEN FREE / LEAD FREE™

FEATURES

- 400 kHz I²C bus compatible*
- 1.8 to 6.0 volt operation
- Low power CMOS technology
- Write protect feature
  - Entire array protected when WP at V_{IH}
- Page write buffer

- Self-timed write cycle with auto-clear
- 1,000,000 program/erase cycles
- 100 year data retention
- 8-pin DIP, 8-pin SOIC, 8-pin MSOP or 8 pin TSSOP

  (Also available in "Green" packages)
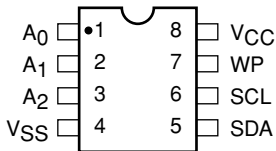- Industrial, automotive and extended temperature ranges

DESCRIPTION

The CAT24WC164 is a16K-bit, cascadable Serial CMOS EEPROM internally organized as 2048 words of 8 bits each. Catalyst's advanced CMOS technology substantially reduces device power requirements. The
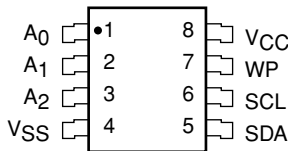
CAT24WC164 features a 16-byte page write buffer. The device operates via the I²C bus serial interface, has a special write protection feature, and is available in 8-pin DIP, 8-pin SOIC, 8-pin TSSOP and 8-lead MSOP.

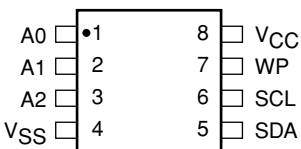## PIN CONFIGURATION

DIP Package (P, L)

A0	1	8	V_{CC}
A1	2	7	WP
A2	3	6	SCL
V_{SS}	4	5	SDA

SOIC Package (J, W)

A0	1	8	V_{CC}
A1	2	7	WP
A2	3	6	SCL
V_{SS}	4	5	SDA

5020 FHD F01

MSOP Package (R, Z)

A0	1	8	V_{CC}
A1	2	7	WP
A2	3	6	SCL
V_{SS}	4	5	SDA

TSSOP Package (U, Y)

A0	1	8	V_{CC}
A1	2	7	WP
A2	3	6	SCL
V_{SS}	4	5	SDA

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{CC}	+1.8V to +6.0V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM
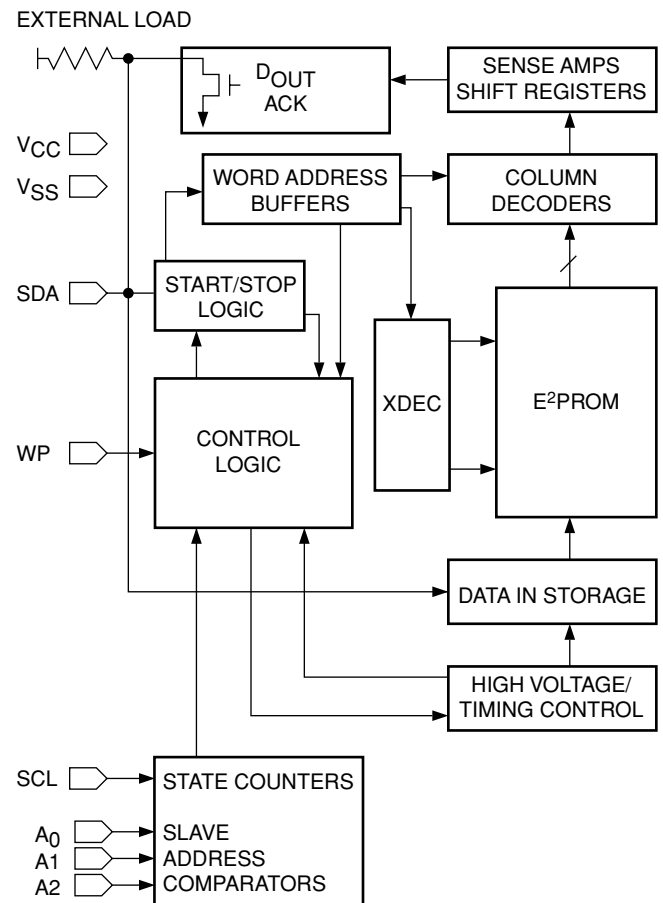
* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

Doc. No. 1026, Rev. H

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... –55°C to +125°C

Storage Temperature .... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground[1] .... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .... –2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C).................................. 1.0W

Lead Soldering Temperature (10 secs) .... 300°C

Output Short Circuit Current[2] 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Typ	Max	Units
N_{END}[3]	Endurance	MIL-STD-883, Test Method 1033	1,000,000			Cycles/Byte
T_{DR}[3]	Data Retention	MIL-STD-883, Test Method 1008	100			Years
V_{ZAP}[3]	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			Volts
I_{LTH}[3][4]	Latch-up	JEDEC Standard 17	100			mA

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	f_{SCL} = 100 kHz			3	mA
I_{SB}[5]	Standby Current (V_{CC} = 5.0V)	V_{IN} = GND or V_{CC}			1	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			10	μA
V_{IL}	Input Low Voltage		–1		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage (V_{CC} = 3.0V)	I_{OL} = 3 mA			0.4	V
V_{OL2}	Output Low Voltage (V_{CC} = 1.8V)	I_{OL} = 1.5 mA			0.5	V

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$C_{I/O}$[3]	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V			8	pF
C_{IN}[3]	Input Capacitance (A0, A1, A2, SCL, WP)	V_{IN} = 0V			6	pF

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Maximum standby current (I_{SB}) = 10μA for the Automotive and Extended Automotive temperature range.

A.C. CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	1.8 V - 6.0 V		2.5 V - 6.0 V		
		Min	Max	Min	Max	Units
F_{SCL}	Clock Frequency		100		400	kHz
T_I[1]	Noise Suppression Time Constant at SCL, SDA Inputs		200		200	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5		1	µs
t_{BUF}[1]	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.2		µs
t_{HIGH}	Clock High Period	4		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	50		50		ns
t_R[1]	SDA and SCL Rise Time		1		0.3	µs
t_F[1]	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4		0.6		µs
t_{DH}	Data Out Hold Time	100		100		ns

Power-Up Timing[1][2]

Symbol	Parameter	Min	Typ	Max	Units
t_{PUR}	Power-up to Read Operation			1	ms
t_{PUW}	Power-up to Write Operation			1	ms

Write Cycle Limits

Symbol	Parameter	Min	Typ	Max	Units
t_{WR}	Write Cycle Time			5	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24WC164 supports the I²C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. Data transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24WC164 operates as a Slave device. Both the Master and Slave devices can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum of 8 devices may be connected to the bus as determined by the device address inputs A0, A1, and A2.

PIN DESCRIPTIONS

SCL: Serial Clock
The CAT24WC164 serial clock input pin is used to clock all data transfers into or out of the device. This is an input pin.

SDA: Serial Data/Address
The CAT24WC164 bidirectional serial data/address pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs
These inputs set device address when cascading multiple devices. When these pins are left floating the default values are zeros.

A maximum of eight devices can be cascaded. If only one CAT24WC164 is addressed on the bus, all three

Figure 1. Bus Timing
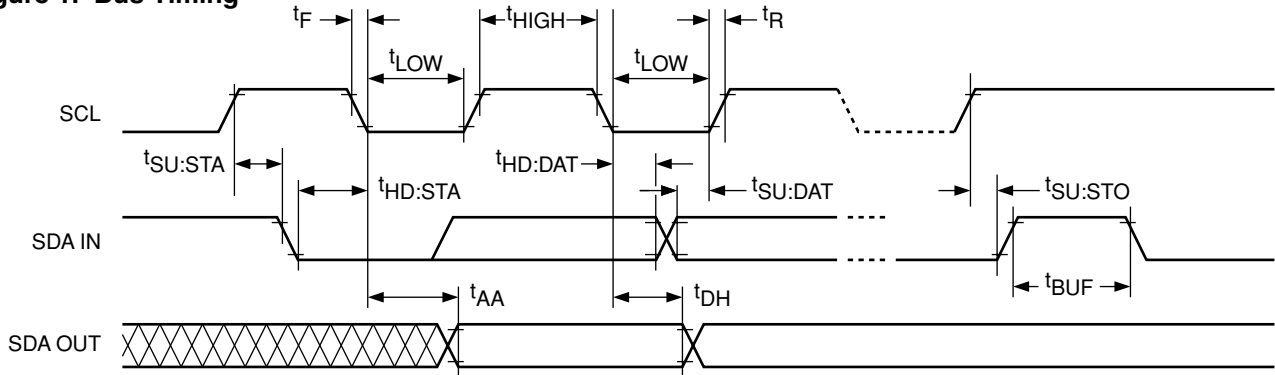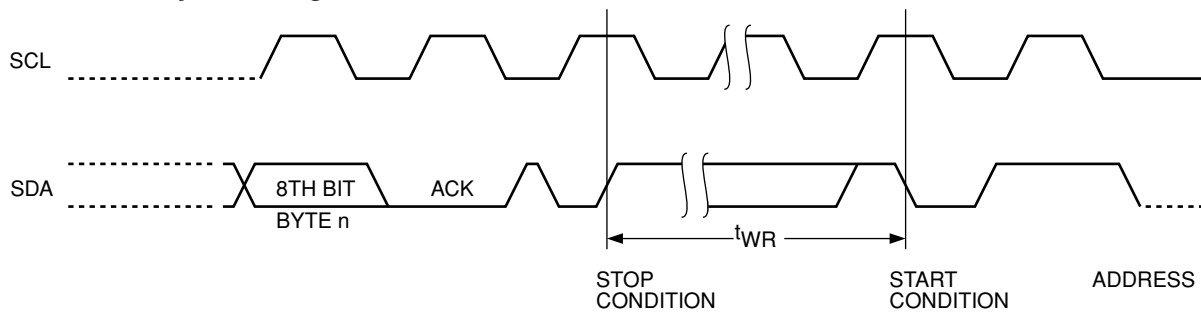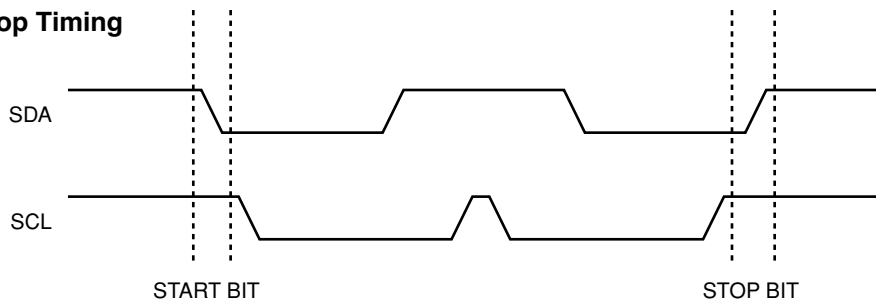

Figure 2. Write Cycle Timing

Figure 3. Start/Stop Timing

address pins (A0, A1and A2) can be left floating or connected to V$_{SS}$.

The CAT24WC164 can be made compatible with the CAT24WC16 by tying A2, A1 and A0 to VSS or by leaving A2, A1 and A0 float.

WP: Write Protect
If the WP pin is tied to V$_{CC}$ the entire memory array becomes Write Protected (READ only). When the WP pin is tied to V$_{SS}$ or left floating normal read/write operations are allowed to the device.

I^{2}C BUS PROTOCOL

The following defines the features of the I^{2}C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24WC164 monitor the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The most significant bit of the 8-bit slave address is fixed as 1. (see Fig. 5). The next three significant bits (A2, A1, A0) are the device address bits and define which device or which part of the device the Master is accessing (The A1 bit must be the compliment of the A1 input pin signal). Up to eight CAT24WC164 devices may be individually addressed by the system. The next three bits are used as the three most significant bits of the data word address. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT24WC164 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24WC164 then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT24WC164 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

Figure 4. Acknowledge Timing
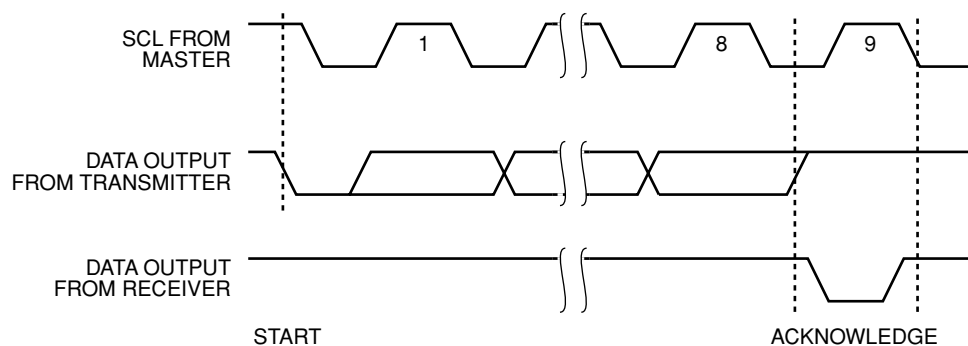
When the CAT24WC164 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24WC164 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the remainder of the byte address that is to be written into the address pointer of the CAT24WC164. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24WC164 acknowledge once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24WC164 writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to fifteen additional bytes. After each byte has been transmitted the CAT24WC164 will respond with an acknowledge, and internally increment the low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than sixteen bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all sixteen bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24WC164 in a single write cycle.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24WC164 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24WC164 is still busy with the write operation, no ACK will be returned. If the CAT24WC164 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

The Write Protection feature allows the user to protect against inadvertent programming of the memory array. If the WP pin is tied to V_{CC}, the entire memory array is protected and becomes read only. The CAT24WC164 will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device's failure to send an acknowledge after the first byte of data is received.

Figure 5. Slave Address Bits

CAT24WC164	1	A2	$\overline{A1}$	A0	a10	a9	a8	R/$\overline{W}$
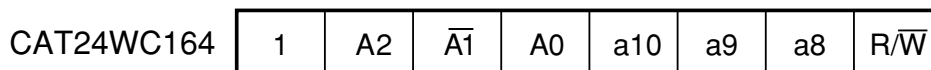
**   a8, a9 and a10 correspond to the address of the memory array address word.
***   A0, $\overline{A1}$ and A2 must compare to its corresponding hard wired input pins (pins 1, 2 and 3).

READ OPERATIONS

The READ operation for the CAT24WC164 is initiated in the same manner as the write operation with the one exception that the R/W̄ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The device address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=2047, then the counter will 'wrap around' to addrss 0 and continue to clock out data.

After the CAT24WC164 receives its slave address information (with the R/W̄ bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24WC164 acknowledge the word address, the Master device resends the START condition

and the slave address, this time with the R/W̄ bit set to one. The CAT24WC164 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the immediate Address READ or Selective READ operations. After the CAT24WC164 sends initial 8-bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24WC164 will continue to output an 8-bit byte for each acknowledge sent by the Master. The operation is terminated when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT24WC164 is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24WC164 address bits so that the entire memory array can be read during one operation. If more than the 2047 bytes are read out, the counter will "wrap around" and continue to clock out data bytes.
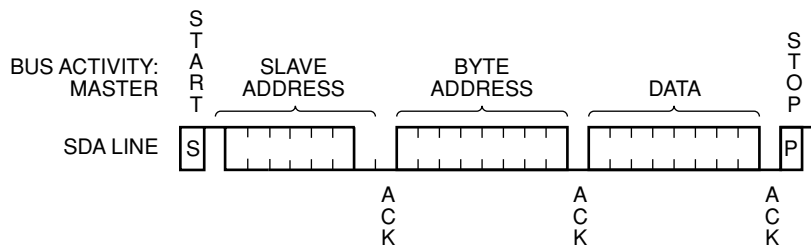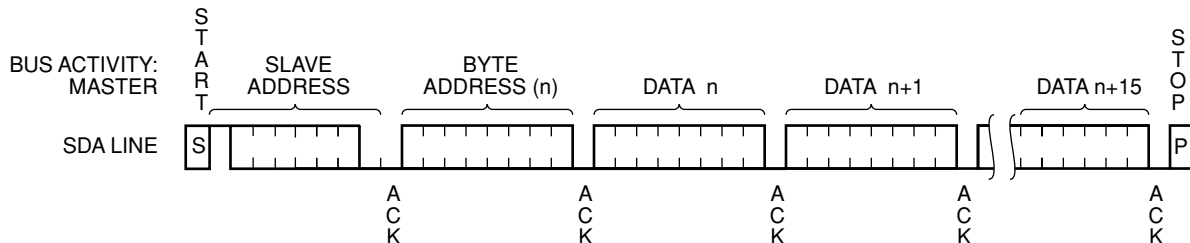
Figure 6. Byte Write Timing

Figure 7. Page Write Timing

NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0
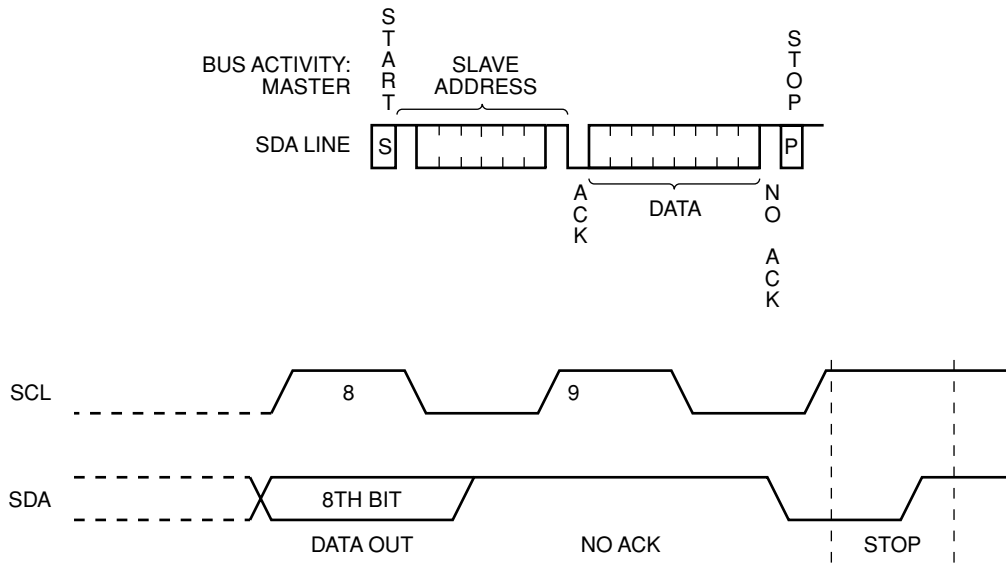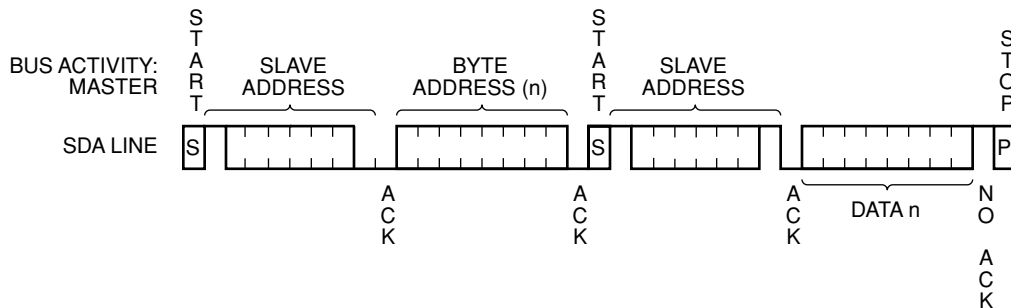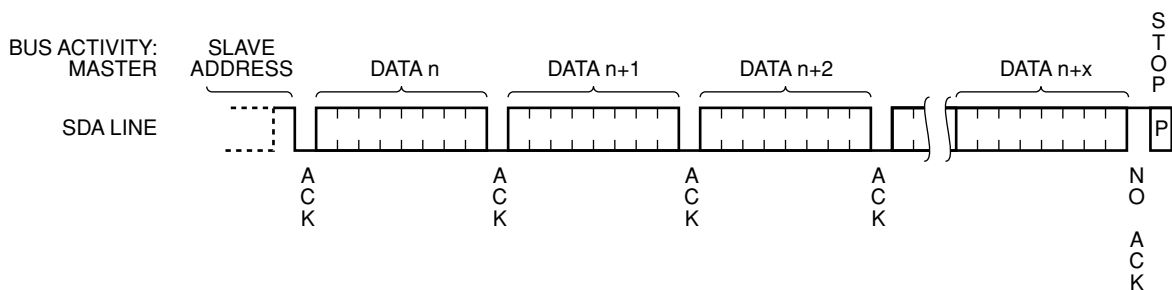
Figure 8. Immediate Address Read Timing

BUS ACTIVITY:
MASTER

START

SLAVE
ADDRESS

STOP

SDA LINE

S

ACK

DATA

NO
ACK

P

SCL

8

9

SDA

8TH BIT

DATA OUT

NO ACK

STOP

Figure 9. Selective Read Timing

BUS ACTIVITY:
MASTER

START

SLAVE
ADDRESS

BYTE
ADDRESS (n)

START

SLAVE
ADDRESS

STOP

SDA LINE

S

ACK

ACK

S

ACK

DATA n

NO
ACK

P

Figure 10. Sequential Read Timing

BUS ACTIVITY:
MASTER

SLAVE
ADDRESS

DATA n

DATA n+1

DATA n+2

DATA n+x

STOP

SDA LINE

ACK

ACK

ACK

ACK

NO
ACK

P

ORDERING INFORMATION

Prefix	Device #	Suffix

CAT   24WC164   J   I   -1.8   TE13   Rev F[2]

Optional Company ID

Product Number
24WC164: 16K

Temperature Range
I = Industrial (-40˚ to 85˚C)
A = Automotive (-40˚ to 105℃)*
E = Extended (-40˚ to 125℃)

Tape & Reel
TE13: 2000/Reel

Die Revision

Package
P: PDIP
J: SOIC (JEDEC)
U: TSSOP
R: MSOP
L: PDIP (Lead free, Halogen free)
W: SOIC (Lead free, Halogen free)
Y: TSSOP (Lead free, Halogen free)
Z: MSOP (Lead free, Halogen free)

Operating Voltage
Blank: 2.5V - 6.0V
1.8: 1.8V - 6.0V

Notes:
(1) The device used in the above example is a CAT24WC164JI-1.8TE13 (SOIC, Industrial Temperature, 1.8 Volt to 6 Volt Operating Voltage, Tape & Reel).
(2) Product die revision letter is marked on top of the package as a suffix to the production date code (e.g. AYWWF). For additional information, please contact your Catalyst sales office.

REVISION HISTORY

Date	Rev.	Reason
12/29/2003	F	Added 8-pin MSOP package to Features section
		Deleted 2.5V - 6.0V from AC Characteristics
		Changed 4.5V - 5.5V to 2.5V - 6.0V in AC Characteristics
		Changed max to 5 in Write Cycle Limits (t_{WR})
		Added overbar to A1 in Figure 5 (slave address bits)
7/23/2004	G	Added die revision to Ordering Information
8/3/2004	H	Update DC Operating Characteristics table & notes

CATALYST