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Errata: CS44600 Rev. A

Rev. A Silicon (Reference CS44600 Datasheet revision DS633A3)

- In SPI control port mode, during write operations, the CDOUT pin does not stay in the HI-Z state, but instead drives high or low. This is not a concern for systems where the CS44600 is the only slave device on the SPI bus. However, this will cause bus contention in systems where the CDOUT signal is shared between multiple slave devices.

  This will operate as per the datasheet in rev B.

  I²C control port mode operates as stated in the datasheet.

- When GPIO[3:0] are configured as edge trigger inputs (as set in the GPIO Pin Level/Edge Trigger register, address 2Eh) and an edge event occurs, the GPIO status will not be cleared after a read of the GPIO Status register (address 2Fh) unless the affected GPIO has had its interrupt unmasked (as set in the GPIO Interrupt Mask register, address 30h). Therefore, if edge sensitivity is needed for GPIO[3:0], the corresponding interrupt should be unmasked, regardless if interrupts are being used.

  GPIO[6:4] operate as described in the data sheet.

  This will operate as per the datasheet in rev B.

- When the minimum PWM output pulse width is set to a non-zero value (as set in the Minimum PWM Output Pulse Width register, address 32h), the power down output mode is set to 1 (as set in the Clock Configuration and Power Control register, address 02h), and the PWM channel is powered down (as set in the PWM Channel Power Down Control register, address 03h), pulses will be output on the powered down channel's inverted output (PWMOUTxx-). The pulse width will be equivalent to the MIN_PULSE[4:0] setting.

  Power down output is correct if the minimum PWM output pulse width is set to 0 or the power down output mode is set to 0.

  This will operate as per the datasheet in rev B.

- The inverted PWM outputs (PWMOUTxx-) can go low at the beginning of a ramp-up sequence regardless of the power down output mode setting (as set in the Clock Configuration and Power Control register, address 02h).

  This will operate as per the datasheet in rev B.

- The Channel Output Configuration bits (A1/B1_OUT_CNFG, A2/B2_OUT_CNFG, A3_OUT_CNFG, and B3_OUT_CNFG) in the PWM Configuration Register (address 31h) work as defined in the datasheet for PSR feedback, however these bits are transposed for ramp-up/down functionality. Therefore, these bits should all be set to the same value.

  This will operate as per the datasheet in rev B.

- It is not recommended to continuously read (poll) the Interrupt Status register (address 2Ah) for updates. Continued read operations to the Interrupt Status register may cause an invalid event status to be reported. The recommended method to check event status is to enable the register bits to generate an interrupt (using the Interrupt Mode Control register, address 28h, and the Interrupt Mask register, address 29h). Once the interrupt has been issued by the CS44600 to the host controller, perform a read operation to the Interrupt Status register.

  This will operate as per the datasheet in rev B.

- When using the internal oscillator, performance is degraded as compared to using an external clock source.

  This will operate as per the datasheet in rev B.

- The CS44600 rev A meets the JESD22-114 (Human Body Model) and JESD22-115 (Machine Model) specifications for ESD. However, for proper operation, the voltage used for the control port (VLC) must be set to a maximum of 2.5 V. A level shifter must be used to interface 3.3 V or 5.0 V control logic with the CS44600 rev A control port operating at 2.5 V.

  This will operate as per the datasheet in rev B.