



SANYO Semiconductors

DATA SHEET

LV8095LQ — Bi-CMOS IC For VCMs Constant-current Driver IC

Overview

The LV8095LQ is a constant current driver IC for voice coil motors. It supports I²C control and integrates a digital/analog converter (DAC).

Its ultraminiature package makes the IC ideal for constant-current driving the voice coil motors (AF and ZM) used in a wide variety of portable equipment including camera cell-phones.

Features

- Constant current driver for voice coil motors.
- I²C bus control supported.
- No external capacitors needed (capacitor-less).
- Ultraminiature package (USLP8 : 2.0×1.3×0.56mm) for easy soldering.
- Built-in thermal protection circuit.
- Built-in voltage drop protection circuit.
- Constant current control enabled by DAC (8 bits).
- Wide operating voltage range (2.5 to 5.5V).

Specifications

Absolute Maximum Ratings at T_a = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		-0.3 to +5.5	V
Maximum VDD voltage	V _{DD} max		-0.3 to +5.5	V
Output voltage	V _{OUT} max	OUT1	-0.3 to +6.0	V
Input voltage	V _{IN} max	SCL, SDA, PD	-0.3 to +5.5	V
GND pin source current	I _{GND}		200	mA
Allowable power dissipation	P _d max	*Mounted on a specified board.	650	mW
Operating temperature	T _{opr}		-30 to +85	°C
Storage temperature	T _{stg}		-40 to +150	°C

* Specified board : 50mm×40mm×0.8mm, 4-layer glass epoxy circuit board.

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LV8095LQ

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC}		2.5 to 5.0	V
V _{DD} voltage	V _{DD}		1.3 to 5.0	V
Maximum preset output current	I _O		200	mA
High-level input voltage	V _{IH}	Applied to SCL, SDA, and PD pins	0.8×V _{DD} to V _{DD}	V
Low-level input voltage	V _{IL}		-0.3 to 0.2×V _{DD}	V

Electrical Characteristics Ta = 25°C, V_{CC} = 2.8V, V_{DD} = 2.8V

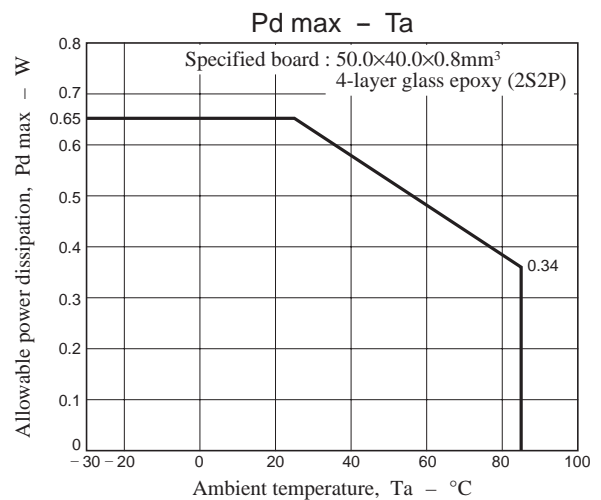
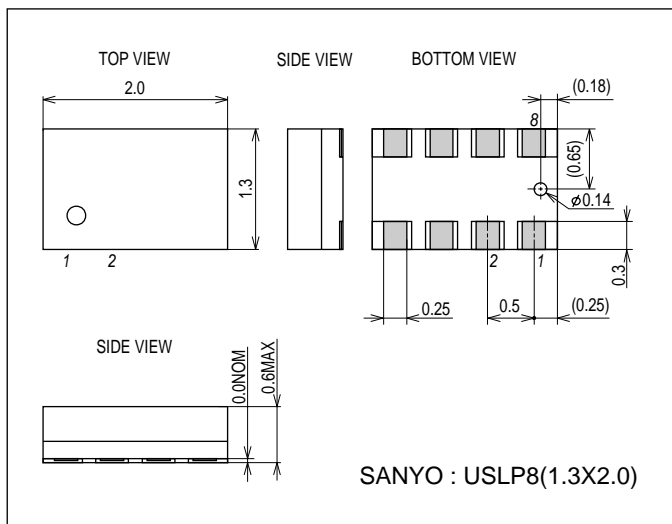
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	I _{CC0}	PD = 0V		0.1	1	μA
	I _{CC1}	PD = 2.8V		0.5	3	mA
Input current	I _{IN}	V _{IN} = 2.8V, V _{ENA} = 2.8V	-1	0	1	μA
Output saturation voltage	V _{sat1}	SW : ON, SW : b, Full code setting, I _{OUT} = 50mA		0.10	0.18	V
	V _{sat2}	SW : ON, SW : b, Full code setting, I _{OUT} = 100mA		0.20	0.4	V
DAC block						
Resolution		RF = 1Ω, SW1 : OFF, SW2 : a		8		bits
Relative accuracy	INL	RF = 1Ω, SW1 : OFF, SW2 : a			±1	LSB
Differential linearity	DNL	RF = 1Ω, SW1 : OFF, SW2 : a			±1	LSB
Full code current	I _{full}	RF = 1Ω, SW1 : OFF, SW2 : a	95	100	105	mA
Error code current 0	I _{zero}	RF = 1Ω, SW1 : OFF, SW2 : a		1	4	mA
Spark killer diode						
Reverse current	I _S (leak)				1	μA
Forward voltage	V _{SF}	I _{OUT} = 200mA *			1.3	V

*1 : Design guaranteed value (no measurement is performed)

Package Dimensions

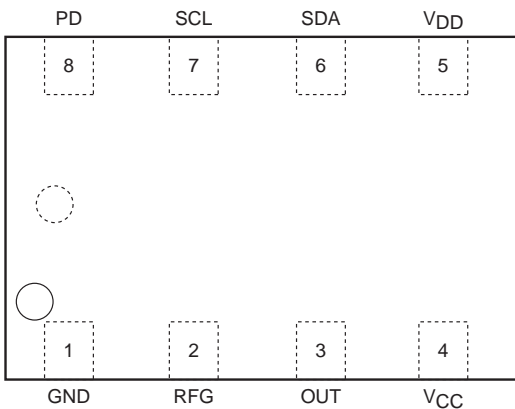
unit : mm (typ)

3348



Pin Assignment

USLP8
(Top View)

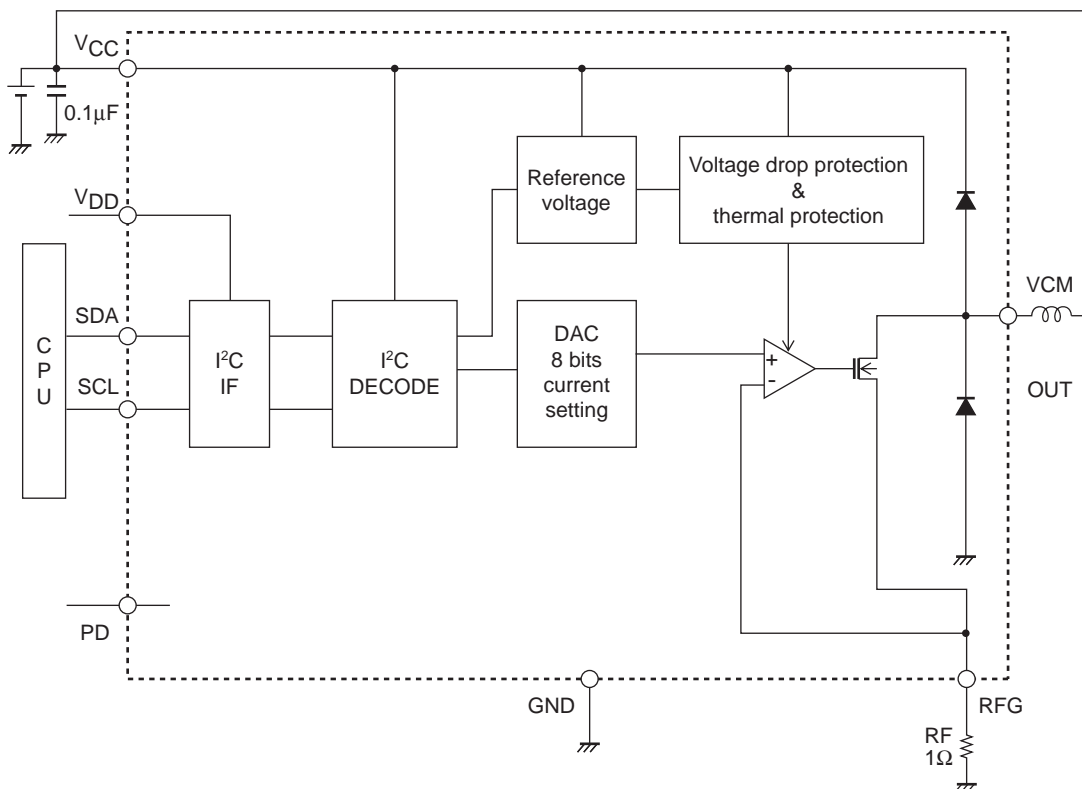


Pin No.	Pin Name	Pin Description
1	GND	Ground
2	RFG	Current sensing resistor connection
3	OUT	Output pin
4	VCC	Analog system power supply
5	VDD	Logic system power supply *1
6	SDA	I ² C SDA input
7	SCL	I ² C SCL input
8	PD	Power-down & reset *2

*1 : The voltage applied to the VDD pin must be set to the same level as those of the SDA, SCL and PD input high-level voltages.

*2 : Setting the PD pin to low level powers down and resets the IC. Set this pin temporarily to low level, then to high level after power-on, and keep it to high level (same voltage level as VDD) during normal operation.

Block Diagram



Wiring resistance (thick line) around the RF is added to the resistance of RF as an error. It must be kept as small as possible.

$$\text{Formula for calculating constant current : } I_{\text{OUT}} = 0.1 \div R_{\text{F}}$$

If, for instance, I_{OUT} is to be set to 100mA max :

$$R_{\text{F}} = 0.1 \div (100\text{mA})$$

$$R_{\text{F}} = 1\Omega$$

Notes on use

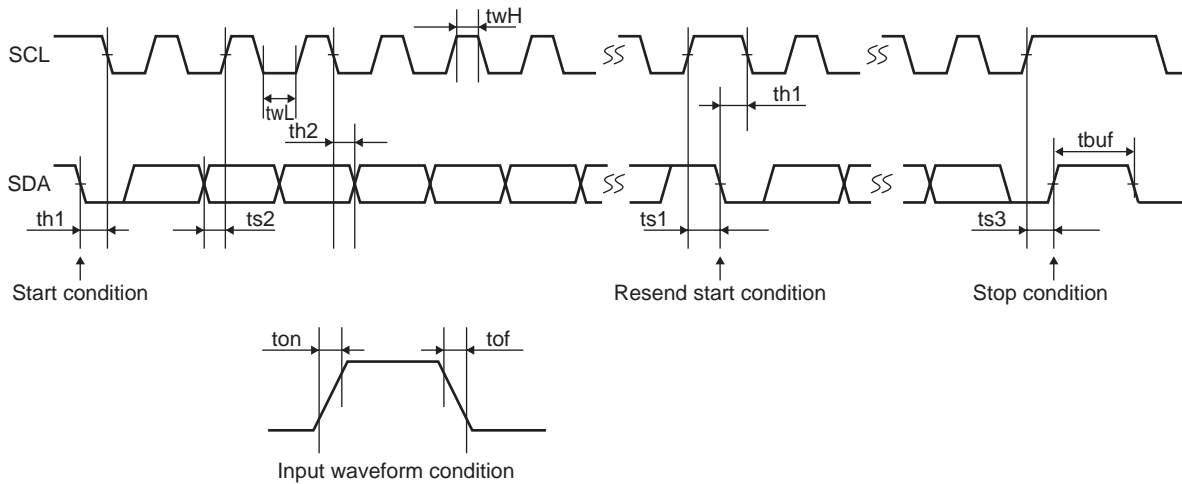
- Determine the preset current value using the resistor between RFG and GND according to the formula above.
- The recommended RF value is 1Ω.

Pin Description

Pin No.	Pin Name	Description	Equivalent Circuit
1	GND	Ground pin	
2 3	RFG OUT	<p>2 : RFG Current detection resistor connection pin The current detection resistor (1Ω) is connected between this pin and GND to detect the output current and perform constant current control.</p> <p>3 : OUT Output pin This is an NMOS open drain output, and the voice coil motor is connected between this pin and the V_{CC} pin for use.</p>	
4 5	V_{CC} V_{DD}	<p>4 : V_{CC} Power supply input pin</p> <p>5 : V_{DD} This is separate from the V_{CC} power supply pin for the SDA, SCL and PD logic input, and it is used while the same voltage as that for the high level of these logic input is applied to it.</p>	
6	SDA	<p>I^2C serial data input pin</p> <p>Input high level : $0.8 \times V_{DD}$ or higher Input low level : $0.2 \times V_{DD}$ or lower</p>	
7 8	SCL PD	<p>7 : SCL 8 : PD Power down and reset When low, power-down and reset is performed at the same time. This pin is held high for normal use. In normal operation, however, this pin must be set low temporarily and an initial reset must be applied after V_{CC} starts up. Input high level : $0.8 \times V_{DD}$ or higher Input low level : $0.2 \times V_{DD}$ or lower</p>	

Serial Bus Communication Specifications

I²C serial transfer timing conditions
Standard mode



Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscL	SCL clock frequency	0		100	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	4.7			μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	250			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	4.0			μs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	4.0			μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0			μs
Pulse width	twL	SCL low period pulse width	4.7			μs
	twH	SCL high period pulse width	4.0			μs
Input waveform conditions	ton	SCL, SDA (input) rising time			1000	ns
	tof	SCL, SDA (input) falling time			300	ns
Bus free time	tbuf	Interval between stop condition and start condition	4.7			μs

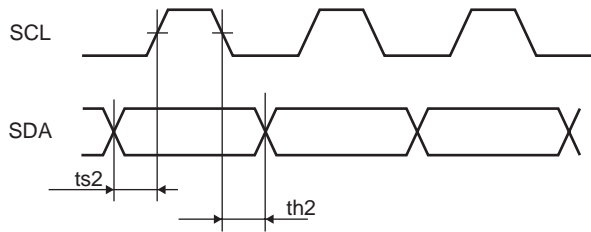
High-speed mode

Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscL	SCL clock frequency	0		400	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	0.6			μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	100			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	0.6			μs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	0.6			μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0			μs
Pulse width	twL	SCL low period pulse width	1.3			μs
	twH	SCL high period pulse width	0.6			μs
Input waveform conditions	ton	SCL, SDA (input) rising time			300	ns
	tof	SCL, SDA (input) falling time			300	ns
Bus free time	tbuf	Interval between stop condition and start condition	1.3			μs

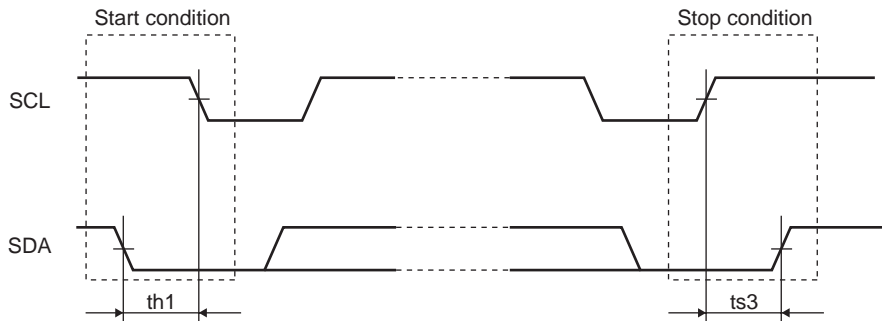
I²C bus transmission method

Start and stop conditions

The I²C bus requires that the state of SDA be preserved while SCL is high as shown in the timing diagram below during a data transfer operation.

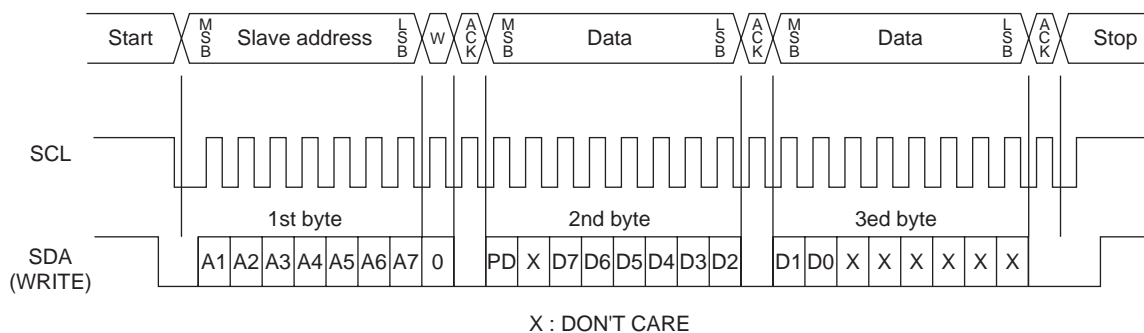


When data is not being transferred, both SCL and SDA are in the high state. The start condition is generated and access is started when SDA is changed from high to low while SCL and SDA are high. Conversely, the stop condition is generated and access is ended when SDA is changed from low to high while SCL is high.



Data transfer and acknowledgement response

After the start condition has been generated, the data is transferred one byte (8 bits) at a time. Generally, in an I²C bus, a unique 7-bit slave address is assigned to each device, and the first byte of the transfer data is allocated to the 7-bit slave address and to the command (R/W) indicating the transfer direction of the subsequent data. However, this IC is provided with only a write mode for receiving the data. Every time 8 bits of data for each byte are transferred, the ACK signal is sent from the receiving end to the sending end. Immediately after the clock pulse of SCL bit 8 in the data transferred has fallen to low, SDA at the sending end is released, and SDA is set to low at the receiving end, causing the ACK signal to be sent. When, after the receiving end has sent the ACK signal, the transfer of the next byte remains in the receiving status, the receiving end releases SDA at the falling edge of the ninth SCL clock.



LV8095LQ

The standard data transfer to this device consists of three bytes : the slave address of the first byte and the data of the second and third bytes.

The table below shows the format of the second and third bytes.

	2nd byte								3rd byte							
Serial data bits	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Function	PD	x	D7	D6	D5	D4	D3	D2	D1	D0	x	x	x	x	x	x

Slave address : 0110011(0)

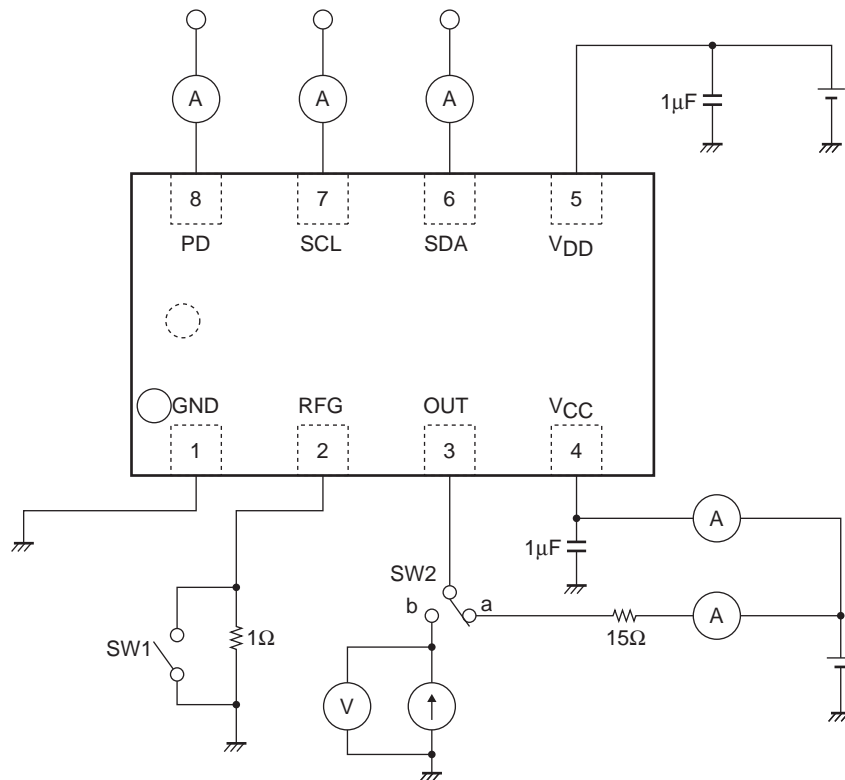
PD : Power-down

D1-D7 : 8-bit data used to set output constant current ; MIN = 00000000, MAX = 11111111

D0-D7 setting method (output current design values assume an RF of 1Ω)

Current setting code	D7	D6	D5	D4	D3	D2	D1	Output setting (LSB)	Output current (mA) (design value)
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1	0.392
2	0	0	0	0	0	1	0	2	0.784
254	1	1	1	1	1	1	0	254	99.608
255	1	1	1	1	1	1	1	255	100

Specified Test Circuit



- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of October, 2007. Specifications and information herein are subject to change without notice.