



CYPRESS

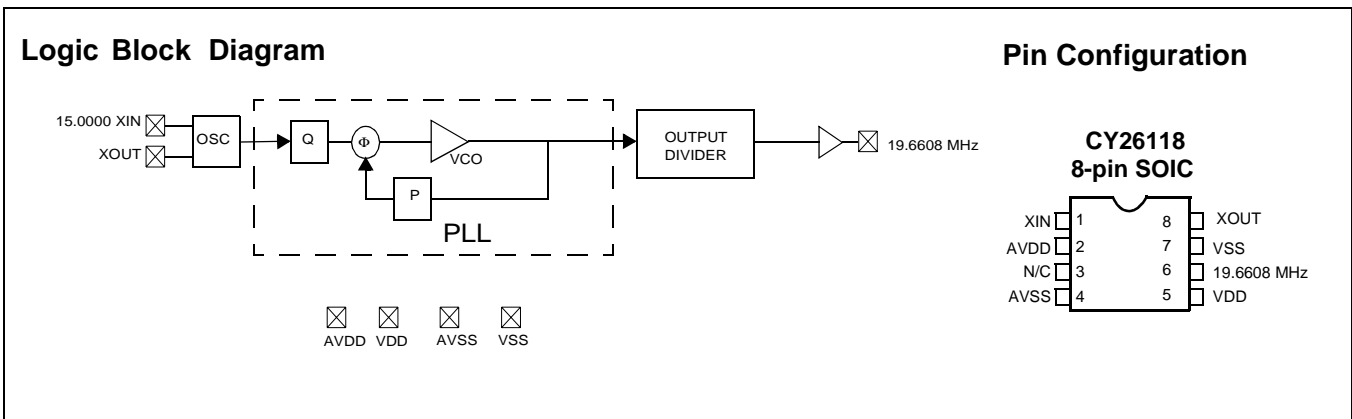
PRELIMINARY

CY26118

# 19.6608-MHz Clock Generator

Features	Benefits
• Integrated phase-locked loop (PLL)	Highest-performance PLL tailored for multimedia applications
• Low-jitter, high-accuracy outputs	Meets critical timing requirements in complex system designs
• 3.3V operation	

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY26118	1	15.0000 MHz	19.6608 MHz



**Pin Summary**

Name	Pin Number	Description
X <sub>IN</sub>	1	15.000 MHz Reference Crystal Input
A <sub>VDD</sub>	2	Analog Voltage Supply
N/C	3	No Connect
A <sub>VSS</sub>	4	Analog Ground
V <sub>DD</sub>	5	Output Voltage Supply
19.6608 MHz	6	19.6608-MHz clock output
V <sub>SS</sub>	7	Output Ground
X <sub>OUT</sub> <sup>[1]</sup>	8	Reference Crystal Output

**Absolute Maximum Conditions**

Parameter	Description	Min.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	-0.5	7.0	V
T <sub>S</sub>	Storage Temperature <sup>[2]</sup>	-65	125	° C
T <sub>J</sub>	Junction Temperature		125	° C
	Digital Inputs	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
	Digital Outputs referred to V <sub>DD</sub>	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
	Electro-Static Discharge		2000	V

**Recommended Operating Conditions**

Parameter	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operating Voltage	3.0	3.3	3.6	V
T <sub>A</sub>	Ambient Temperature	0		70	° C
C <sub>LOAD</sub>	Max Load Capacitance			15	pF
P <sub>max</sub>	Max Output Power Dissipation, 8-pin package			150	° C/W
f <sub>REF</sub>	Reference Frequency		15.000		MHz
t <sub>PU</sub>	Power-up time for all V <sub>DD</sub> 's to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

**DC Electrical Characteristics**

Parameter	Name	Description	Min.	Typ.	Max.	Unit
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.5, V <sub>DD</sub> = 3.3V	12	24		mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.5, V <sub>DD</sub> = 3.3V	12	24		mA
C <sub>IN</sub>	Input Capacitance				7	pF
I <sub>Iz</sub>	Input Leakage Current			5		mA
I <sub>DD</sub>	Supply Current	Sum of Core and Output Current			20	mA

**Notes:**

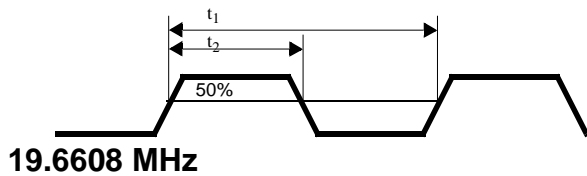
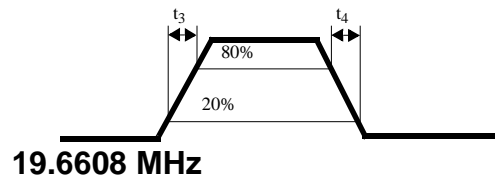
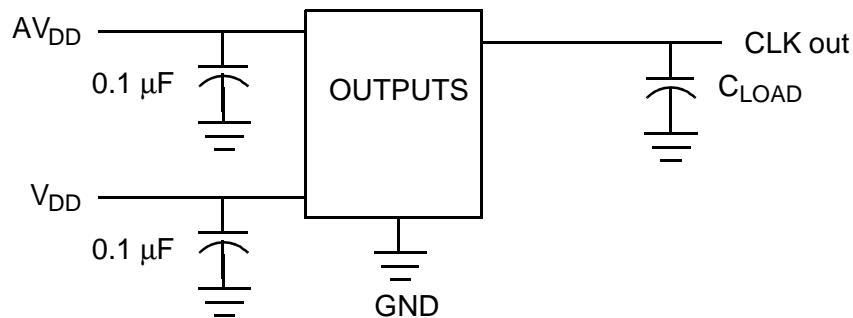
1. Float X<sub>OUT</sub> if X<sub>IN</sub> is externally driven.
2. Rated for 10 years.

**AC Electrical Characteristics ( $V_{DD} = 3.3V$ )**

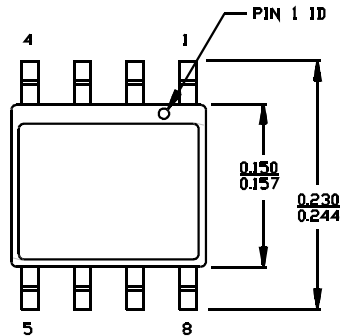
Parameter <sup>[3]</sup>	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> 50% of $V_{DD}$	45	50	55	%
$t_3$	Rising Edge Slew Rate	Output Clock Rise Time 20% - 80% of $V_{DD}$	0.8	1.8		V/ns
$t_4$	Falling Edge Slew Rate	Output Clock Fall Time 80% to 20% of $V_{DD}$	0.8	1.8		V/ns
$t_9$	Clock Jitter	Peak-to-Peak period jitter		200		ps
$t_{10}$	PLL Lock Time				3	ms

**Note:**

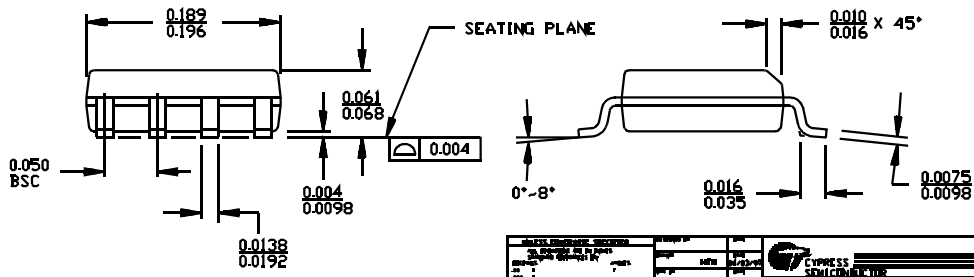
3. Not 100% tested.



**Figure 1. Duty Cycle Definition;  $DC = t_2/t_1$** 

**Figure 2. Rise and Fall Time Definitions**
**Test Circuit**

**Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY26118SC	S8	8-Pin SOIC	Commercial	3.3V

**Pin Diagrams**
**8-Lead (150-Mil) SOIC S8**


1. DIMENSIONS IN INCHES **MIN.**  
**MAX.**
2. PIN 1 ID IS OPTIONAL.  
ROUND ON SINGLE LEADFRAME  
RECTANGULAR ON MATRIX LEADFRAME



DATE ENGINEER	DATE	DESIGN	BY
DATE CHECKED	DATE	DESIGN	BY
DATE APPROVED	DATE	DESIGN	BY
			



<b>Document Title: CY26118 19.6608-MHz Clock Generator</b> <b>Document Number: 38-07274</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	110764	02/06/02	CKN	New Data Sheet
*A	121883	12/14/02	RBI	Power up requirements added to Operating Conditions Information