ELECTRONIC DESIGNS INC.

EDI8M3264C

High Speed Two Megabit SRAM Module

64Kx32 Static RAM CMOS, High Speed Module

The EDI8M3264C is a high speed 2 megabit Static RAM module organized as 64Kx32. This module is constructed from eight 64Kx4 Static RAMs in LCC packages on a multi-layered ceramic substrate.

Four chip selects ($\overline{E0}$-$\overline{E3}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The EDI8M3264C is offered in a 600 mil, 60 pin DIP which enables two megabits of memory to be placed in less than 1.2 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

Military product, incorporating semiconductor components which are compliant to MIL-STD-883, paragraph 1.2.1 is available.

Features

64Kx32 bit CMOS Static Random Access Memory

- Access Times 25, 35, 45, and 55ns
- Individual Byte Selects
- Fully Static, No Clocks
- TTL Compatible I/O

High Density Packaging

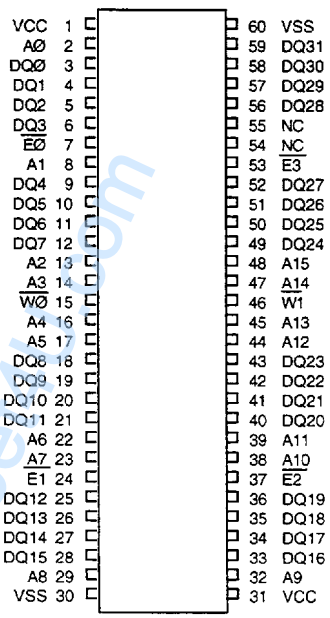
- 60 Pin DIP, No. 69
- Common Data Inputs and Outputs

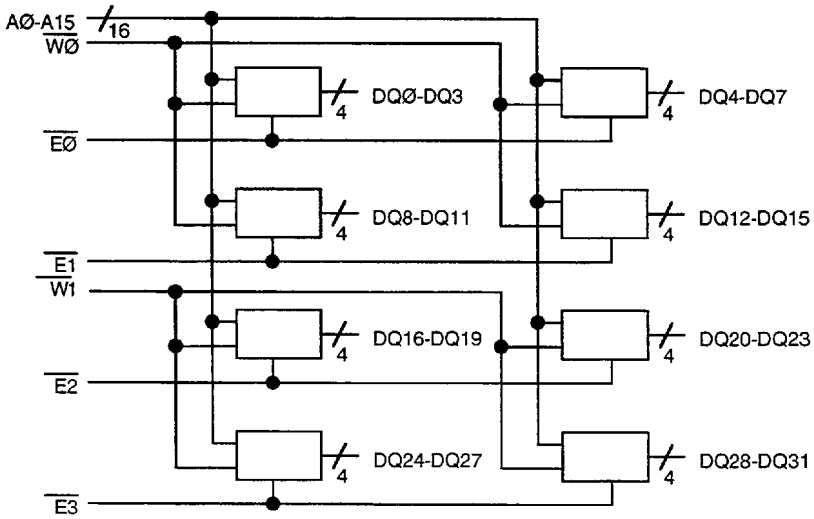
Single +5V (±10%) Supply Operation

Pin Names

$\overline{A0}$-$\overline{A15}$	Address Inputs
$\overline{E0}$-$\overline{E3}$	Chip Enable
$\overline{W}$	Write Enable
DQ0-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Pin Configurations and Block Diagrams





(1)

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Industrial .....-40°C to +85°C
Military. .....-55°C to +125°C
Storage Temperature .....-65°C to +150°C
Power Dissipation..... 1 Watt
Output Current..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times..... 5ns
Input and Output Timing Levels..... 1.5V
Output Load ..... 1TTL, CL = 50pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	--	640	1180	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq$ VIH, VIN $\leq$ VIL or VIN $\geq$ VIH	--	20	280	mA
Full Standby Power Supply Current	ICC3	$\overline{E} \geq$ VCC-0.2V VIN $\geq$ VCC-0.2V or VIN $\leq$ 0.2V	--	10	140	mA
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±5	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	±5	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Standby	HIGH Z	ICC3
L	H	Read	DOUT	ICC1
L	L	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	80	pF
Capacitance Control (DQ Pins)	CD/Q	12	pF
Input Capacitance ($\overline{E}$Ø-$\overline{E3}$)	CC	25	pF
Input Capacitance ($\overline{W}$)	CN	45	pF

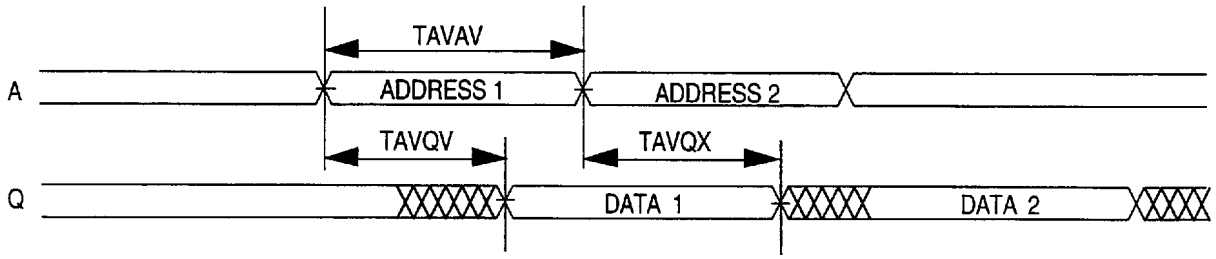
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

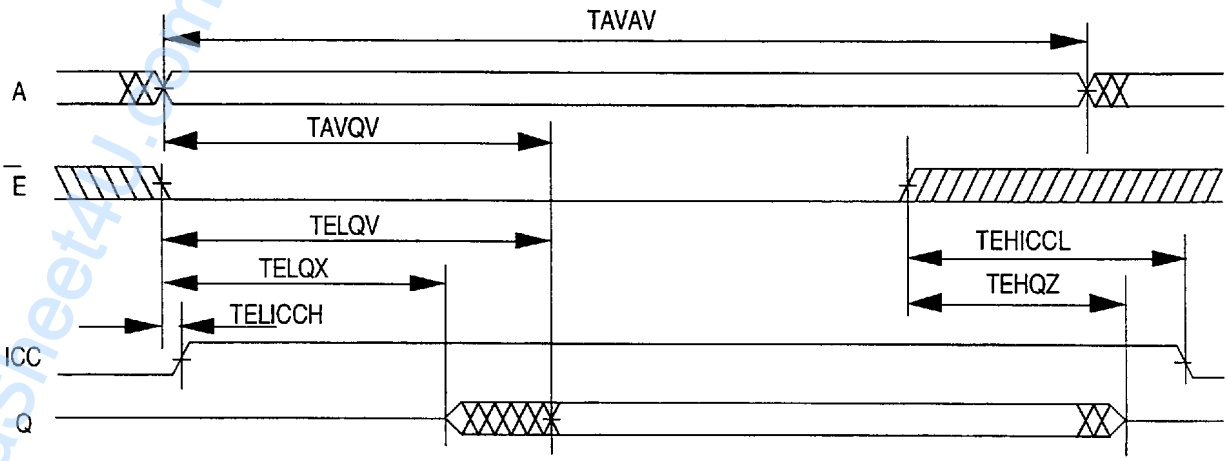
Parameter	Symbol JEDEC	Symbol Alt.		25ns Min	25ns Max	35ns Min	35ns Max	45ns Min	45ns Maz	55ns Min	55ns Max	Units
Read Cycle Time	TAVAV	TRC		25		35		45		55		ns
Address Access Time	TAVQV	TAA			25		35		45		55	ns
Chip Enable Access Time	TELQV	TACS			25		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ		0		0		3		3		ns
Chip Enable to Output in High Z (1)	TEHQZ	TCHZ		0	12	0	15	0	20	0	20	ns
Output Hold from Address Change	TAVQX	TOH		3		3		3		3		ns
Chip Enable to Power Up (1)	TELICCH	TPU		0		0		0		0		ns
Chip Disable to Power Down (1)	TEHICCL	TPD			25		35		45		55	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
W High, E Low



Read Cycle 2
W High

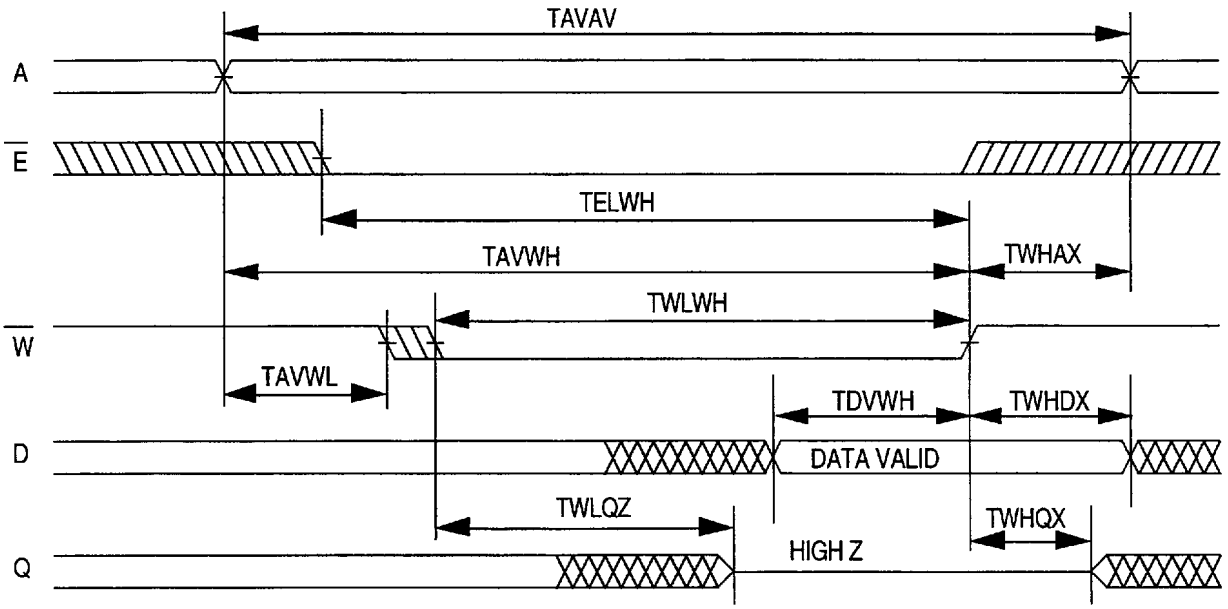


AC Characteristics
Write Cycle

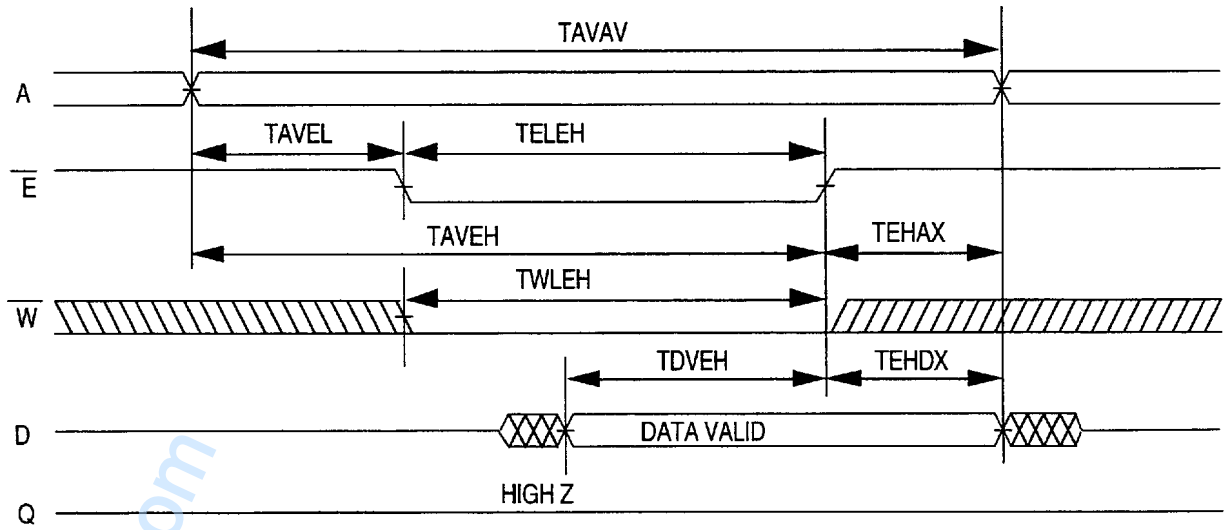
Parameter	Symbol JEDEC	Symbol Alt.		20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	45ns Min	45ns Max	Units
Write Cycle Time	TAVAV	TWC		25		35		45		55		ns
Chip Enable to	TELWH	TCW		20		30		40		55		ns
End of Write	TWLEH	TCW		20		30		40		55		ns
Address Setup Time	TAVWL	TAS		2		2		2		2		ns
	TAVEL	TAS		2		2		2		2		ns
Address Valid to	TAVWH	TAW		20		30		35		40		ns
End of Write	TAVEH	TAW		20		30		35		40		ns
Write Pulse Width	TWLWH	TWP		20		30		35		40		ns
	TELEH	TWP		20		30		35		40		ns
Write Recovery Time	TWHAX	TWR		2		2		2		2		ns
	TEHAX	TWR		2		2		2		2		ns
Data Hold Time	TWHDX	TDH		2		2		2		2		ns
	TEHDX	TDH		2		2		2		2		ns
Write to Output in High Z (1)	TWLQZ	TWHZ		0	12	0	15	0	20	0	20	ns
Data to Write Time	TDVWH	TDW		12		15		20		20		ns
	TDVEH	TDW		12		15		20		20		ns
Output Active from End of Write (1)	TWHQX	TWLZ		3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled

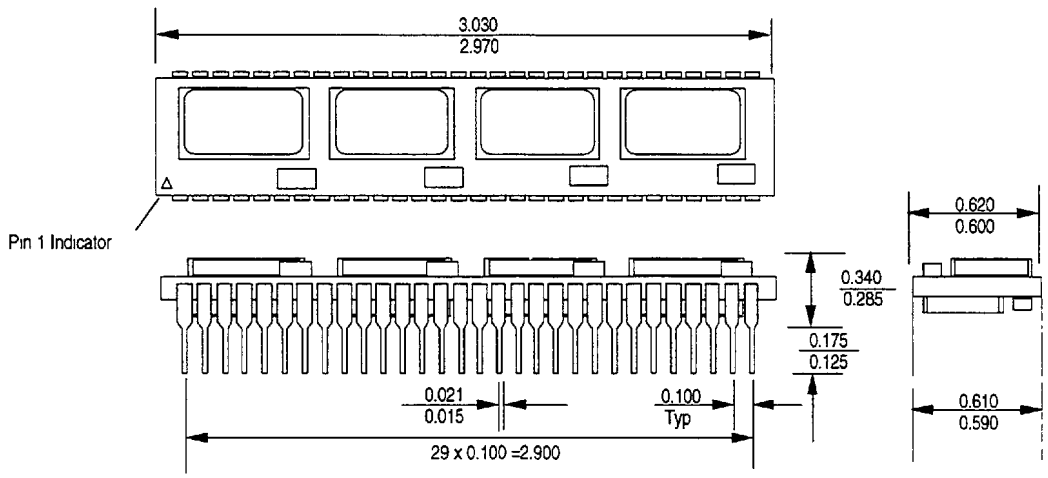


Ordering Information

Part No.	Speed (ns)	Leads	Package Style	No.
EDI8M3264C25C6B	25	60	0.6 DIP	69
EDI8M3264C35C6B	35	60	0.6 DIP	69
EDI8M3264C45C6B	45	60	0.6 DIP	69
EDI8M3264C55C6B	55	60	0.6 DIP	69

Package Description

Package No.69
60 pin DIP,
LCCs on a Ceramic Substrate



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