19-1052; Rev 0; 6/96

MAXIM

# Low-Voltage, SPST, CMOS Analog Switches



## General Description

The MAX4501/MAX4502 are single-pole/single-throw (SPST), low-voltage, single-supply, CMOS analog switches. The MAX4501 is normally open (NO). The MAX4502 is normally closed (NC).

These CMOS switches can operate continuously with a single supply between +2V and +12V. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1.0nA at +25 ℃ or 10nA at +85 ℃.

The digital input has 0.8V and 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply.

## Features

- ♦ **Available in SOT23-5 Package**
- ♦ **+2V to +12V Single-Supply Operation**
- ♦ **Guaranteed On-Resistance: 250Ω at +5V**
- ♦ **Guaranteed Low Off-Leakage Current:**
  **1nA at +25°C**
  **10nA at +85°C**
- ♦ **Guaranteed Low On-Leakage Current:**
  **2nA at +25°C**
  **20nA at +85°C**
- ♦ **Low Charge Injection: 10pC**
- ♦ **Fast Switching Speed: $t_{ON}$ = 75ns, $t_{OFF}$ = 50ns**
- ♦ **TTL/CMOS-Logic Compatible with +5V Supply**

## Applications

Battery-Operated Equipment

Audio and Video Signal Routing

Low-Voltage Data-Acquisition Systems

Communications Circuits

PCMCIA Cards

Cellular Phones

Modems

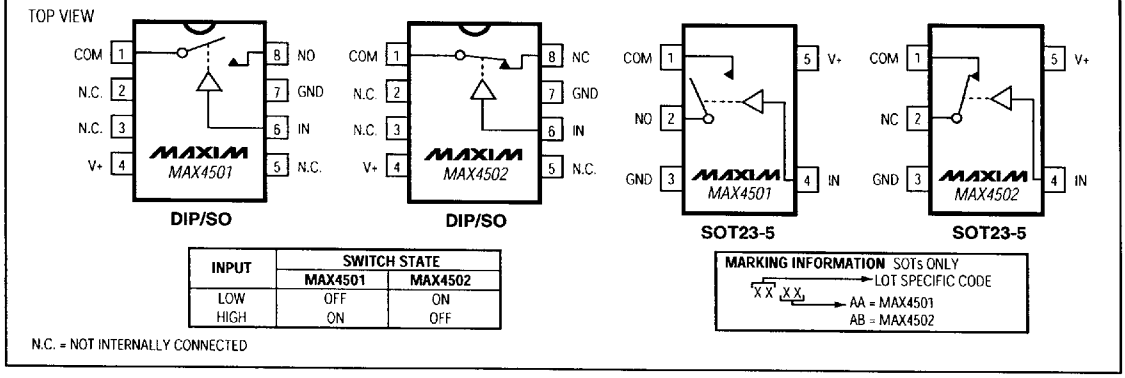
## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX4501**CPA | 0 ℃ to +70 ℃ | 8 Plastic DIP |
| MAX4501CSA | 0 ℃ to +70 ℃ | 8 SO |
| MAX4501CUK | 0 ℃ to +70 ℃ | 5 SOT23-5 |
| MAX4501C/D | 0 ℃ to +70 ℃ | Dice* |
| MAX4501EPA | -40 ℃ to +85 ℃ | 8 Plastic DIP |
| MAX4501ESA | -40 ℃ to +85 ℃ | 8 SO |
| MAX4501EUK | -40 ℃ to +85 ℃ | 5 SOT23-5 |
| MAX4501MJA | -55 ℃ to +125 ℃ | 8 CERDIP** |

***Ordering Information continued at end of data sheet.***

** Contact factory for dice specifications.*
*** Contact factory for availability.*

## Pin Configurations/Functional Diagrams/Truth Table




| INPUT | SWITCH STATE | |
|---|---|---|
| | MAX4501 | MAX4502 |
| LOW | OFF | ON |
| HIGH | ON | OFF |

N.C. = NOT INTERNALLY CONNECTED

**MARKING INFORMATION** SOTs ONLY
XX XX → LOT SPECIFIC CODE
AA = MAX4501
AB = MAX4502

# Low-Voltage, SPST, CMOS Analog Switches

## ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V+ .....-0.3V, +13V
Voltage into Any Terminal (Note 1).....-0.3V to (V+ + 0.3V)
or ±10mA (whichever occurs first)
Continuous Current into Any Terminal.....±10mA
Peak Current, NO_ or COM_
(pulsed at 1ms,10% duty cycle).....±20mA
ESD per Method 3015.7 .....>2000V
Continuous Power Dissipation ($T_A$ = +70 °C)
Plastic DIP (derate 9.09mW/ °C above +70 °C) .....727mW
SO (derate 5.88mW/ °C above +70 °C).....471mW
SOT23-5 (derate 7.1mW/ °C above +70 °C).....571mW
CERDIP (derate 8.00mW/ °C above +70 °C).....640mW
Operating Temperature Ranges
MAX4501C_ _/MAX4502C_ _ .....0 °C to +70 °C
MAX4501E_ _/MAX4502E_ _ .....-40 °C to +85 °C
MAX4501MJA/MAX4502MJA .....-55 °C to +125 °C
Storage Temperature Range .....-65 °C to +150 °C
Lead Temperature (soldering, 10sec) .....+300 °C

**Note 1:** Voltages exceeding V+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS—+5V Supply

(V+ = +4.5V to +5.5V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25 °C.)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP (Note 2) | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | | |
| Analog Signal Range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | | 0 | | V+ | V |
| COM to NO or NC On-Resistance | $R_{ON}$ | $V_{COM}$ = 3.5V, $I_{COM}$ = 1mA | $T_A$ = +25 °C | | | 90 | 250 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | | 350 | |
| NO or NC Off-Leakage Current (Note 3) | $I_{NO(OFF)}$, $I_{NC(OFF)}$ | V+ = 5.5V, $V_{COM}$ = 1V, $V_{NO}$ or $V_{NC}$ = 4.5V | $T_A$ = +25 °C | | -1 | 0.01 | 1 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | C, E | -10 | | 10 | |
| | | | | M | -100 | | 100 | |
| COM Off-Leakage Current (Note 3) | $I_{COM(OFF)}$ | V+ = 5.5V, $V_{COM}$ = 1V, $V_{NO}$ or $V_{NC}$ = 4.5V | $T_A$ = +25 °C | | -1 | 0.01 | 1 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | C, E | -10 | | 10 | |
| | | | | M | -100 | | 100 | |
| COM On-Leakage Current (Note 3) | $I_{COM(ON)}$ | V+ = 5.5V, $V_{COM}$ = 1V, $V_{NO}$ or $V_{NC}$ = 4.5V | $T_A$ = +25 °C | | -2 | 0.01 | 2 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | C, E | -20 | | 20 | |
| | | | | M | -200 | | 200 | |
| **DIGITAL I/O** | | | | | | | | |
| Input Logic High | $V_{IH}$ | | | | 2.4 | | V+ | V |
| Input Logic Low | $V_{IL}$ | | | | 0 | | 0.8 | V |
| Input Current Logic High or Low | $I_{IH}$, $I_{IL}$ | $V_{IN}$ = V+, 0V | | | -1 | 0.03 | 1 | µA |
| **SWITCH DYNAMIC CHARACTERISTICS** | | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO}$ = $V_{NC}$ = 1.5V, $V_{IN}$ = 3V, $R_L$ = 1kΩ Figure 1 | $T_A$ = +25 °C | | | 16 | 75 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | | 150 | |
| Turn-Off Time | $t_{OFF}$ | $V_{NO}$ = $V_{NC}$ = 1.5V, $V_{IN}$ = 3V, $R_L$ = 1kΩ Figure 1 | $T_A$ = +25 °C | | | 10 | 50 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | | 150 | |

## ELECTRICAL CHARACTERISTICS—+5V Supply (continued)

(V+ = +4.5V to +5.5V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25 °C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP (Note 2) | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **SWITCH DYNAMIC CHARACTERISTICS (continued)** | | | | | | | |
| Charge Injection (Note 4) | Q | $C_L$ = 1nF, $V_{NO}$ = 0V, $R_S$ = 0Ω, $T_A$ = +25 °C, Figure 2 | | | 1 | 10 | pC |
| Off Isolation | $V_{ISO}$ | $R_L$ = 50Ω, $C_L$ = 15pF, $V_{NO}$ = 1$V_{RMS}$, f = 100kHz, $T_A$ = +25 °C, Figure 3 | | | < -100 | | dB |
| NO or NC Off Capacitance | $C_{NO(OFF)}$, $C_{NC(OFF)}$ | f = 1MHz, Figure 4 | | | 3 | | pF |
| COM Off Capacitance | $C_{COM(OFF)}$ | f = 1MHz, Figure 4 | | | 3 | | pF |
| COM On Capacitance | $C_{COM(ON)}$ | f = 1MHz, Figure 4 | | | 8 | | pF |
| **POWER SUPPLY** | | | | | | | |
| V+ Supply Current | I+ | $V_{IN}$ = 0V or V+ | $T_A$ = +25 °C | -1 | | 1 | µA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | -10 | | 10 | |

## ELECTRICAL CHARACTERISTICS—+12V Supply

(V+ = +11.4V to +12.6V, $V_{INH}$ = 5.0V, $V_{INL}$ = 0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25 °C.)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP (Note 2) | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | | |
| Analog Signal Range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | | 0 | | V+ | V |
| COM to NO or NC On-Resistance | $R_{ON}$ | $V_{COM}$ = 10V, $I_{COM}$ = 1mA | $T_A$ = +25 °C | | | 40 | 160 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | | 200 | |
| NO or NC Off-Leakage Current (Note 3) | $I_{NO(OFF)}$, $I_{NC(OFF)}$ | $V_{COM}$ = 10V, $V_{NO}$ or $V_{NC}$ = 1V | $T_A$ = +25 °C | | -5 | | 5 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | C, E | -50 | | 50 | |
| | | | | M | -500 | | 500 | |
| COM Off-Leakage Current (Note 3) | $I_{COM(OFF)}$ | $V_{COM}$ = 10V, $V_{NO}$ or $V_{NC}$ = 1V | $T_A$ = +25 °C | | -5 | | 5 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | C, E | -50 | | 50 | |
| | | | | M | -500 | | 500 | |
| COM On-Leakage Current (Note 3) | $I_{COM(ON)}$ | $V_{COM}$ = 10V | $T_A$ = +25 °C | | -10 | | 10 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | C, E | -100 | | 100 | |
| | | | | M | -1000 | | 1000 | |
| **DIGITAL I/O** | | | | | | | | |
| Input Logic High | $V_{INH}$ | | | | 5.0 | | V+ | V |
| Input Logic Low | $V_{INL}$ | | | | 0 | | 0.8 | V |
| Input Current Logic High or Low | $I_{INH}$, $I_{INL}$ | $V_{IN}$ = V+, 0V | | | -1 | 0.03 | 1 | µA |
| **POWER SUPPLY** | | | | | | | | |
| V+ Supply Current | I+ | IN = 0V or V+ | $T_A$ = +25 °C | | -1 | | 1 | µA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | -10 | | 10 | |

## ELECTRICAL CHARACTERISTICS—+3V Supply

(V+ = +3.0V to +3.6V, $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25 °C.)

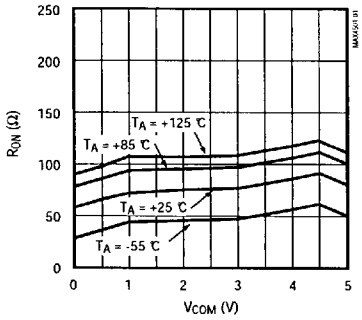
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP (Note 2) | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Analog Signal Range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | 0 | | V+ | V |
| COM to NO or NC On-Resistance | $R_{ON}$ | $V_{COM}$ = 1.5V, $I_{NO}$ = 0.1mA | $T_A$ = +25 °C | | 175 | 600 | Ω |
| | | | $T_A = T_{MIN}$ to $T_{MAX}$ | | | 800 | |
| **DIGITAL I/O** | | | | | | | |
| Input Logic High | $V_{INH}$ | | | 2.4 | | V+ | V |
| Input Logic Low | $V_{INL}$ | | | 0 | | 0.8 | V |
| Input Current Logic High or Low | $I_{INH}$, $I_{INL}$ | $V_{IN}$ = V+, 0V | | -1.00 | 0.03 | 1.00 | µA |
| **SWITCH DYNAMIC CHARACTERISTICS** | | | | | | | |
| Turn-On-Time (Note 4) | $t_{ON}$ | $V_{NO} = V_{NC}$ = 1.5V, $V_{IN}$ = 3V, $R_L$ = 1kΩ Figure 1 | $T_A$ = +25 °C | | 45 | 300 | ns |
| | | | $T_A = T_{MIN}$ to $T_{MAX}$ | | | 500 | |
| Turn-Off-Time (Note 4) | $t_{OFF}$ | $V_{NO} = V_{NC}$ = 1.5V, $V_{IN}$ = 3V, $R_L$ = 1kΩ Figure 1 | $T_A$ = +25 °C | | 10 | 125 | ns |
| | | | $T_A = T_{MIN}$ to $T_{MAX}$ | | | 175 | |
| Charge Injection (Note 4) | Q | $C_L$ = 1nF, $T_A$ = +25 °C, Figure 2 | | | 0.5 | 10 | pC |
| **POWER SUPPLY** | | | | | | | |
| V+ Supply Current | I+ | IN = 0V or V+ | $T_A$ = +25 °C | -1 | | 1 | µA |
| | | | $T_A = T_{MIN}$ to $T_{MAX}$ | -10 | | 10 | |

**Note 2:** The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
**Note 3:** Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are guaranteed by correlation at +25 °C.
**Note 4:** Guaranteed, not production tested.
**Note 5:** SOT packaged parts are 100% tested at +25 °C. Limits at maximum and minimum rated temperature are guaranteed by design and correlation limits at +25 °C.

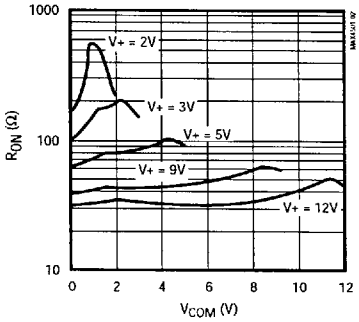
## Typical Operating Characteristics

(V+ = 5V, GND = 0V, $T_A$ = +25 °C, unless otherwise noted.)

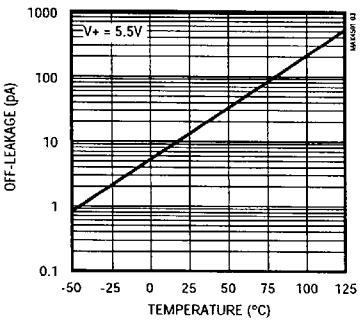
**ON-RESISTANCE vs. $V_{COM}$ AND TEMPERATURE**



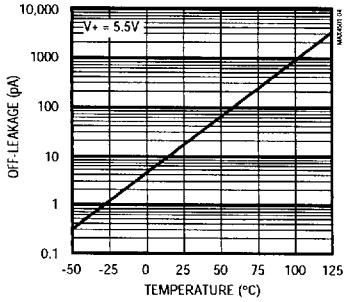

**ON-RESISTANCE vs. $V_{COM}$**



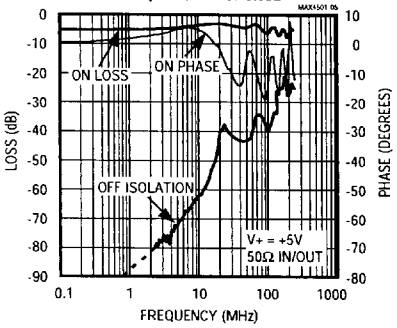

**OFF-LEAKAGE vs. TEMPERATURE**



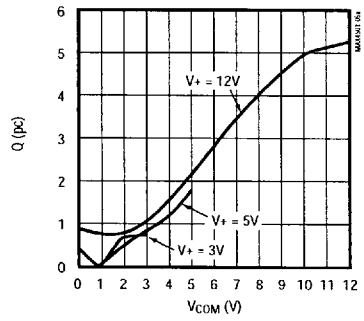

**OFF-LEAKAGE vs. TEMPERATURE**



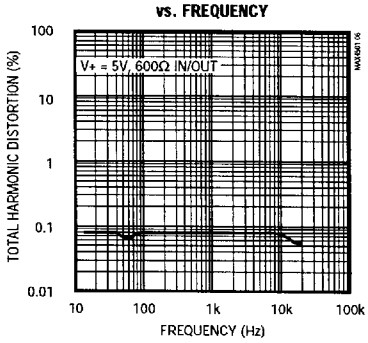

**FREQUENCY RESPONSE**



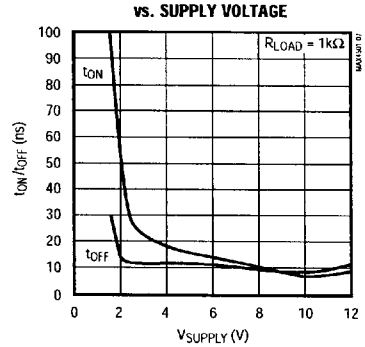

**CHARGE INJECTION vs. $V_{COM}$**




**TOTAL HARMONIC DISTORTION vs. FREQUENCY**




**SWITCHING TIME vs. SUPPLY VOLTAGE**



# Low-Voltage, SPST, CMOS Analog Switches

## Pin Description

| PIN | | | | NAME | FUNCTION |
|---|---|---|---|---|---|
| MAX4501 | | MAX4502 | | | |
| DIP/SO | SOT23-5 | DIP/SO | SOT23-5 | | |
| 1 | 1 | 1 | 1 | COM | Analog Switch Common Terminal |
| 2, 3, 5 | — | 2, 3, 5 | — | N.C. | No Connect (not internally connected) |
| 4 | 5 | 4 | 5 | V+ | Positive Supply-Voltage Input (analog and digital) |
| 6 | 4 | 6 | 4 | IN | Digital Control Input |
| 7 | 3 | 7 | 3 | GND | Ground |
| 8 | 2 | — | — | NO | Analog Switch (normally open) |
| — | — | 8 | 2 | NC | Analog Switch (normally closed) |

Note: NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass equally well in both directions.

## Applications Information

### Power-Supply Considerations

The MAX4501/MAX4502 are constructed like most CMOS analog switches, except they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set the analog voltage limits of the switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and V+ or GND.

V+ and GND also power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels to switched V+ and GND signals to drive the analog signal gates. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. COM, NO, and NC pins have ESD-protection diodes to V+ and GND.

The logic-level thresholds are CMOS/TTL-compatible when V+ is +5V. As V+ is raised, the threshold increases slightly. When V+ reaches +12V, the logic-level threshold is about 3V—above the TTL guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

**Do not connect the MAX4501/MAX4502's V+ to +3V and then connect the logic-level pins to TTL logic-level signals. TTL levels can exceed +3V and violate the absolute maximum ratings, damaging the part and/or external circuits.**

### High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 250MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks which are highly layout dependent. The problem is not in turning the switch on; it's in turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -60dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher circuit impedances also cause off isolation to decrease. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

## Test Circuits/Timing Diagrams

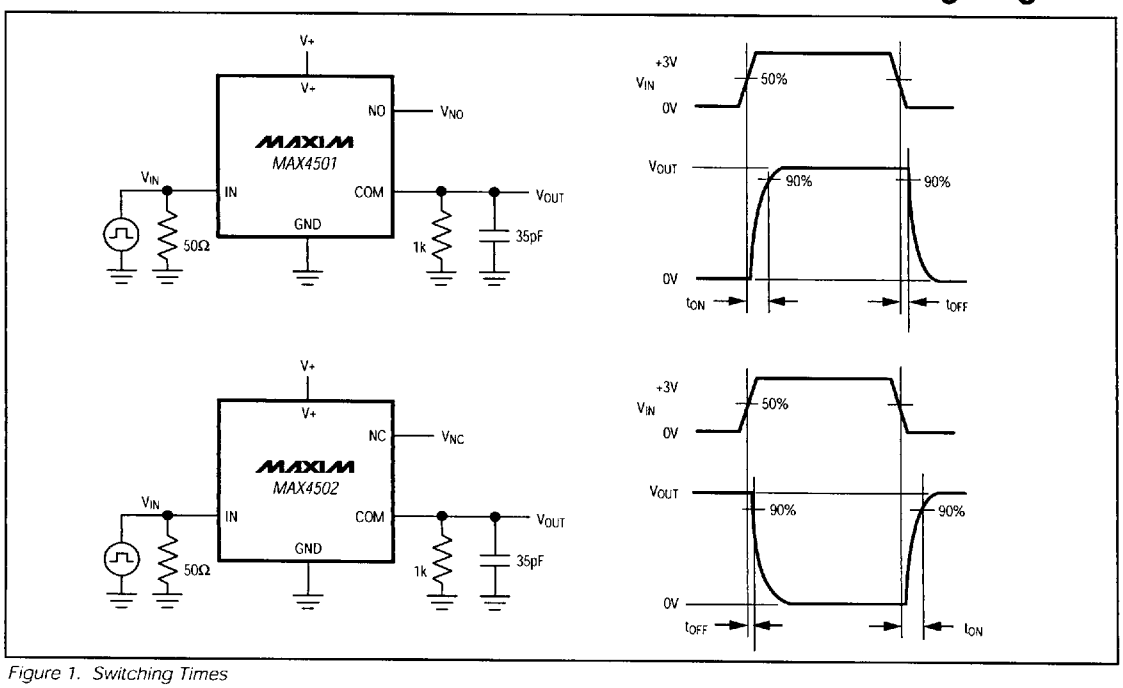



*Figure 1. Switching Times*

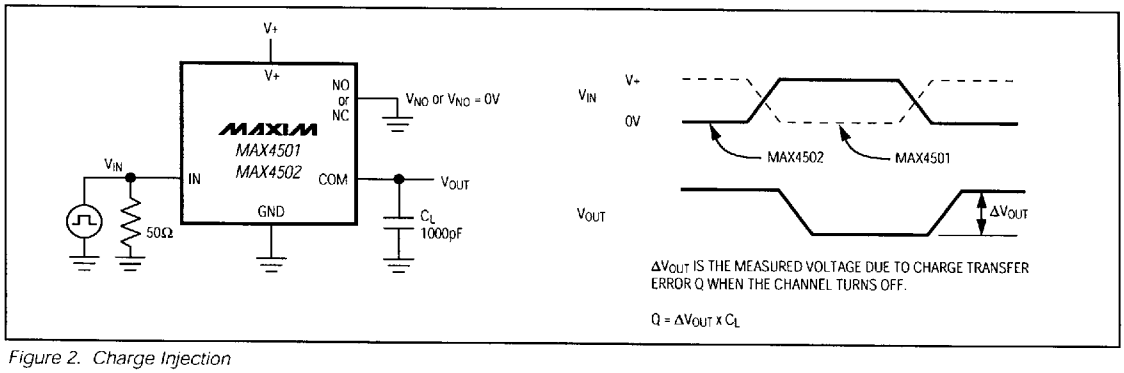



*Figure 2. Charge Injection*

# Low-Voltage, SPST, CMOS Analog Switches

## Test Circuits/Timing Diagrams (continued)

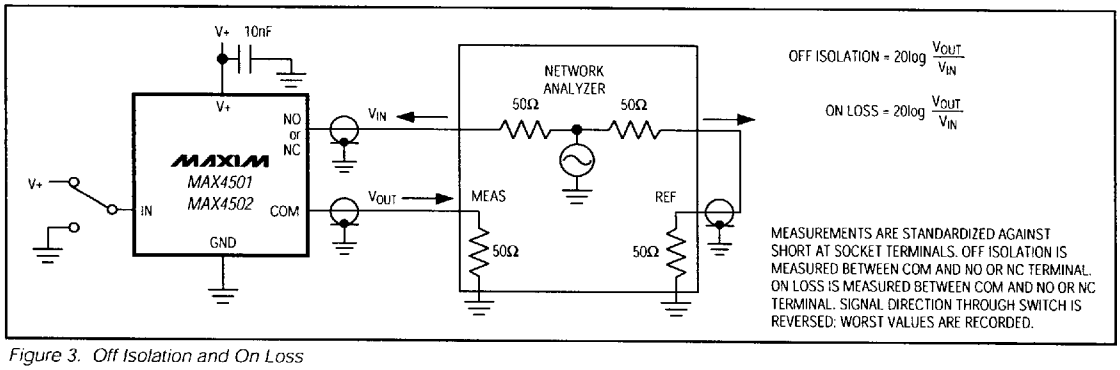



*Figure 3. Off Isolation and On Loss*

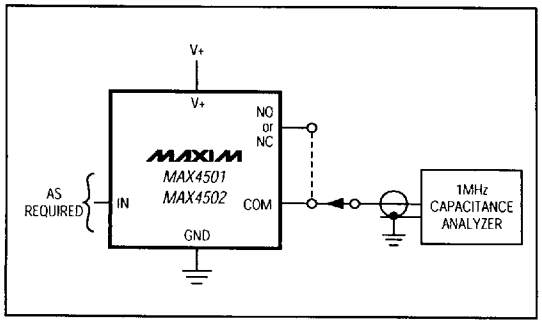
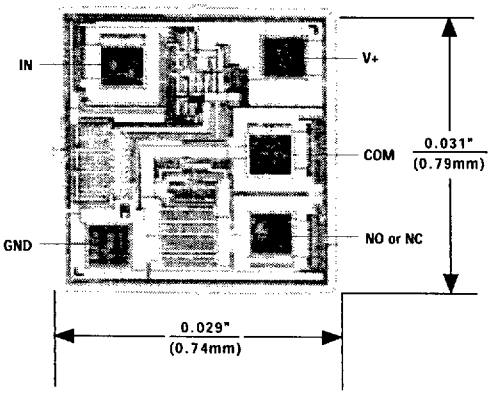



*Figure 4. NO, NC, and COM Capacitance*

## Chip Topography




TRANSISTOR COUNT: 17

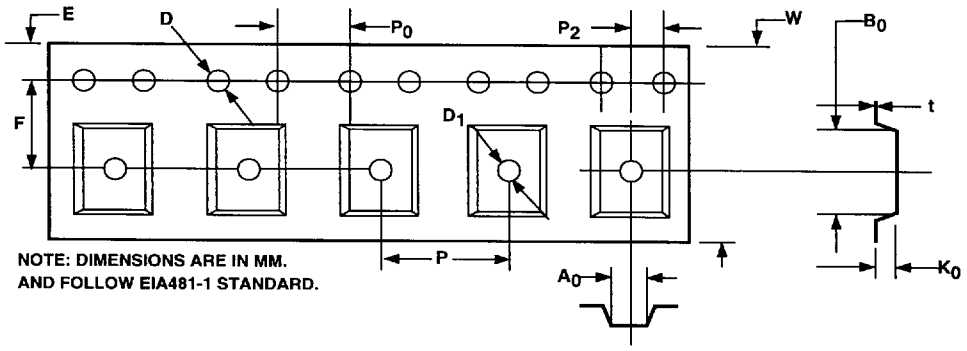
SUBSTRATE CONNECTED TO V+

## Ordering Information (continued)

| PART | TEMP. RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX4502**CPA | 0 ℃ to +70 ℃ | 8 Plastic DIP |
| MAX4502CSA | 0 ℃ to +70 ℃ | 8 SO |
| MAX4502CUK | 0 ℃ to +70 ℃ | 5 SOT23-5 |
| MAX4502C/D | 0 ℃ to +70 ℃ | Dice* |
| MAX4502EPA | -40 ℃ to +85 ℃ | 8 Plastic DIP |
| MAX4502ESA | -40 ℃ to +85 ℃ | 8 SO |
| MAX4502EUK | -40 ℃ to +85 ℃ | 5 SOT23-5 |
| MAX4502MJA | -55 ℃ to +125 ℃ | 8 CERDIP** |

** Contact factory for dice specifications.*
*** Contact factory for availability.*

## Tape-and-Reel Information




NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

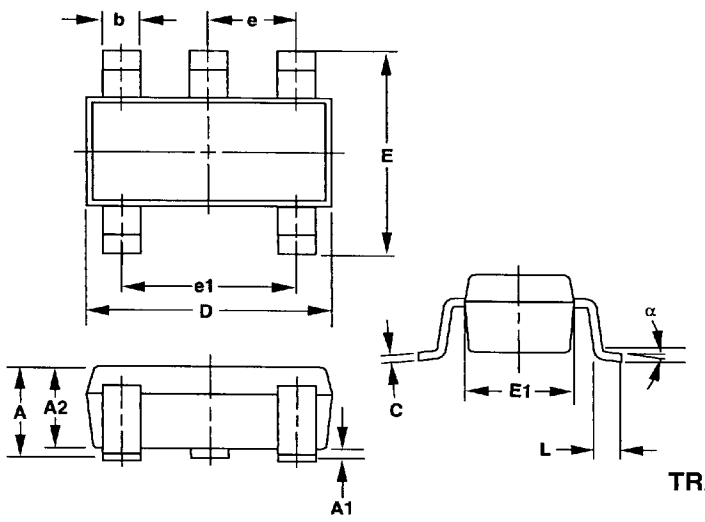
| | | |
|---|---|---|
| $A_0$ | 3.200 | ±0.102 |
| $B_0$ | 3.099 | ±0.102 |
| D | 1.499 | +0.102<br>+0.000 |
| $D_1$ | 0.991 | +0.254<br>+0.000 |

| | | |
|---|---|---|
| E | 1.753 | ±0.102 |
| F | 3.505 | ±0.051 |
| $K_0$ | 1.397 | ±0.102 |
| P | 3.988 | ±0.102 |

| | | |
|---|---|---|
| $P_0$ | 3.988 | ±0.102 |
| $P_0$10 | 40.005 | ±0.203 |
| $P_2$ | 2.007 | ±0.051 |
| t | 0.254 | ±0.127 |
| W | 8.001 | +0.305<br>-0.102 |

5 SOT23-5

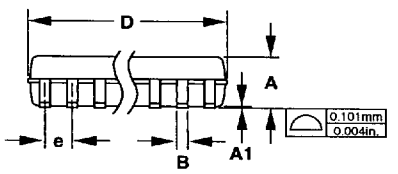
## Package Information

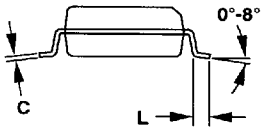



| DIM | MILLIMETERS | |
|---|---|---|
| | MIN | MAX |
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.35 | 0.50 |
| C | 0.08 | 0.20 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.75 |
| L | 0.35 | 0.55 |
| e | 0.95ref | |
| e1 | 1.90ref | |
| α | 0° | 10° |

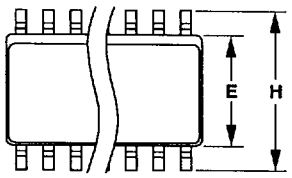
21-0057B

**5-PIN SOT23-5 SMALL-OUTLINE TRANSISTOR PACKAGE**




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| e | 0.050 | | 1.27 | |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

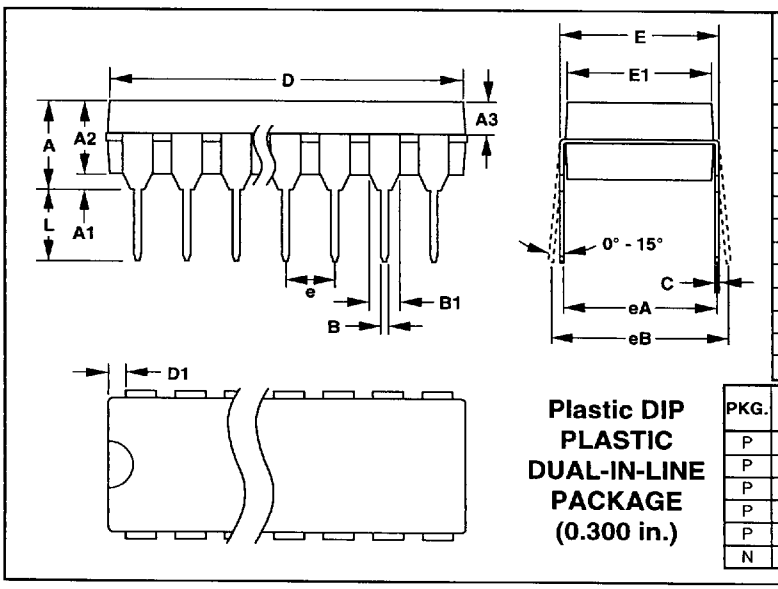



**Narrow SO SMALL-OUTLINE PACKAGE (0.150 in.)**

| DIM | PINS | INCHES | | MILLIMETERS | |
|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX |
| D | 8 | 0.189 | 0.197 | 4.80 | 5.00 |
| D | 14 | 0.337 | 0.344 | 8.55 | 8.75 |
| D | 16 | 0.386 | 0.394 | 9.80 | 10.00 |

21-0041A

## Package Information (continued)




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | – | 0.200 | – | 5.08 |
| A1 | 0.015 | – | 0.38 | – |
| A2 | 0.125 | 0.175 | 3.18 | 4.45 |
| A3 | 0.055 | 0.080 | 1.40 | 2.03 |
| B | 0.016 | 0.022 | 0.41 | 0.56 |
| B1 | 0.045 | 0.065 | 1.14 | 1.65 |
| C | 0.008 | 0.012 | 0.20 | 0.30 |
| D1 | 0.005 | 0.080 | 0.13 | 2.03 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.310 | 6.10 | 7.87 |
| e | 0.100 | – | 2.54 | – |
| eA | 0.300 | – | 7.62 | – |
| eB | – | 0.400 | – | 10.16 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |

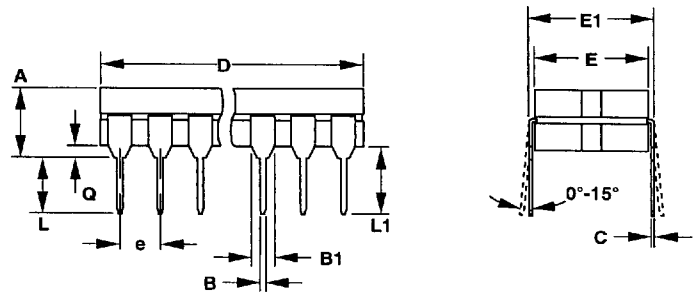
**Plastic DIP PLASTIC DUAL-IN-LINE PACKAGE (0.300 in.)**

| PKG. | DIM | PINS | INCHES | | MILLIMETERS | |
|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX |
| P | D | 8 | 0.348 | 0.390 | 8.84 | 9.91 |
| P | D | 14 | 0.735 | 0.765 | 18.67 | 19.43 |
| P | D | 16 | 0.745 | 0.765 | 18.92 | 19.43 |
| P | D | 18 | 0.885 | 0.915 | 22.48 | 23.24 |
| P | D | 20 | 1.015 | 1.045 | 25.78 | 26.54 |
| N | D | 24 | 1.14 | 1.265 | 28.96 | 32.13 |

21-0043A

# Low-Voltage, SPST, CMOS Analog Switches

## Package Information (continued)




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | – | 0.200 | – | 5.08 |
| B | 0.014 | 0.023 | 0.36 | 0.58 |
| B1 | 0.038 | 0.065 | 0.97 | 1.65 |
| C | 0.008 | 0.015 | 0.20 | 0.38 |
| E | 0.220 | 0.310 | 5.59 | 7.87 |
| E1 | 0.290 | 0.320 | 7.37 | 8.13 |
| e | 0.100 | | 2.54 | |
| L | 0.125 | 0.200 | 3.18 | 5.08 |
| L1 | 0.150 | – | 3.81 | – |
| Q | 0.015 | 0.070 | 0.38 | 1.78 |
| S | – | 0.098 | – | 2.49 |
| S1 | 0.005 | – | 0.13 | – |

**CERDIP**
**CERAMIC DUAL-IN-LINE**
**PACKAGE**
**(0.300 in.)**

| DIM | PINS | INCHES | | MILLIMETERS | |
|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX |
| D | 8 | – | 0.405 | – | 10.29 |
| D | 14 | – | 0.785 | – | 19.94 |
| D | 16 | – | 0.840 | – | 21.34 |
| D | 18 | – | 0.960 | – | 24.38 |
| D | 20 | – | 1.060 | – | 26.92 |
| D | 24 | – | 1.280 | – | 32.51 |

21-0045A